CLC011 Serial Digital Video Decoder

Check for Samples: CLC011

FEATURES

- **Data decoding and deserializing**
- **CLC011B operates to 360Mbps**
- **Low noise injection to power supplies**
- **Single +5V or −5.2V supply operation**
- **Output levels programmable for interface to 5V or 3.3V logic**
- **Low power**
- **Low cost**

DESCRIPTION

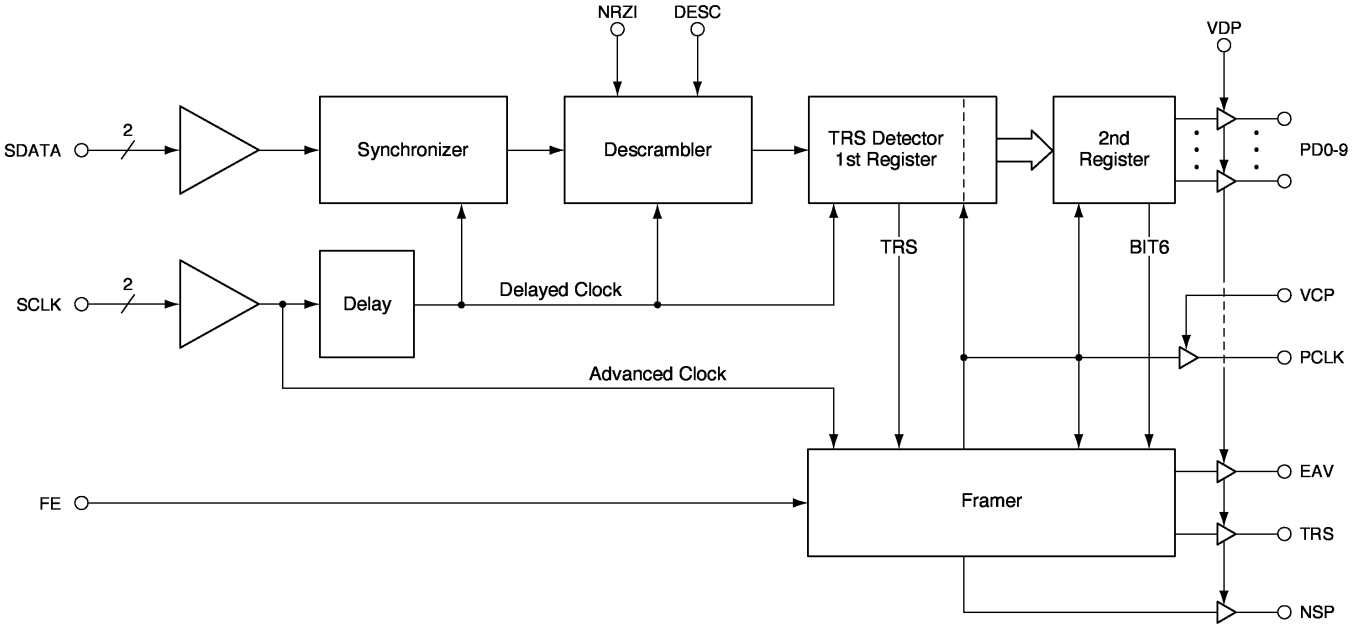
TI's Comlinear CLC011, Serial Digital Video Decoder, decodes and descrambles SMPTE 259M standard Serial Digital Video datastreams with serial clock into 10-bit parallel words and a corresponding word-rate clock. SMPTE 259M standard parallel data is encoded and scrambled using a 9-bit shift register and is also converted from NRZ to NRZI. The CLC011 restores the original parallel data by reversing the encoding process. The CLC011 also extracts timing information embedded in the SDV data. These reserved code words, known as Timing Reference Signals (TRS), indicate the start and end of each active video line. By decoding the TRS, the CLC011 correctly identifies the word boundaries of the encoded input data. Detection of the TRS reserved codes is indicated by low-true signals at the TRS and End of Active Video (EAV) outputs.

The CLC011's design using current-mode logic (CML) reduces noise injection into the power supply thereby easing board layout and interfacing. The CMOS compatible outputs, which feature controlled rise and fall times, may be set for either 3.3V or 5V swings with the VDP and VCP inputs.

The CLC011 Serial Digital Video Decoder, CLC014 Adaptive Cable Equalizer and the CLC016 Data Retiming PLL combine to provide a complete Serial Digital Video receiver system.

The CLC011 is packaged in a 28-pin PLCC.

Block Diagram



Connection Diagram

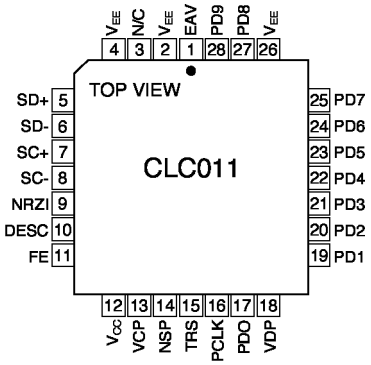


Figure 1. 28-Pin PLCC

Table 1. Pin Descriptions

Name	Pin No.	Description
EAV	1	End of active video flag. For component video, a logic low is output for one cycle of the parallel clock every time an EAV timing reference is detected. The pulse is aligned with the fourth word of the timing reference (the XYZ word). For composite video, this line is always asserted high.
V_{EE}	2, 4, 26	Negative supply pins.
NC	3	Unused pin.
SDI+, SDI−	5, 6	Differential serial data inputs.
SCI+, SCI−	7, 8	Differential serial clock inputs.
NRZI	9	A logic high at this pin enables NRZI-to-NRZ conversion.
DESC	10	A logic high at this pin enables descrambling.
FE	11	Frame enable. Enables resynchronization of the parallel word at the next TRS.
V_{CC}	12	Positive supply pin.
VCP	13	Parallel clock high level programming pin. The voltage at this supply pin defines the logic high level for the parallel clock output.

Table 1. Pin Descriptions (continued)

Name	Pin No.	Description
NSP	14	New sync position. Indicates that the most recent TRS is in a new position relative to the previous TRS. Remains high until the parallel rate clock is aligned properly with the TRS.
TRS	15	Timing reference flag. A logic low is output for the duration of the TRS.
PCLK	16	Parallel clock output. The rising edge of this clock is located at the center of the parallel data window.
PD0–9	17, 19–25, 27, 28	Parallel data outputs.
VDP	18	Parallel data high level programming pin. The voltage at this supply pin defines the logic high level for the data outputs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC}–V_{EE})	+6V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
ESD Rating (HBM)	
PDx	500V
other	2kV
Package Thermal Resistance	
θ_{JA} 28-Pin PLCC	85°C/W
θ_{JC} 28-Pin PLCC	35°C/W
Reliability Information	
Transistor Count	3076

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC}–V_{EE})	4.5V to 5.5V
Logic High Voltage	
(V_{CP}–V_{EE} and V_{DP}–V_{EE})	3.0V to 5.5V
Operating Temperature	0°C to +70°C

Electrical Characteristics[1][2]

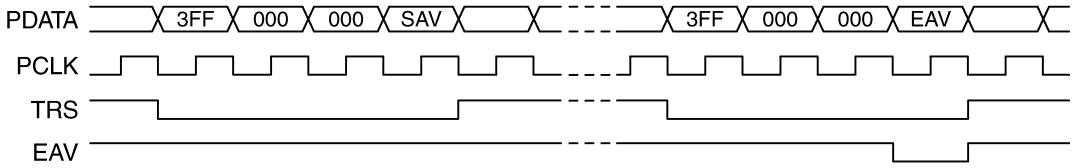
(V_{CC} = +5V, V_{EE} = 0V, C_L = 10 pF; unless specified).

Parameter	Conditions	Typ +25°C	Min/Max +25°C[3]	Min/Max 0°C to +70°C[3]	Units
DYNAMIC PERFORMANCE					
Minimum Serial Data Rate[4]		0			Mbps
Maximum Serial Data Rate[4]		400	360	360	Mbps
PDn and PCLK Rise/Fall Time[5]	C_L = 2 pF,[6]	2.0			ns
PDn and PCLK Rise/Fall Time[5]	C_L = 20 pF,[6]	4.0			ns
PCLK Rising Edge Residual Jitter	[6]	50			ps_{pp}
TIMING PERFORMANCE					
SD to SC Setup Time			0.2	0.2	ns
SC to SD Hold Time			0	0	ns
PDn to PCLK Skew	[6]	±0.8			ns
PDn Valid to PCLK ↑	PCLK = 27 MHz, [6]	18			ns
PCLK ↑ to PDn Invalid	PCLK = 27 MHz, [6]	18			ns
Digital Latency	[7][8][6]	42			sclk cycles
Output Buffer Latency	[8] [6]	10			ns
STATIC PERFORMANCE					
I_{CC} Supply Current	[6] V_{CC} Pin	44			mA
VDP and VCP Supply Current	PCLK = 0 MHz, [6]	2			mA
VDP and VCP Supply Current	PCLK = 27 MHz, [6]	12			mA
SD and SC Inputs					
Input Range Upper Limit			V_{CC}	V_{CC}	V
Input Range Lower Limit			V_{EE} +2.5	V_{EE} +2.5	V
Minimum Differential Input			200	200	mV
I_{IH}			10	15	µA
FE, NRZI, and DESC Inputs					
V_{IL}			V_{EE} +0.8	V_{EE} +0.8	V
V_{IH}			V_{EE} +2.0	V_{EE} +2.0	V
Outputs					
V_{OL}	I_{OL} = 10 mA		V_{EE} +0.5	V_{EE} +0.5	V
V_{OH}	I_{OH} = 10 mA		V_{CC} −0.5	V_{CC} −0.5	V
MISCELLANEOUS PERFORMANCE					
SD and SC Input Capacitance	[6]	2.0			pF
SD and SC Input Resistance	[6]	20			kΩ

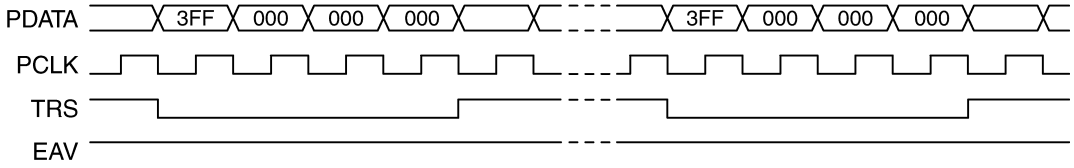
(1) See Timing Diagrams.
(2) 100% tested at 25°C, sample tested over temperature.
(3) Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
(4) Nominal position of rising edge of serial clock is at the center of the serial data eye.
(5) Nominal position of the rising edge of PCLK is at the center of the PDn eye.
(6) Typicals only specified.
(7) Data latency due to digital registers, measured from MSB of serial data to parallel clock out.
(8) Total latency is the digital latency plus the output buffer latency.

Timing Diagrams

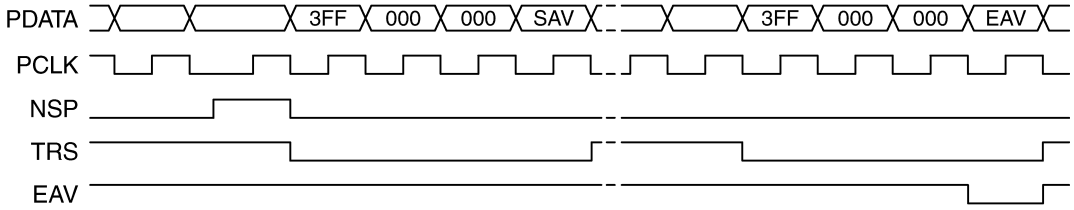
TRS and EAV Timing – Component Video



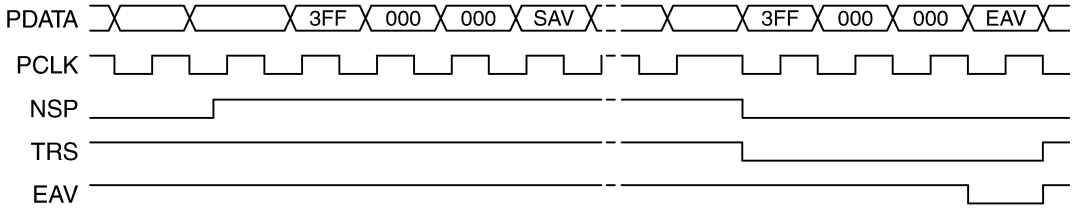
TRS and EAV Timing – Composite Video



Resynchronization Timing – FE tied to V_{CC}



Resynchronization Timing – FE tied to NSP



Overview

The CLC011, Serial Digital Video Decoder, decodes and descrambles SMPTE 259M standard Serial Digital Video datastreams into 10-bit parallel words and a corresponding word-rate clock. The following information describes:

- the CLC011 operation,
- recommended interface circuitry, and
- PCB layout suggestions.

Applications assistance for the CLC011 may be obtained by calling the Interface Applications Hotline, (408) 721-8500.

Input Interfacing—Signal Inputs

The serial data and clock inputs of the CLC011 are both differential. Their input voltage ranges from 2.5V above the negative supply (V_{EE} +2.5V) to the positive supply voltage (V_{CC}). Supply voltages for the CLC011 may be either +5V or –5.2V for ECL compatibility and interfacing. When operated from the negative supply, inputs accept standard ECL signal levels. The minimum differential input swing is 200 mV. The CLC011 interfaces with the CLC016 Data Retiming PLL as shown in Figure 2. A simplified schematic of the CLC011's signal inputs appears in Figure 3.

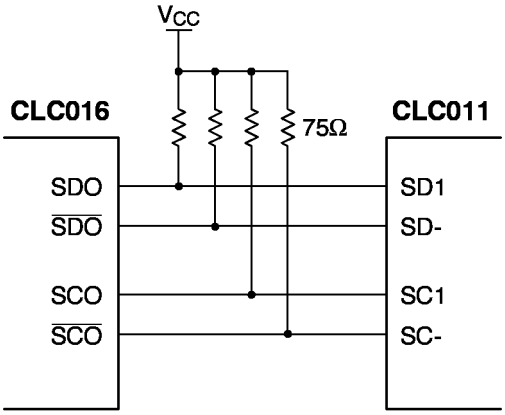


Figure 2. Interface with CLC016

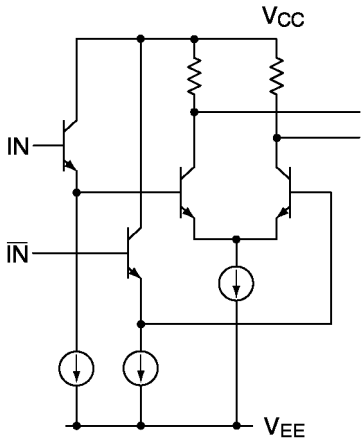


Figure 3. Simplified Input Buffer Schematic

Input Interfacing—Control Inputs

Three TTL-compatible inputs control operation of the CLC011: NRZI, DESC and FE. A typical interface circuit for the control inputs is shown in Figure 4.

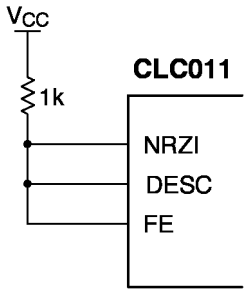


Figure 4. Typical Control Logic Connection

NRZI: NRZI, when a logic high, enables NRZI to NRZ conversion. For standard SMPTE 259M operation, NRZI is high.

DESC (Descramble): The bits of a SMPTE 259M datastream are scrambled upon encoding according to a polynomial equation. DESC, when a logic high, enables descrambling of the encoded signal. For standard SMPTE 259M operation, DESC is high.

FE (Framing Enable): SMPTE 259M datastreams include a four-word-long reserved sequence known as the Timing Reference Signal (TRS). Using this sequence, the CLC011 determines the position of word boundaries, also known as framing, of the incoming data.

The FE input, when a logic high and following recognition of a TRS, causes the CLC011 to automatically adjust its framing. The word boundary is aligned at the appropriate bit position and the parallel output clock is aligned with the appropriate cycle of the serial clock. When FE is held low and a TRS, out of phase with the current PCLK, is received, output NSP will go high. However, the phase of PCLK will not be adjusted. NSP will remain high until a TRS, in-phase with the current PCLK, is received.

FE is normally conditioned in one of three ways.

1. **FE tied high.** This is the most common mode for FE. In this mode, when a TRS is received, PCLK is aligned to the new TRS. If a new sync position (NSP) is identified, the NSP output will go high until the next TRS is received.
2. **FE tied to NSP.** When in this mode, if a TRS that is out of phase with the existing PCLK is detected, NSP will go high, but the phase of PCLK will not be adjusted. If the next TRS received is in-phase with PCLK, NSP will go low and the decoder will continue without changing its state. If the next TRS to arrive is out of phase with PCLK, then PCLK's phase is adjusted to meet the new TRS and NSP is made low. Single erroneous TRS pulses are ignored in this mode, but if they persist, the decoder will re-adjust PCLK to properly frame the data.
3. **FE held low during active video.** The automatic framing feature using the TRS may be disabled in cases where non-SMPTE 259M signals are being processed. In some applications like computer-generated animation, the serial video data may not adhere to the SMPTE 259M standard and patterns that resemble TSR's can occur within the active video line. When such patterns occur and to prevent the CLC011 from attempting re-framing, make FE a logic low during the active video line.

Output Interface—Output Logic Levels

All outputs of the CLC011 are CMOS compatible. They can be programmed to provide appropriate output logic levels to connect to following stages operating from supplies of 3.0V to 5.5V. Output voltages are set by applying the positive supply voltage powering the following stage to VDP, which controls PD0-9, EAV, TRS and NSP, and VCP, which controls PCLK. An example of the CLC011, powered from +5V, driving a device powered from a 3.3V supply is shown in Figure 5.

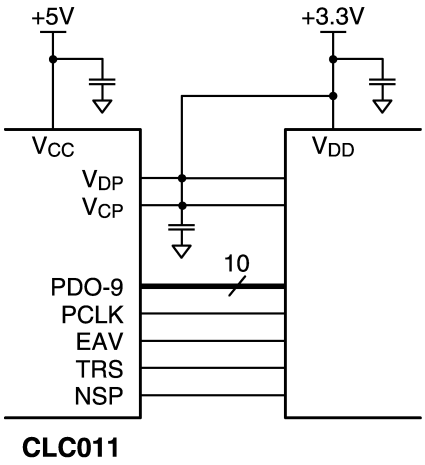


Figure 5. Typical Output Interface

The CLC011's output drivers, shown simplified in Figure 6, are designed to maintain a constant, controlled slew rate regardless of load. This design results in lower output switching noise injection via the supply pins and into other circuitry. Even so, it is recommended that the CLC011 and other digital circuitry be separated from analog circuitry and cable equalizers.

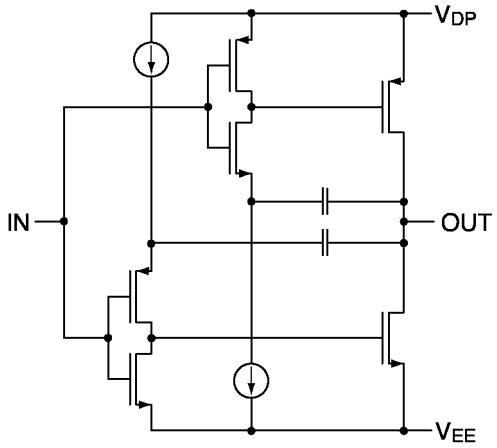


Figure 6. Simplified Output Buffer Schematic

Output Interface—Control Outputs

PCLK (Parallel Clock): The parallel output or word clock, PCLK, is synchronous with the parallel data outputs, PD0–9. The rising edge of PCLK is located at the center of the parallel data window.

TRS (Timing Reference Signal): The active-low TRS output pulse is four parallel clock periods long. TRS is active during decoding of both composite and component video signals.

EAV (End of Active Video): The EAV output is pulsed low for one cycle of the parallel clock every time an EAV timing reference is detected during decoding of component video. The pulse is coincident with the fourth word of the timing reference (the XYZ word). During reception of composite video, this output is always asserted high.

NSP (New Sync Position): The active-low NSP output indicates that the most recently received TRS is in a different position relative to the previous TRS. NSP remains high until the parallel rate clock is properly aligned with the TRS, then goes low.

PCB Layout Guidelines

The CLC011 is not as sensitive to PCB layout as some Serial Digital Video decoders. The following suggestions will help achieve and maintain optimum system performance.

1. Locate the CLC011 decoder away from equalizers and other sensitive circuitry to avoid unwanted crosstalk from clock and data outputs which may degrade system performance.
2. The trace from the signal input connector to the CLC011 must be kept short and should not run parallel to the data output traces.
3. Bypass each power pin with a 0.01 µF to 0.1 µF monolithic ceramic capacitor.
4. Power the CLC011 and other clock recovery circuitry from a separate power supply network from that of other digital circuitry on the board.

Other PCB layout tips may be found in: “Keeping Analog Signals Pure in a Hostile Digital World”, Electronic Design, Special Analog Issue, June 24, 1996, available from Texas Instruments. Request Literature number 665502-001.

Evaluation Board

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the SDI/SDV/SDH devices. The evaluation boards can be ordered through TI's Distributors. Supplies are limited, please check for current availability.

The SD901EVK SMPTE 259M Receiver evaluation kit provides an operating environment in which the decoder can be evaluated by system / hardware designers. The evaluation board has all the needed circuitry and connectors for easy connection and checkout of the device circuit options as discussed in the CLC011 datasheet. A schematic, parts list and pictorial drawing are provided with the board.

From the WWW, the following information may be viewed / downloaded for most evaluation boards: www.national.com/appinfo/interface

- Device Datasheet and / or EVK User Manual
- View a picture of the EVK
- View the EVK Schematic
- View the top assembly drawing and BOM
- View the bottom assembly drawing and BOM

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