National Semiconductor

PRELIMINARY

COP420P/COP444CP/COP444LP Piggyback EPROM Microcontrollers

General Description

The COP420P, COP444CP, and COP444LP are piggyback versions of the COPS™ microcontroller families. These devices are identical to their respective device except the program ROM has been removed. The device package incorporates the circuitry and socket on top of package to accommodate the piggyback EPROM—MM2716, NMC27C16 or other appropriate EPROMs. With the addition of an EPROM, the device performs exactly as its masked equivalent.

The device is a complete microcontroller system with CPU, RAM, I/O and EPROM socket in a 28-lead package. The completed package allows field test of the system in the final electrical and mechanical configuration. This important benefit facilitates development and debug of the COP400 program prior to masking of a production part.

These devices are also economical in low and medium volume applications or when the program may require changing.

Device Selection	Device Emulated	Piggyback Device
Low Power NMOS	COP420L, COP444L	COP444LP
High Speed NMOS	COP420	COP420P
Low Power CMOS	COP424C, COP444C	COP444CP

Features

COP444LP

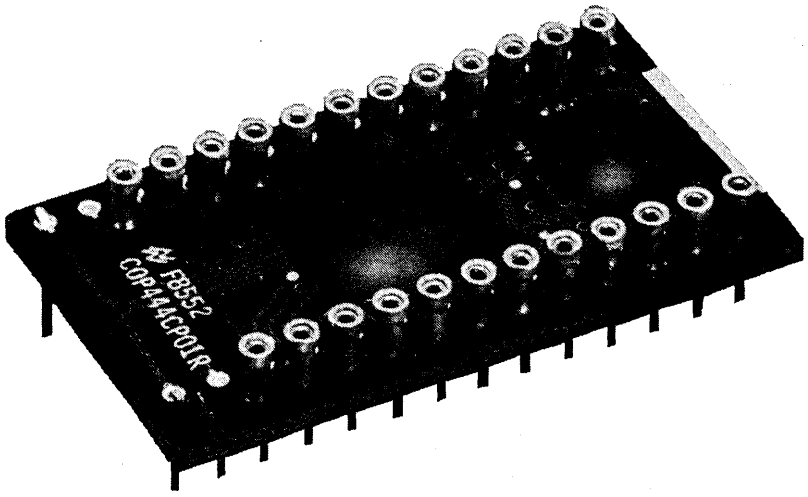
- 16 μs instruction time
- Same Specification as COP404LSN-5

COP420P

- 4 μs instruction time
- Same Specification as COP402N

COP444CP

- 4 μs instruction time
- Fully static (can turn off clock)
- Power-saving IDLE state and Halt mode
- Same Specification as COP404CN



TL/DD/8705-10

COP420P Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to +7V
Operating Temperature Range	
COP420P	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Total Sink Current	50 mA
Total Source Current	70 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

COP420P DC Electrical Characteristics

$0°C \le T_A \le 70°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operation Voltage		4.5	5.5	V
Power Supply Ripple	Peak to Peak (Note 3)		0.4	V
Supply Current	All Outputs Open		81	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High	V_{CC} = 5.5V	3.0		V
Logic High	V_{CC} = 4.5V	2.0		V
Logic Low		−0.3	0.4	V
Schmitt Trigger Input				
RESET				
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ±10%	2.0		V
Logic Low		−0.3	0.8	V
Input Load Source Current	V_{CC} = 5V, V_{IN} = 0V	−100	−800	μA
Input Capacitance			7	pF
Hi-Z Input Leakage		−1	+1	μA
Output Voltage Levels				
D, G, L, SK, SO Outputs				
TTL Operation	V_{CC} = 5V ±10%			
Logic High	I_{OH} = −100 μA	2.0		V
Logic Low	I_{OL} = 1.6 mA	−0.3	0.4	V
IP0–IP7, P8, P9, SKIP, CKO, AD/$\overline{DATA}$				
Logic High	I_{OH} = −75 μA	2.4		V
Logic Low	I_{OL} = 400 μA	−0.3	0.4	V
CMOS Operation (Note 2)				
Logic High	I_{OH} = −10 μA	V_{CC} − 1		V
Logic Low	I_{OL} = 10 μA	−0.3	0.2	V
Output Current Levels				
LED Direct Drive (Note 3)	V_{CC} = 5.0V			
Logic High	V_{OH} = 2.0V	1.0	14	mA
Allowable Sink Current				
Per Pin (L, D, G)			10	mA
Per Pin (All Others)			2	mA
Per Port (L)			16	mA
Per Port (D, G)			10	mA
Allowable Source Current				
Per Pin (L)			−15	mA
Per Pin (All Others)			−1.5	mA

COP420P AC Electrical Characteristics

$0°C \le T_A \le 70°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time		4	10	μs
Operating CKI Frequency	÷16 Mode	1.6	4.0	MHz
CKI Duty Cycle (Note 1)		40	60	%
Rise Time	Frequency = 4 MHz		60	ns
Fall Time	Frequency = 4 MHz		40	ns
Inputs				
SI				
t_{SETUP}		0.3		μs
t_{HOLD}		250		ns
All Other Inputs				
t_{SETUP}		1.7		μs
t_{HOLD}		300		ns
Output Propagation Delay	R_L = 5k, C_L = 50 pF, V_{OUT} = 1.5V			
SO and SK				
t_{pd1}			1.0	μs
t_{pd0}			1.0	μs
CKO				
t_{pd1}			0.25	μs
t_{pd0}			0.25	μs
AD/DATA, SKIP				
t_{pd1}			0.6	μs
t_{pd0}			0.6	μs
All Other Outputs				
t_{pd1}			1.4	μs
t_{pd0}			1.4	μs

Note 1: Duty cycle = $t_{W1}/(t_{W1} + t_{W0})$.

Note 2: Voltage change must be less than 0.5V in a 1 ms period.

Note 3: Exercise great care not to exceed maximum device power dissipation limits when direct driving LEDs (or sourcing similar loads) at high temperature.

COP444CP Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

COP444CP DC Electrical Characteristics

0°C < T_A < 70°C, 4.5V ≤ V_{CC} ≤ 5.5V unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		4.5	5.5	V
Power Supply Ripple (Note 3)	Peak to Peak		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 5V, t_C = 4 μs		15	mA
Input Voltage Levels				
RESET, D0				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-Up Current	V_{CC} = 4.5V, V_{IN} = 0	30	330	μA
Hi-Z Input Leakage		−1	+1	μA
Input Capacitance			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ±5%			
Logic High	I_{OH} = −100 μA	2.7		V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10 μA		0.2	V
Output Current Levels				
Sink (Note 6)	V_{CC} = 4.5V, V_{OUT} = V_{CC}	1.2		mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V	0.5		mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V	30	330	μA
Allowable Sink/Source Current Per Pin (Note 4)			5	mA
Allowable Loading on CKOH			100	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 2 V_{CC}		0.7	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 7 V_{CC}		1.6	mA
TRI-STATE Leakage Current		−2.5	+2.5	μA

COP444CP AC Electrical Characteristics

$0°C < T_A < 70°C$, $4.5V \leq V_{CC} \leq 5.5V$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (t_C)	$V_{CC} \geq 4.5V$	4	DC	μs
Operating CKI Frequency	$V_{CC} \geq 4.5V$	DC	1.0	MHz
Inputs				
t_{SETUP}	G Inputs }	$t_C/4 + 0.7$		μs
	SI Input } $V_{CC} \geq 4.5V$	0.3		μs
	IP Input }	1.0		μs
	All Others }	1.7		μs
t_{CLOCK}	$V_{CC} \geq 4.5V$	0.25		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
IP7–IP0, A10–A8, SKIP				
$t_{(pd1)}$, $T_{(pd0)}$	$V_{CC} \geq 4.5V$		1.94	μs
AD/$\overline{DATA}$				
$t_{(pd1)}$, $t_{(pd0)}$	$V_{CC} \geq 4.5V$		375	μs
All Other Outputs				
$t_{(pd1)}$, $t_{(pd0)}$	$V_{CC} > 4.5V$		1.0	μs

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI and all other pins pulled up to V_{CC} with 20k resistors.

Note 2: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 3: Voltage change must be less than 0.5V in a 1 ms period.

Note 4: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} (i.e., 0.1 mA at 2.4V V_{CC} and 0.5 mA at 4.5V V_{CC}).

COP444LP Absolute Maximum Ratings

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C
	0.4W at 70°C
Total Source Current	120 mA
Total Sink Current	140 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

COP444LP DC Electrical Characteristics

$0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})	(Note 1)	4.5	5.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current			66	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})	V_{CC} = 5.5V	3.0		V
Logic High (V_{IH})	V_{CC} = 4.5V	2.0		V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	V
IP0–IP7, SI Input Levels				
Logic High	*V_{CC} = 5.5V	2.4		V
Logic High	V_{CC} = 5V ±5%	2.0		V
Logic Low		−0.3	0.8	V
All Other Inputs				
Logic High	High Trip Level Options	3.6		V
Logic Low		−0.3	1.2	V
Input Capacitance			7	pF
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ±5%			
Logic High (V_{OH})	I_{OH} = 25 μA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36 mA		0.4	V
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	*V_{CC} = 4.5V, V_{OL} = 0.4V	0.9		mA
L0–L7 Outputs	*V_{CC} = 4.5V, V_{OL} = 0.4V	0.4		mA
G0–G3 and D0–D3 Outputs	*V_{CC} = 4.5V, V_{OL} = 1.0V	7.5		mA
CKO	*V_{CC} = 4.5V, V_{OL} = 0.4V	0.2		mA
Output Source Current				
D0–D3, G0–G3 Outputs (I_{OH})	*V_{CC} = 4.5V, V_{OH} = 2.0V	−30	−250	μA
SO and SK Outputs (I_{OH})	*V_{CC} = 4.5V, V_{OH} = 1.0V	1.2		mA
L0–L7 Outputs	*V_{CC} = 4.5V, V_{OH} = 2.0V	−1.4	−20	mA
Input Load Source Current (I_{IL})	V_{CC} = 5.0V, V_{IL} = 0V	−10	−140	μA
Total Sink Current Allowed				
All Outputs Combined			140	mA
D, G Ports			120	mA
L7–L4			4	mA
L3–L0			4	mA
All Other Pins			1.8	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L7–L4			60	mA
L3–L0			60	mA
Each L Pin			30	mA
All Other Pins			1.4	mA

COP444LP AC Electrical Characteristics

$0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time		16	40	μs
CKI				
Input Frequency f_I	÷ 32 mode	0.8	2.0	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 2.0 MHz		120	ns
Fall Time			80	ns
Inputs				
SI, IP7–IP0				
t_{SETUP}			2.0	μs
t_{HOLD}			1.0	μs
IN3–IN0, G3–G0, L7–L0				
t_{SETUP}			8.0	μs
t_{HOLD}			1.3	μs
Output Propagation Delay	C_L = 50 pF, V_{OUT} = 1.5V			
SO, SK Outputs	R_L = 20 kΩ		4.0	μs
t_{pd1}, t_{pd0}				
D3–D0, G3–G0, L7–L0	R_L = 20 kΩ		5.6	μs
t_{pd1}, t_{pd0}				
A0–A7			7.5	μs
t_{pd1}, t_{pd0}			11.5	μs
A_8, A_9				
t_{pd1}, t_{pd0}			6.0	μs
A_{10}				
t_{pd1}, t_{pd0}				

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

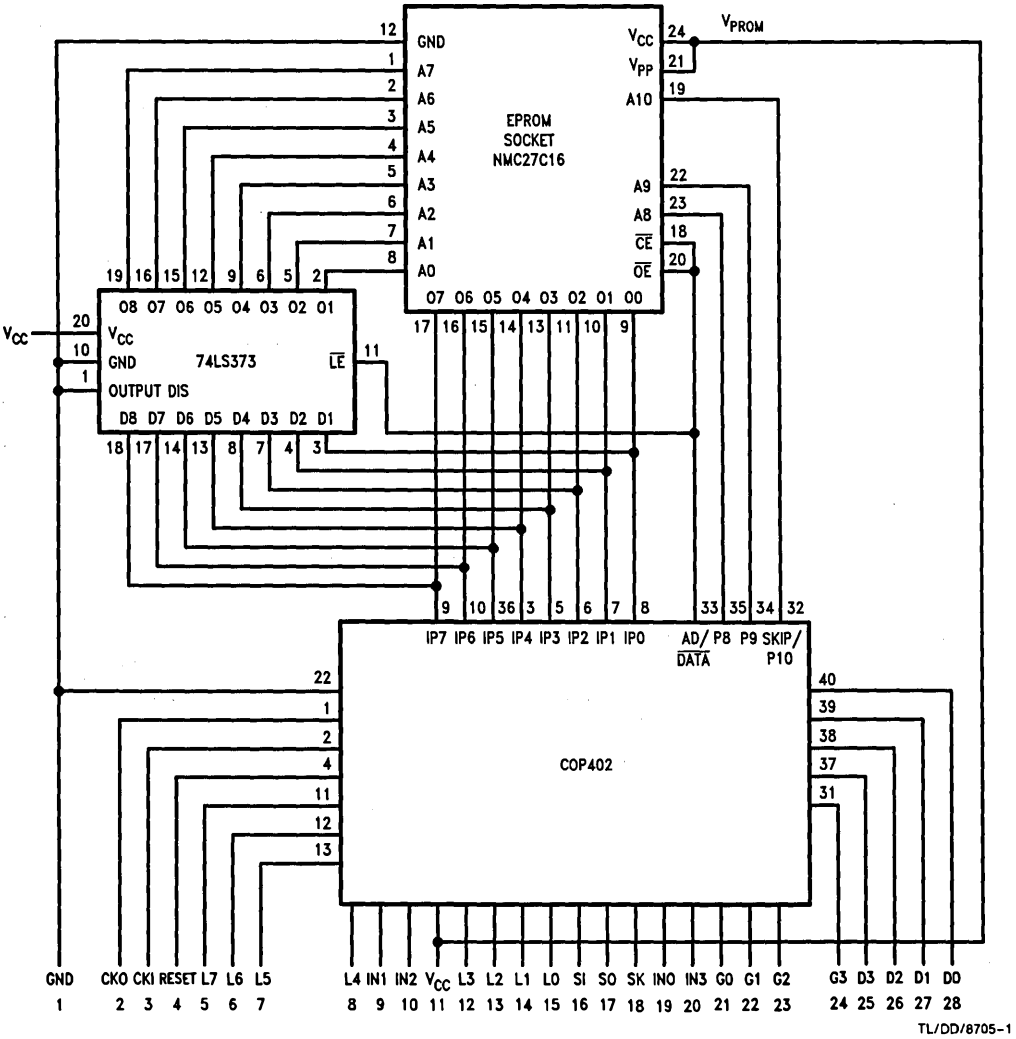


FIGURE 1. COP420P Block Diagram

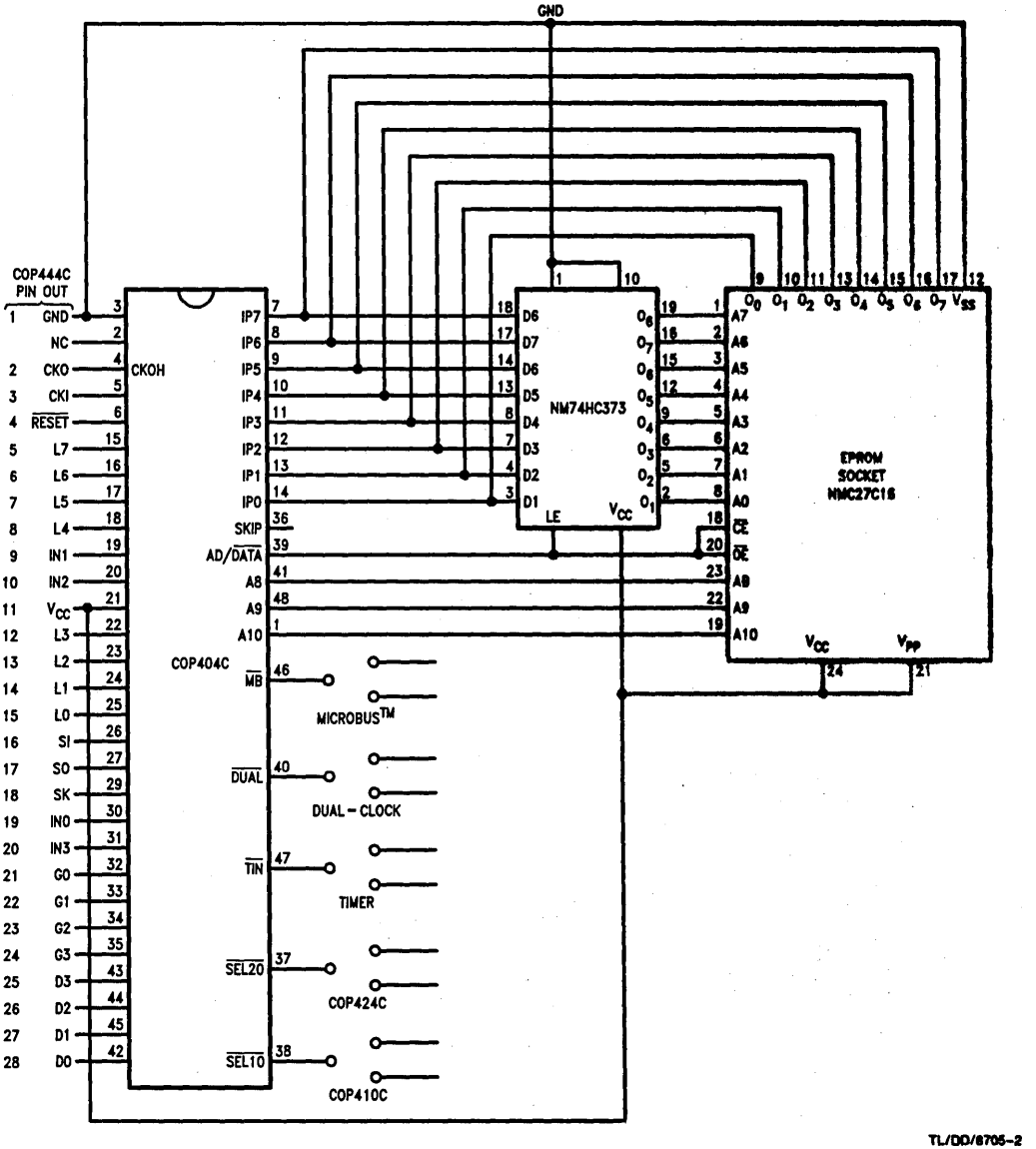


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FIGURE 2. COP444C Block Diagram

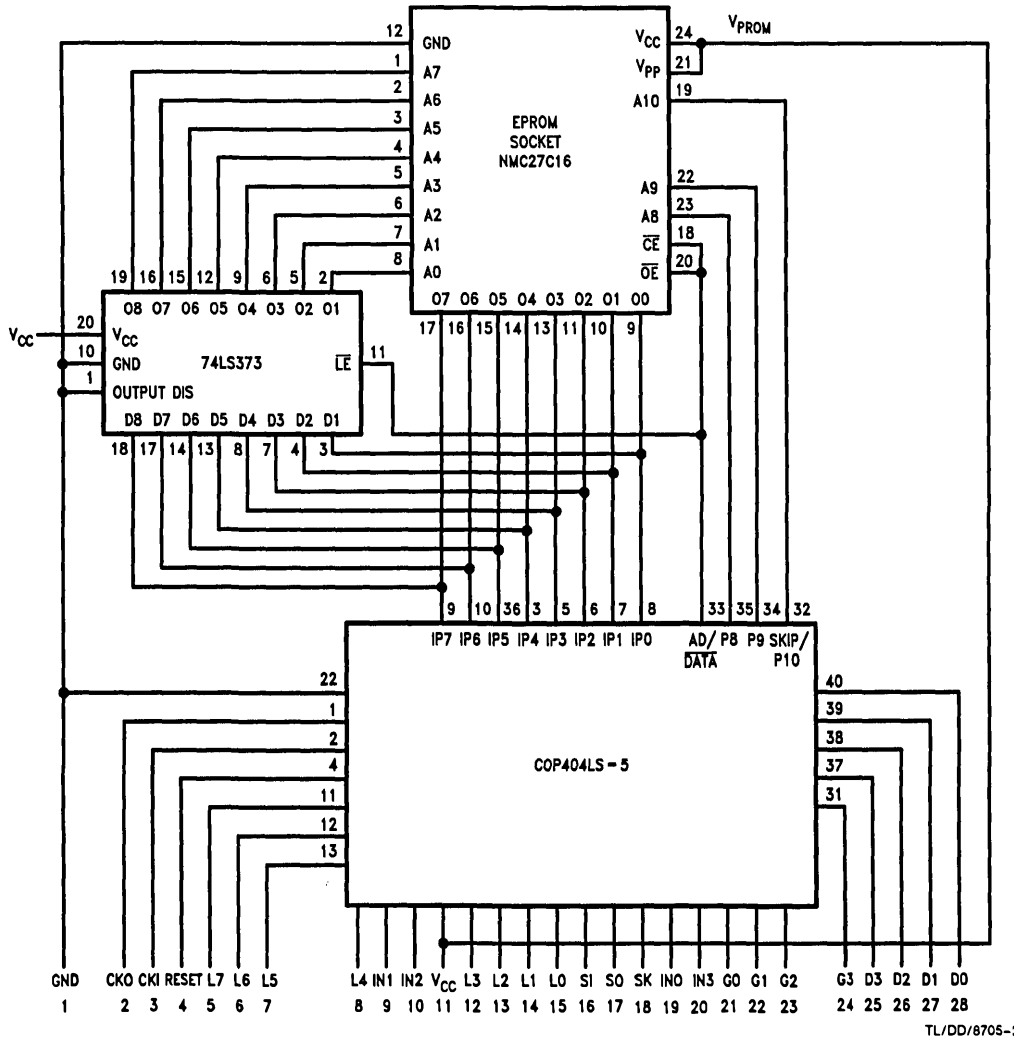
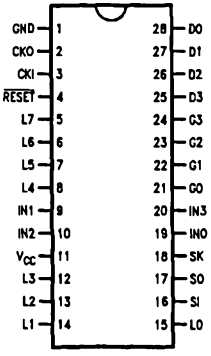


FIGURE 3. COP444LP Block Diagram

Connection Diagrams

COP420P



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24-Pin EPROM Socket

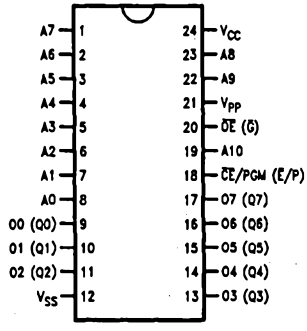

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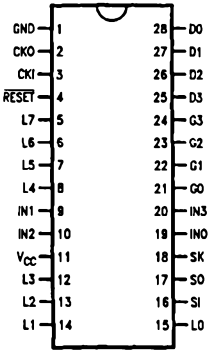
FIGURE 4. COP420P Connection Diagrams

Pin	Description
L_7–L_0	8 Bidirectional I/O Ports with TRI-STATE
G_3–G_0	4 Bidirectional I/O Ports
D_3–D_0	4 General Purpose Outputs
IN_3–IN_0	4 General Purpose Inputs
SI	Serial Input (or Counter Input)
SO	Serial Output (or General Purpose Output)
SK	Logic-Controlled Clock (or General Purpose Output)

Pin	Description
AD/$\overline{DATA}$	Address Out/Data In Flag
CKI	System Oscillator Input
CKO	Clock Generator Output to Crystal/Resonator
$\overline{RESET}$	System Reset Input
V_{CC}	Power Supply
GND	Ground
O_7–O_0	PROM Data Lines
A_9–A_0	PROM Address Outputs

COP444CP



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24 Pin EPROM Socket

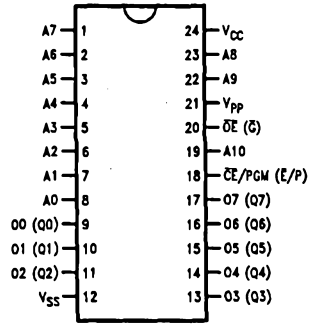

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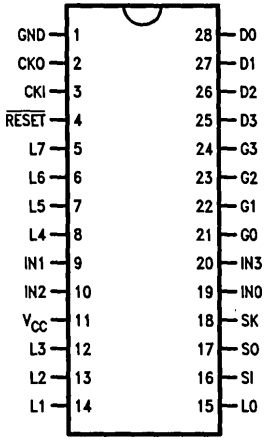
FIGURE 5. COP444CP Connection Diagrams

Pin	Description
L_7–L_0	8 Bidirectional I/O Ports with TRI-STATE
G_3–G_0	4 Bidirectional Very High Current Standard Output
D_3–D_0	4 General Very High Current Standard Output
IN_3–IN_0	4 General Purpose Inputs
SI	Serial Input (or Counter Input)
SO	Serial Output (or General Purpose Output)
SK	Logic-Controlled Clock (or General Purpose Output)

Pin	Description
AD/$\overline{DATA}$	Address Out/Data In Flag
CKI	System Oscillator Input
CKO	Clock Generator Output to Crystal/Resonator
$\overline{RESET}$	System Reset Input
V_{CC}	Power Supply
GND	Ground
O_7–O_0	PROM Data Lines
A_{10}–A_0	PROM Address Outputs

Connection Diagrams (Continued)

COP444LP



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24-Pin EPROM Socket

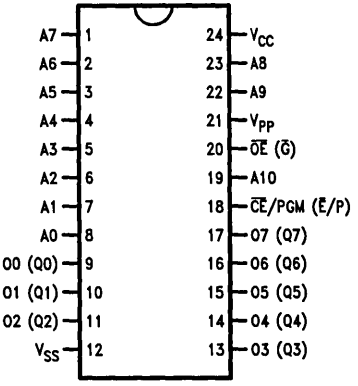

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FIGURE 6. COP444LP Connection Diagrams

Pin	Description
L_7–L_0	8 LED Direct Drive
G_3–G_0	4 Bidirectional Low Current I/O Ports
D_3–D_0	4 General Purpose Outputs
IN_3–IN_0	4 General Purpose Inputs
SI	Serial Input (or Counter Input)
SO	Serial Output (or General Purpose Output)
SK	Logic-Controlled Clock (or General Purpose Output)

Pin	Description
AD/$\overline{DATA}$	Address Out/Data In Flag
CKI	System Oscillator Input
CKO	Clock Generator Output to Crystal/Resonator
$\overline{RESET}$	System Reset Input
V_{CC}	Power Supply
GND	Ground
O_7–O_0	PROM Data Lines
A_{10}–A_0	PROM Address Outputs

COP420 (COP444LP) Mask Options

The following COP420 (COP444L) options have been implemented in the COP420P (COP444LP):

Option Value	Comment
Option 1 = 0	GND pin—no option available
Option 2 = 0	CKO is clock generator output to crystal
Option 3 = 0	CKI is crystal input ÷ 16 (÷ 32 COP444LP)
Option 4 = 0	RESET pin has load device to V_{CC}
Option 5–8 = 2	L outputs have LED direct-drive
Option 9 = 0	IN1 has load device to V_{CC}
Option 10 = 0	IN2 has load device to V_{CC}
Option 11 = 0 (COP420P)	V_{CC} pin—no option available
(Option 11 = 1 COP444LP)	V_{CC} pin—4.5V–5.5V operation
Option 12–15 = 2	L outputs have LED direct-drive
Option 16 = 0	SI has load device to V_{CC}
Option 17 = 2	SO has push-pull output
Option 18 = 2	SK has push-pull output
Option 19 = 0	IN0 has load device to V_{CC}
Option 20 = 0	IN3 has load device to V_{CC}
Option 21–24 = 0	G outputs are standard (COP420P). G outputs have very high current standard output (COP444LP)
Option 25–28 = 0	D outputs are standard (COP420P). D outputs have very high current standard output. (COP444LP)
Option 29 = 0 (COP420P)	Normal operation
(Option 29 = 1 COP444LP)	L has higher voltage input levels
Option 30 = 0 (COP420P)	28-pin package
(Option 30 = 1 COP444LP)	IN has higher voltage input levels
Option 31 = 0 (COP420P)	IN has standard input levels
(Option 31 = 1 COP444LP)	G has higher voltage input levels
Option 32 = 0	G has standard input levels (COP420P). SI has standard input levels (COP444LP)
Option 33 = 0	L has standard input levels (COP420P). RESET has Schmitt trigger input (COP444LP)
Option 34 = 0	No option
Option 35 = 0	SI has standard input levels (COP420P). 28-pin package (COP444LP)

COP444CP Mask Options

The following COP444C options have been implemented in the COP444CP:

Option Value	Comment
Option 1 = 0	GND pin—no option available
Option 2 = 1	CKO is HALT I/O
Option 3 = 5	CKI is external clock input ÷ 4
Option 4 = 1	RESET is Hi-Z input
Option 5–8 = 0	L outputs are standard TRI-STATE
Option 9 = 1	IN1 is a Hi-Z input
Option 10 = 1	IN2 is a Hi-Z input
Option 11 = 0	V_{CC} pin (4.5V–5.5V)
Option 12–15 = 0	L outputs are standard TRI-STATE
Option 16 = 0	SI is a Hi-Z input
Option 17 = 0	SO is a standard output
Option 18 = 0	SK is a standard output
Option 19 = 1	IN0 is a Hi-Z input
Option 20 = 1	IN3 is a Hi-Z input
Option 21–24 = 1	G outputs are low current
Option 25–28 = 0	D outputs are standard
Option 29 = 1	No internal initialization logic
Option 30 = 0	Normal operation
Option 31 = 0	Time-base counter
Option 32 = 0	Normal
Option 33 = 0	28-pin package