National Semiconductor

PRELIMINARY

COP888CLMH
Single-Chip microCMOS Microcontroller

General Description

The COP888CLMH hybrid emulator is a member of the COPS™ microcontroller family. It is functionally identical to the COP888CL except that its package contains an 8k EPROM in place of masked program ROM. This 44-pin part contains a transparent window which allows the EPROM to be erased and re-programmed. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS, with low current drain
- Two power saving modes: HALT and IDLE
- 1 μs instruction cycle time
- 8192 bytes on-board EPROM
- 128 bytes on-board RAM
- Single supply operation: 4.5V–5.5V
- MICROWIRE/PLUS™ serial I/O
- WatchDog and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Ten multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Two Timers each with 2 interrupts
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Versatile instruction set with true bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 44 PCC with 37 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Form fit and function emulation device for the COP888CG
- Real time emulation and full program debug offered by National's Development Systems

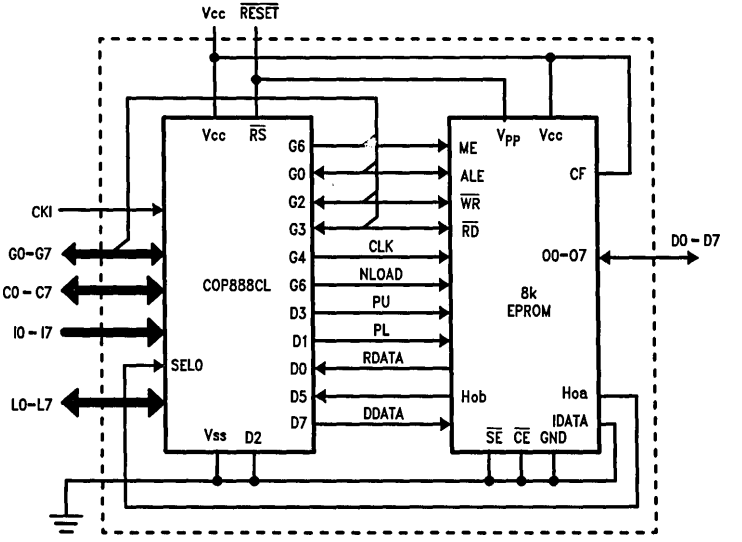

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FIGURE 1. COP888CLMH Block Diagram

General Description (Continued)

The COP888CLMH is a fully static part, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, three 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), full duplex UART, two comparators, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The COP888CLMH operates over a voltage range of 4.5V to 5.5V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagram

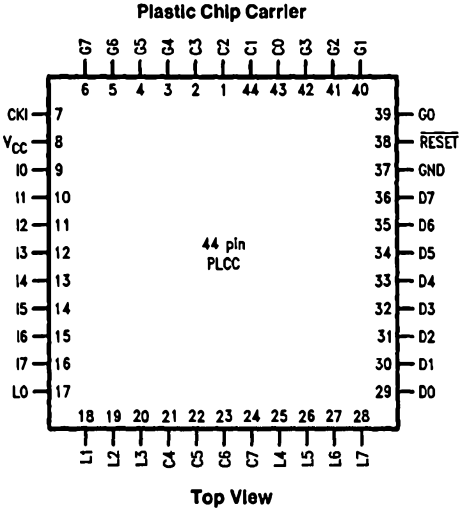

FIGURE 2. COP888CLMH Connection Diagram

COP888CLMH Pinouts

Port	Type	Alt. Fun	Alt. Fun	MUX Mode	44-Pin PCC
L0	I/O	MIWU			17
L1	I/O	MIWU			18
L2	I/O	MIWU			19
L3	I/O	MIWU			20
L4	I/O	MIWU	T2A		25
L5	I/O	MIWU	T2B		26
L6	I/O	MIWU			27
L7	I/O	MIWU			28
G0	I/O	INT		ALE	39
G1	WDOUT				40
G2	I/O	T1B		$\overline{WR}$	41
G3	I/O	T1A		$\overline{RD}$	42
G4	I/O	SO			3
G5	I/O	SK			4
G6	I	SI		ME	5
G7	I/CKO	HALT RESTART			6
D0	O			I/O BIT 0	29
D1	O			I/O BIT 1	30
D2	O			I/O BIT 2	31
D3	O			I/O BIT 3	32
I0	I				9
I1	I				10
I2	I				11
I3	I				12
I4	I				13
I5	I				14
I6	I				15
I7	I				16
D4	O			I/O BIT 4	33
D5	O			I/O BIT 5	34
D6	O			I/O BIT 6	35
D7	O			I/O BIT 7	36
C0	I/O				43
C1	I/O				44
C2	I/O				1
C3	I/O				2
C4	I/O				21
C5	I/O				22
C6	I/O				23
C7	I/O				24
V_{CC}					8
GND					37
CKI					7
$\overline{RESET}$				V_{PP}	38

I/O BITS = Address and Data Lines

MUX MODE = Programming Mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6V
Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V
ESD Susceptibility (Note 5)	2000V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 2)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 3)					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			25	mA
HALT Current (Note 4)	V_{CC} = 5.5V, CKI = 0 MHz		200		μA
IDLE Current					
CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			15	mA
Input Levels					
$\overline{RESET}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5	−2		+2	μA
Input Pullup Current	V_{CC} = 5.5V	40		250	μA
G and L Port Input Hysteresis			0.05 V_{CC}		V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1V	10			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4.5V, V_{OH} = 2.7V	10		100	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
TRI-STATE Leakage	V_{CC} = 4.5V	−2		+2	μA

Note 1: Except pins G6 (ME) and the RESET (V_{PP}) pin during EPROM MUX mode programming at which time the absolute maximum voltage is 14V on these two pins.

Note 2: Rate of voltage change must be less than 0.5 V/ms.

Note 3: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 4: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. The clock monitor is disabled.

Note 5: Human body model, 100 pF through 1500Ω.

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin					
D Outputs (Sink)				15	mA
All Others				3	mA
Maximum Input Current without Latchup (Note 6)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator,		1		DC	μs
R/C Oscillator		3		DC	μs
CKI Clock Duty Cycle (Note 7)	f_r = Max	40		60	%
Rise Time (Note 7)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 7)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}		200			ns
t_{HOLD}		60			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK				0.7	μs
All Others				1	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 6: Except pin G7: −60 mA to +100 mA (sampled but not 100% tested).

Note 7: Parameter sampled but not 100% tested.

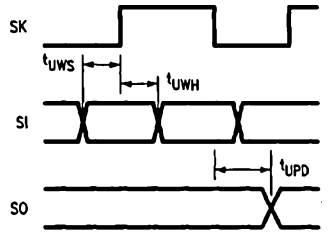

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FIGURE 3. MICROWIRE/PLUS Timing

Pin Descriptions

V_{CC} and GND are the power supply pins.

CKI is the clock input. This can come from an R/C generated oscillator, or a crystal oscillator (in conjunction with CKO). See Oscillator Description section.

$\overline{\text{RESET}}$ is the master reset input. See Reset Description section.

The COP888CLMH contains three bidirectional 8-bit I/O ports (C, G and L), where each individual bit may be independently configured as an input, output or TRI-STATE under program control. Three data memory address locations are allocated for each of these I/O ports. Each I/O port has two associated 8-bit memory mapped registers, the CONFIGURATION register and the output DATA register. A memory mapped address is also reserved for the input pins of each I/O port. (See the COP888CLMH memory map for the various addresses associated with the I/O ports.) *Figure 3* shows the I/O port configurations for the COP888CLMH. The DATA and CONFIGURATION registers allow for each port bit to be individually configured under software control as shown below:

CONFIGURATION Register	DATA Register	Port Set-Up
0	0	Hi-Z Input (TRI-STATE Output)
0	1	Input with Weak Pull-Up
1	0	Push-Pull Zero Output
1	1	Push-Pull One Output

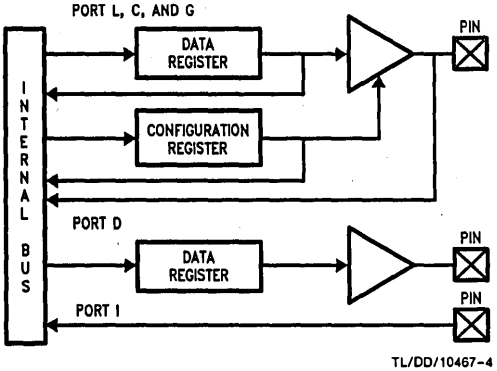

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FIGURE 4. I/O Port Configurations

PORT L is an 8-bit I/O port. All L-pins have Schmitt triggers on the inputs.

The Port L supports Multi-Input Wake Up on all eight pins. L4 and L5 are used for the timer input functions T2A and T2B.

The Port L has the following alternate features:

- L0 MIWU
- L1 MIWU
- L2 MIWU
- L3 MIWU
- L4 MIWU or T2A
- L5 MIWU or T2B
- L6 MIWU
- L7 MIWU

Port G is an 8-bit port with 5 I/O pins (G0, G2–G5), an input pin (G6), and two dedicated output pins (G1 and G7). Pins G0 and G2–G6 all have Schmitt Triggers on their inputs. Pin G1 serves as the dedicated WDOUT WatchDog output, while pin G7 is either input or output depending on the oscillator mask option selected. With the crystal oscillator option selected, G7 serves as the dedicated output pin for the CKO clock output. With the single-pin R/C oscillator mask option selected, G7 serves as a general purpose input pin but is also used to bring the device out of HALT mode with a low to high transition. There are two registers associated with the G Port, a data register and a configuration register. Therefore, each of the 5 I/O bits (G0, G2–G5) can be individually configured under software control.

When programming the COP888CLMH, G0 becomes Address Latch Enable (ALE) and pins G2, G3 and G6 become Write bar ($\overline{\text{WR}}$), Read bar ($\overline{\text{RD}}$) and Mux Enable (ME), respectively.

Since G6 is an input only pin and G7 is the dedicated CKO clock output pin (crystal clock option) or general purpose input (R/C clock option), the associated bits in the data and configuration registers for G6 and G7 are used for special purpose functions as outlined below. Reading the G6 and G7 data bits will return zeros.

Note that the chip will be placed in the HALT mode by writing a "1" to bit 7 of the Port G Data Register. Similarly the chip will be placed in the IDLE mode by writing a "1" to bit 6 of the Port G Data Register.

Writing a "1" to bit 6 of the Port G Configuration Register enables the MICROWIRE/PLUS to operate with the alternate phase of the SK clock. The G7 configuration bit, if set high, enables the clock start up delay after HALT when the R/C clock configuration is used.

	Config Reg.	Data Reg.
G7	CLKDLY	HALT
G6	Alternate SK	IDLE

Port G has the following alternate features:

- G0 INTR (External Interrupt Input)
- G2 T1B (Timer T1 Capture Input)
- G3 T1A (Timer T1 I/O)
- G4 SO (MICROWIRE Serial Data Output)
- G5 SK (MICROWIRE Serial Clock)
- G6 SI (MICROWIRE Serial Data Input)

Port G has the following dedicated functions:

- G1 WDOUT WatchDog and/or Clock Monitor dedicated output
- G7 CKO Oscillator dedicated output or general purpose input

Pin Descriptions (Continued)

When programming the COP888CLMH, G0 becomes Address Latch Enable (ALE) and pins G2, G3 and G6 become Write ($\overline{WR}$), Read ($\overline{RD}$) and Mux Enable (ME), respectively.

Port I is an eight-bit input port. The 28- and 40-pin devices do not have a full complement of Port I pins. The unavailable pins are not terminated i.e., they are floating. A read operation for these unterminated pins will return unpredictable values. The user must ensure that the software takes this into account by either masking or restricting the accesses to bit operations. The unterminated Port I pins will draw power only when addressed.

Port I1–I3 are used for Comparator 1. Port I4–I6 are used for Comparator 2.

The Port I has the following alternate features.

- I1 COMP1 −IN (Comparator 1 Negative Input)
- I2 COMP1 +IN (Comparator 1 Positive Input)
- I3 COMP1OUT (Comparator 1 Output)
- I4 COMP2 −IN (Comparator 2 Negative Input)
- I5 COMP2 +IN (Comparator 2 Positive Input)
- I6 COMP2OUT (Comparator 2 Output)

Port D is an 8-bit output port that is preset high when $\overline{RESET}$ goes low. The user can tie two or more D port outputs together in order to get a higher drive.

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Figure 5 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table I shows the component values required for various standard crystal values.

R/C OSCILLATOR

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart input.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.

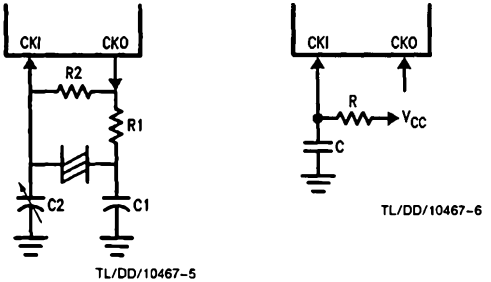


FIGURE 5. Crystal and R/C Oscillator Diagrams

TABLE I. Crystal Oscillator Configuration, T_A = 25°C, V_{CC} = 5V

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)
0	1	30	30–36	10
0	1	30	30–36	4
0	1	200	100–150	0.455

TABLE II. RC Oscillator Configuration, T_A = 25°C, V_{CC} = 5V

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)
3.3	82	2.8 to 2.2	3.6 to 4.5
5.6	100	1.5 to 1.1	6.7 to 9
6.8	100	1.1 to 0.8	9 to 12.5

Programming the COP888CLMH

The COP888CLMH is a hybrid part consisting of a COP888CG die and an 8k EPROM die with port re-creation logic. In order to access the EPROM, the COP888CG die has been placed in ROMless mode by holding its D2 pad at GND. The other D-lines of the COP888CG die are used to communicate with the EPROM. All 8 D-lines are recreated internally and appear on the pins of the COP888CLMH as normal D outputs.

When programming the COP888CLMH, a multiplexed method (MUX MODE) is used. To enter this mode a voltage of 12.2V–13V is applied to pin ME (pin G6). The 8 D-Port pins on the COP888CLMH become address bits with a low to high transition on ALE (pin G0), and data bits with a high to low transition on $\overline{WR}$ (pin G2). With a low to high transition on $\overline{RD}$ (pin G3), the data being programmed is verified. On the 28-pin part, address and data bits 4 to 7 are accessed via L4 to L7. The following steps must be followed in order to place the part in programming mode:

1. Apply V_{CC} = 5V.
2. Ground the RESET and CKI pins. This puts the COP outputs in TRI-STATE mode.
3. Apply V_{PP} = 12.2V–13V to pin G6. This places the EPROM in MUX mode. The current requirement is 450 μA maximum (V_{IN} = 13V, V_{CC} = 5.0V, −40°C).
4. Apply 12.2V–13V to the RESET pin. This supplies V_{PP} to the EPROM which requires 30 mA maximum during WRITE pulses. It is permissible for V_{PP} to drop to V_{CC} during the READ pulses as is done on some programmers.
5. Begin programming each EPROM byte interactively. (See *Figures 6* and *7*). The interactive programming algorithm programs a byte with a 0.5 ms pulse, and then does a verify to determine if that byte was fully programmed. If it was not, the program pulse is repeated and verified again. This is done up to a maximum of 20 times, but most bytes will program with a single pulse.

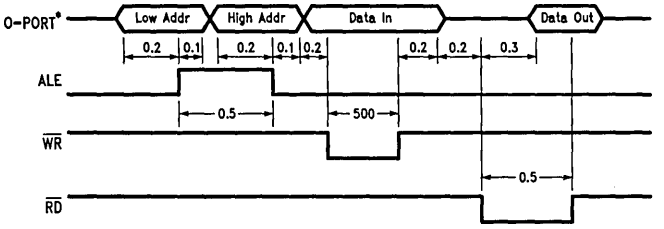
Programming the COP888CLMH (Continued)

Erasure of program memory is achieved by removing the part from its socket and exposing the transparent window to an ultra-violet light source.

Note: The last byte of program memory (EPROM location 01FFF HEX) must contain one of two values: 07F HEX for the HALT enabled mode, or 0FF HEX for the HALT disabled mode. The COP888CGLH will not function properly if any other value resides in this last byte location.

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

The maximum absolute allowable voltage which may be applied to the G6 (ME) and RESET (V_{PP}) pins during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V limit. At least a 0.1 μF capacitor is required across V_{PP} to GND and V_{CC} to GND to suppress spurious voltage transients which may damage the device.



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Note: All minimum times are in μs.

* O-Port = D0 to D7

FIGURE 6. COP888CLMH MUX Mode Programming Timing Diagram

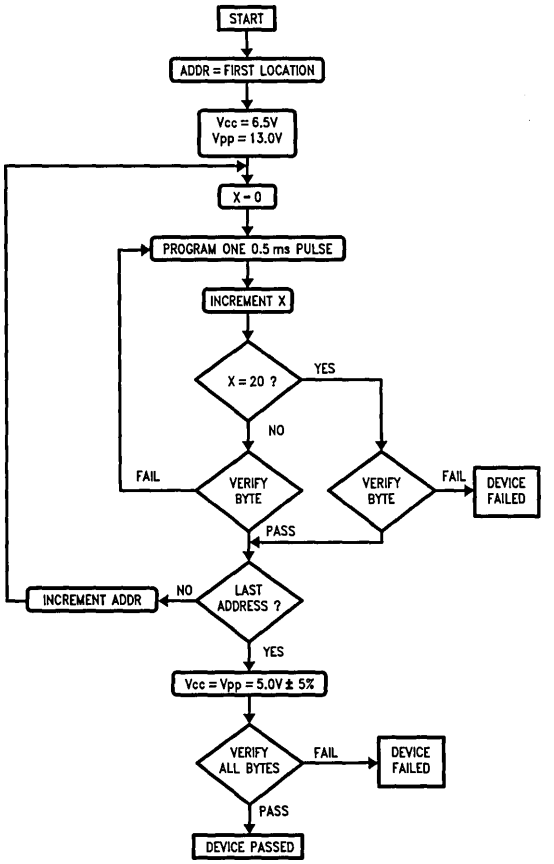

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FIGURE 7. COP888CLMH MUX Mode Programming Flow Chart

Development Support

MOLE DEVELOPMENT SYSTEM

The MOLE (Microcomputer On Line Emulator) is a low cost development system and emulator for all microcontroller products. These include COPs microcontrollers and the HPC family of products. The MOLE consists of a BRAIN Board, Personality Board and optional host software.

The purpose of the MOLE is to provide the user with a tool to write and assemble code, emulate code for the target microcontroller and assist in both software and hardware debugging of the system.

It is a self contained computer with its own firmware which provides for all system operation, emulation control, communication, PROM programming and diagnostic operations.

It contains three serial ports to optionally connect to a terminal, a host system, a printer or a modem, or to connect to other MOLEs in a multi-MOLE environment.

MOLE can be used in either a stand alone mode or in conjunction with a selected host system using PC-DOS communicating via a RS-232 port.

How to Order

To order a complete development package, select the section for the microcontroller to be developed and order the parts listed.

Development Tools Selection Table

Microcontroller	Order Part Number	Description	Includes	Manual Number
COP888	MOLE-BRAIN	Brain Board	Brain Board Users Manual	420408188-001
	MOLE-COP8-PB2	Personality Board	COP888 Personality Board Users Manual	420420084-001
	MOLE-COP8-IBM	Assembler Software for IBM	COP800 Software Users Manual and Software Disk PC-DOS Communications Software Users Manual	424410527-001 420040416-001
	420411060-001	Programmer's Manual		420411060-01

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system and additionally, provides the capability of remotely accessing the MOLE development system at a customer site.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

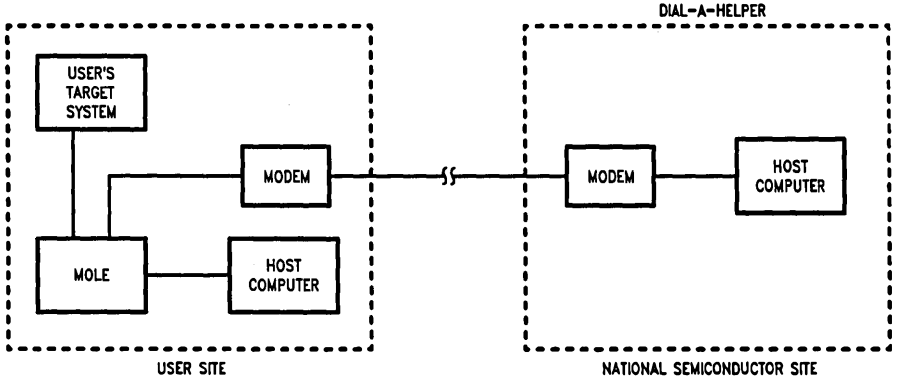
ORDER P/N: MOLE-DIAL-A-HLP

Information System Package contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user is having difficulty in operating a MOLE, he can leave messages on our electronic bulletin board, which we will respond to, or under extraordinary circumstances he can arrange for us to actually take control of his system via modem for debugging purposes.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 Baud
Set-up: Length: 8-Bit
Parity: None
Stop Bit: 1
Operation: 24 Hrs., 7 Days



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