

CS5124, CS5126

High Performance, Integrated Current Mode PWM Controllers

The CS5124/6 is a fixed frequency current mode controller designed specifically for DC-DC converters found in the telecommunications industry. The CS5124/6 integrates many commonly required current mode power supply features and allows the power supply designer to realize substantial cost and board space savings. The product matrix is as follows:

CS5124: 400 kHz w/ V_{BIAS} Pin, 195 mV first current sense threshold.

CS5126: 200 kHz w/ $SYNC$ Pin, 335 mV first current sense threshold.

The CS5124/6 integrates the following features: Internal Oscillator, Slope Compensation, Sleep On/Off, Undervoltage Lock Out, Thermal Shutdown, Soft Start Timer, Low Voltage Current Sense for Resistive Sensing, Second Current Threshold for Pulse by Pulse Over Current Protection, a Direct Optocoupler Interface and Leading Edge Current Blanking.

The CS5124/6 has supply range of 7.7 V to 20 V and is available in 8 pin SO narrow package.

Features

- Line UVLO Monitoring
- Low Current Sense Voltage for Resistive Current Sensing
- External Synchronization to Higher or Lower Frequency Oscillator (CS5126 Only)
- Bias for Start Up Circuitry (CS5124 Only)
- Thermal Shutdown
- Sleep On/Off Pin
- Soft Start Timer
- Leading Edge Blanking
- Direct Optocoupler Interface
- 90 ns Propagation Delay
- 35 ns Driver Rise and Fall Times
- Sleep Mode



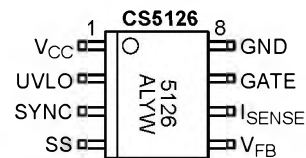
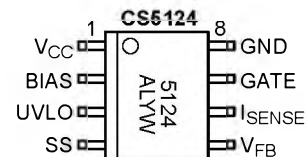
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**SO-8
D SUFFIX
CASE 751**

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5124XD8	SO-8	95 Units/Rail
CS5124XDR8	SO-8	2500 Tape & Reel
CS5126XD8	SO-8	95 Units/Rail
CS5126XDR8	SO-8	2500 Tape & Reel

CS5124, CS5126

ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$, $7.60\text{ V} \leq V_{CC} \leq 20\text{ V}$, $UVLO = 3.0\text{ V}$, $I_{SENSE} = 0\text{ V}$, $C_{V(CC)} = 0.33\ \mu\text{F}$, $C_{GATE} = 1.0\text{ nF}$ (ESR = $10\ \Omega$); $C_{SS} = 470\text{ pF}$; $C_{V(FB)} = 100\text{ pF}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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General

I_{CC} Operating – V_{GATE} not switching	–	–	10	13	mA
I_{CC} at V_{CC} Low	$V_{CC} = 6.0\text{ V}$	–	500	750	μA
I_{CC} Sleep	$V_{UVL} = 1.0\text{ V}$	–	210	275	μA

Low V_{CC} Lockout

V_{CC} Turn-on Threshold Voltage	–	7.2	7.7	8.3	V
V_{CC} Turn-off Threshold Voltage	–	6.8	7.3	7.8	V
V_{CC} Hysteresis	–	350	425	500	mV

UVLO

Sleep Threshold Voltage	UVLO decreasing	1.5	1.8	2.3	V
Sleep Threshold Voltage	UVLO increasing	–	1.88	2.45	V
Sleep Hysteresis	–	35	85	150	mV
UVLO Turn-off Threshold Voltage	Note 2	2.3	2.45	2.6	V
UVLO Turn-on Threshold Voltage	Note 2	2.50	2.63	2.76	V
UVLO Hysteresis	Turn-on – Turn-off ($-40^{\circ}\text{C} \leq T_J \leq 100^{\circ}\text{C}$) Note 2	170	185	200	mV
UVLO Hysteresis	Turn-on – Turn-off ($100^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$) Note 2	50	185	400	mV
UVLO Input Bias Current	–	–1.0	–	1.0	μA
UVLO Clamp	With UVLO sinking 1.0 mA	5.0	7.5	12	V

V_{CC} Clamp and BIAS Pin

CS5124 Only. Connect an NFET as follows: BIAS = G, $V_{CC} = S$, $V_{IN} = D$.

V_{CC} Clamp Voltage	$36\text{ V} \leq V_{IN} \leq 60\text{ V}$, $200\text{ nF} \leq C_{SS} \leq 500\text{ nF}$, $R = 500\text{ k}$	7.275	7.9	8.625	V
BIAS Minimum Voltage	Measure Voltage on BIAS with: $10\text{ V} \leq V_{CC} \leq 20\text{ V}$ & $50\ \mu\text{A} \leq I_{BIAS} \leq 1.0\text{ mA}$	1.6	2.8	4.0	V
BIAS Clamp	With BIAS pin sinking 1.0 mA	12	15	20	V

200 kHz Oscillator

CS5126 Only

Operating Frequency	–	175	200	225	kHz
Max Duty Cycle Clamp	–	78	82.5	85	%
Slope Compensation (Normal operation)	–	12	18	23	mV/ μs
Slope Compensation (Synchronized operation)	Note 2	7.0	12	16	mV/ μs
SYNC Input Threshold Voltage	–	1.0	2.0	3.0	V
SYNC Input Impedance	Measured with SYNC = 1.0 V & 10 V	50	120	230	k Ω

400 kHz Oscillator

CS5124 Only

Operating Frequency	–	360	400	440	kHz
Max Duty Cycle Clamp	–	80.0	82.5	85.0	%
Slope Compensation	–	15	21	26	mV/ μs

2. Not tested in production. Specification is guaranteed by design.

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ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$, $7.60\text{ V} \leq V_{CC} \leq 20\text{ V}$, $UVLO = 3.0\text{ V}$, $I_{SENSE} = 0\text{ V}$, $C_{V(CC)} = 0.33\ \mu\text{F}$, $C_{GATE} = 1.0\text{ nF}$ (ESR = $10\ \Omega$); $C_{SS} = 470\text{ pF}$; $C_{V(FB)} = 100\text{ pF}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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Soft Start

Soft Start Charge Current	–	7.0	10	13	μA
Soft Start Discharge Current	–	0.5	10.0	–	mA
V_{SS} Voltage when V_{FB} Begins to Rise	$V_{FB} = 300\text{ mV}$	1.40	1.62	1.80	V
Peak Soft Start Charge Voltage	–	4.7	4.9	–	V
Valley Soft Start Discharge Voltage	–	200	275	400	mV

Current Sense

CS5124 Only

First Current Sense Threshold	At max duty cycle	170	195	215	mV
Second Current Sense Threshold	–	250	275	315	mV
I_{SENSE} to GATE Prop. Delay	0 to 700 mV pulse into I_{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 400 mV pulse into I_{SENSE}	90	130	180	ns
Internal Offset	Note 3	–	60	–	mV

Current Sense

CS5126 Only

First Current Sense Threshold	At max duty cycle	300	335	360	mV
Second Current Sense Threshold	–	485	525	575	mV
I_{SENSE} to GATE Prop. Delay	0 to 800 mV pulse into I_{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 550 mV pulse into I_{SENSE}	110	175	210	ns
Internal Offset	Note 3	–	125	–	mV

Voltage Feedback

V_{FB} Pull-up Res.	–	2.9	4.3	8.1	$\text{k}\Omega$
V_{FB} Clamp Voltage	CS5124 Only	2.63	2.90	3.15	V
V_{FB} Clamp Voltage	CS5126 Only	2.40	2.65	290	V
V_{FB} Fault Voltage Threshold	–	460	490	520	mV

Output Gate Drive

Maximum Sleep Pull-down Voltage	$V_{CC} = 6.0\text{ V}$, $I_{OUT} = 1.0\text{ mA}$	–	1.2	2.0	V
GATE High (AC)	Series resistance < $1.0\ \Omega$, Note 3	$V_{CC} - 1.0$	$V_{CC} - 0.5$	–	V
GATE Low (AC)	Series resistance < $1.0\ \Omega$, Note 3	–	0.0	0.5	V
GATE High Clamp Voltage	$V_{CC} = 20\text{ V}$	11.0	13.5	16.0	V
Rise Time	Measure GATE rise time, $1.0\text{ V} < \text{GATE} < 9.0\text{ V}$ $V_{CC} = 12\text{ V}$	–	45	65	ns
Fall Time	Measure GATE fall time, $9.0\text{ V} > \text{GATE} > 1.0\text{ V}$ $V_{CC} = 12\text{ V}$	–	25	55	ns

Thermal Shutdown

Thermal Shutdown Temperature	Note 3 GATE low	135	150	165	$^{\circ}\text{C}$
Thermal Enable Temperature	Note 3 GATE switching	100	125	150	$^{\circ}\text{C}$
Thermal Hysteresis	Note 3	15	25	35	$^{\circ}\text{C}$

3. Not tested in production. Specification is guaranteed by design.

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PACKAGE THERMAL DATA

Parameter		SO-8	Unit
R _{θJC}	Typical	45	°C/W
R _{θJA}	Typical	165	°C/W