CS8183

Dual Micropower 200 mA Low Dropout Tracking Regulator/Line Driver

The CS8183 is a dual low dropout tracking regulator designed to provide adjustable buffered output voltages that closely track (±10 mV) the reference inputs. The outputs deliver up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The outputs have been designed to operate over a wide range (2.8 V to 45 V) while still maintaining excellent DC characteristics. The CS8183 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and –50 V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The V_{REF}/ENABLE leads serve two purposes. They are used to provide the input voltage as a reference for the output and they also can be pulled low to place the device in sleep mode where it nominally draws less than 30 μA from the supply.

Features

- Two Regulated Outputs 200 mA, ±10 mV Track Worst Case
- Low Dropout (0.35 V typ. @ 200 mA)
- Low Quiescent Current
- Independent Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in the SO–20L Package

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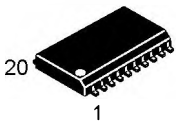
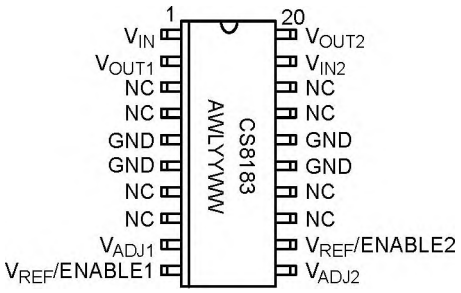


SO–20L
DWF
SUFFIX
CASE 751D

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS8183YDWF20	SO–20L	37 Units/Rail
CS8183YDWFR20	SO–20L	1000 Tape & Reel

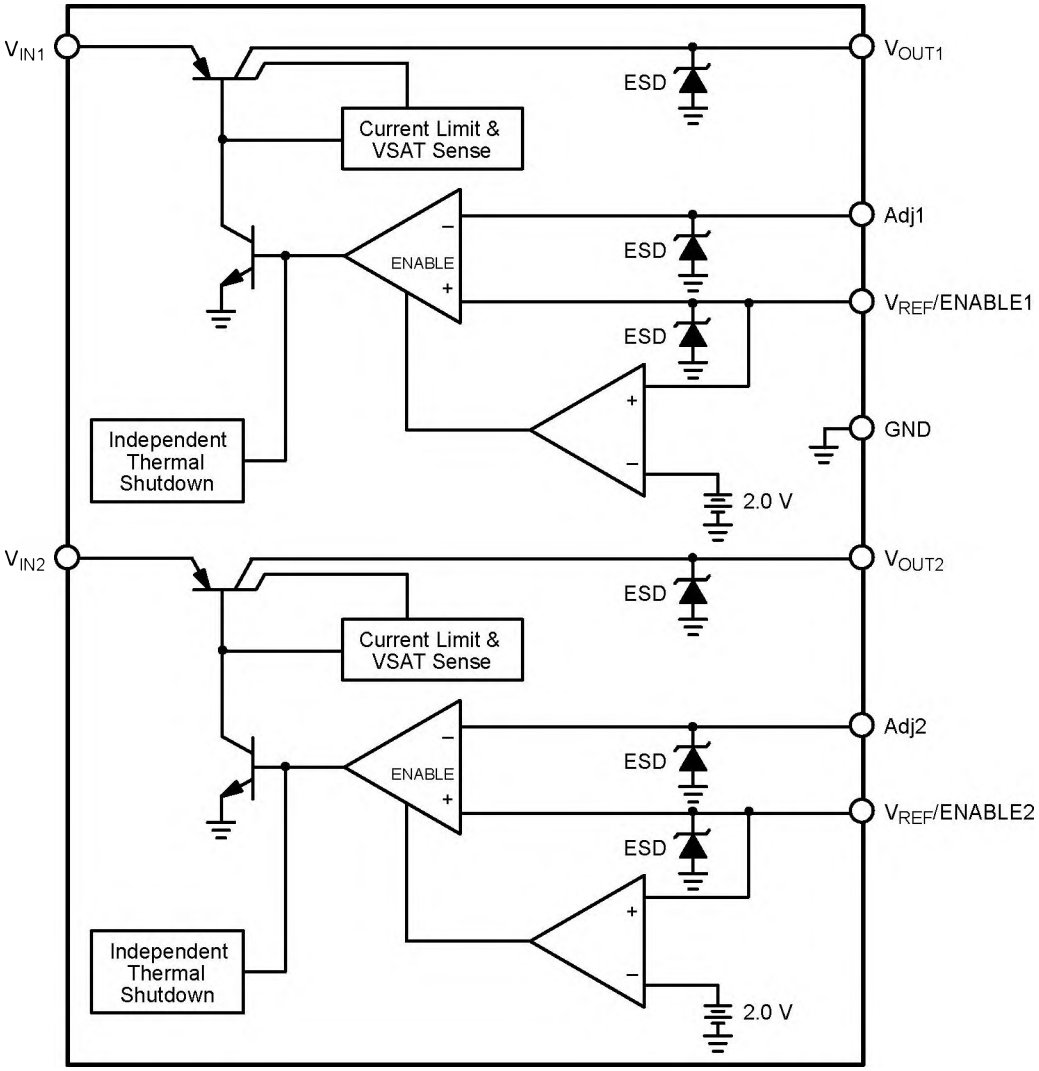


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
Storage Temperature	–65 to 150	°C
Supply Voltage Range (continuous)	15 to 45	V
Supply Voltage Range (normal, continuous)	3.4 to 45	V
Peak Transient Voltage (V_{IN} = 14 V, Load Dump Transient = 31 V)	45	V
Voltage Range (Adj, V_{REF}/ENABLE, V_{OUT})	–10 to 45	V
Maximum Junction Temperature	150	°C
Package Thermal Resistance: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$	 18 73	 °C/W °C/W
ESD Capability (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V; V_{REF}/ENABLE > 2.75 V; –40°C ≤ T_J ≤ +125°C; C_{OUT} ≥ 10 μF; 0.1 Ω < $C_{OUT\ -\ ESR}$ < 1.0 Ω @ 10 kHz; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Regular Output 1, 2					
V_{REF} – V_{OUT} V_{OUT} Tracking Error	4.5 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{OUT} ≤ 200 mA, Note 2	–10	–	10	mV
Dropout Voltage (V_{IN} – V_{OUT})	I_{OUT} = 100 μA I_{OUT} = 200 mA	– –	100 350	150 600	mV mV
Line Regulation	4.5 V ≤ V_{IN} ≤ 26 V, Note 2	–	–	10	mV
Load Regulation	100 μA ≤ I_{OUT} ≤ 200 mA, Note 2	–	–	10	mV
Adj Lead Current	Loop in Regulation	–	0.2	1.0	μA
Current Limit	V_{IN} = 14 V, V_{REF} = 5.0 V, V_{OUT} = 90% of V_{REF}, Note 2	225	–	700	mA
Quiescent Current (I_{IN} – I_{OUT})	V_{IN} = 12 V, I_{OUT} = 200 mA V_{IN} = 12 V, I_{OUT} = 100 μA V_{IN} = 12 V, V_{REF}/ENABLE = 0 V	– – –	15 75 30	25 150 55	mA μA μA
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	–	0.2	1.5	mA
Ripple Rejection	f = 120 Hz, IOUT = 200 mA, 4.5 V ≤ V_{IN} ≤ 26 V	60	–	–	dB
Thermal Shutdown	–	150	180	210	°C
V_{REF}/ENABLE 1, 2					
Enable Voltage	–	0.80	2.00	2.75	V
Input Bias Current	V_{REF}/ENABLE 1, 2 > 2.0 V	–	0.2	1.0	μA

2. V_{OUT} connected to Adj lead.

PACKAGE PIN DESCRIPTION

Package Lead Number SO–20L	Lead Symbol	Function
1	V_{IN1}	Input voltage for V_{OUT1}.
2	V_{OUT1}	Regulated output voltage 1.
3, 4, 7, 8, 13, 14, 17, 18	NC	No connection.
5, 6, 15, 16	GND	Ground (4 leads fused)
9	V_{ADJ1}	Adjust lead for V_{OUT1}.
10	V_{REF}/ENABLE1	Reference voltage and ENABLE input for V_{OUT1}.
11	V_{ADJ2}	Adjust lead for V_{OUT2}.
12	V_{REF}/ENABLE2	Reference voltage and ENABLE input for V_{OUT2}.
19	V_{IN2}	Input voltage for V_{OUT2}.
20	V_{OUT2}	Regulated output voltage 2.

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the V_{REF}/ENABLE 1, 2 lead below 2.0 V typically, (see Figure 5 or Figure 6), the IC is disabled and enters a sleep state where the device draws less than 30 μA from supply. When the V_{REF}/ENABLE lead is greater than 2.75 V, V_{OUT} tracks the V_{REF}/ENABLE lead normally.

Output Voltage

Figures 2 through 7 only display one channel of the device for simplicity. The configurations shown apply for both channels.

The outputs are capable of supplying 200 mA to the load while configured as a similiar (Figure 2), lower (Figure 4), or higher (Figure 3) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non–inverting.

The device can also be configured as a high–side driver as displayed in Figure 7.

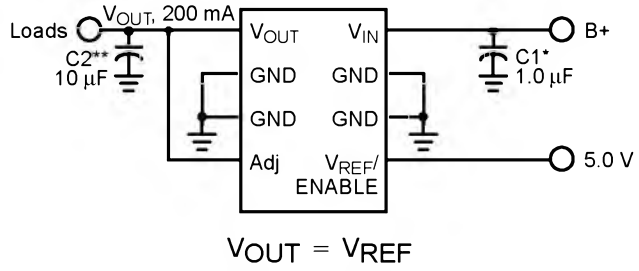


Figure 2. Tracking Regulator at the Same Voltage

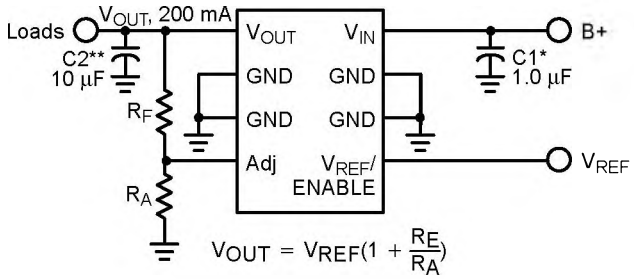


Figure 3. Tracking Regulator at Higher Voltages

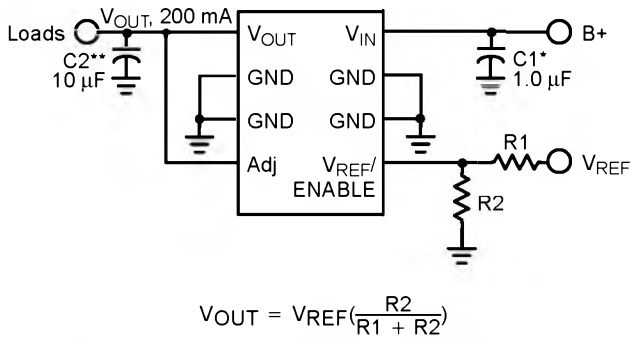


Figure 4. Tracking Regulator at Lower Voltages

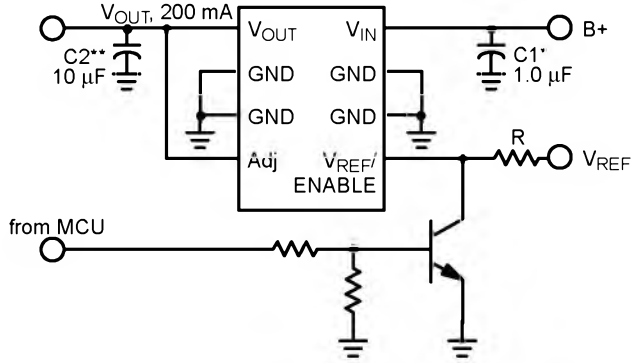


Figure 5. Tracking Regulator with ENABLE Circuit

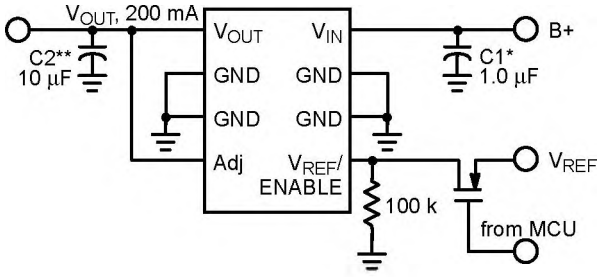


Figure 6. Alternative ENABLE Circuit

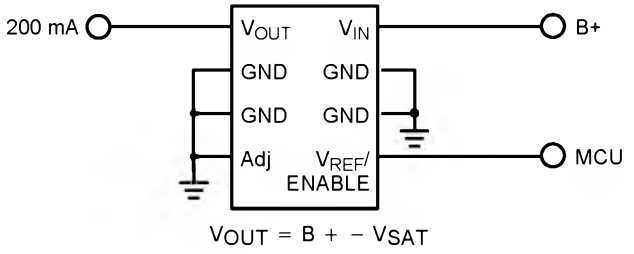


Figure 7. High–Side Driver

* C_1 is required if the regulator is far from the power source filter.
** C_2 is required for stability.

APPLICATION NOTES

Switched Application

The CS8183 has been designed for use in systems where the reference voltage on the V_{REF}/ENABLE pin is continuously on. Typically, the current into the V_{REF}/ENABLE pin will be less than 1.0 μA when the voltage on the V_{IN} pin (usually the ignition line) has been switched out (V_{IN} can be at high impedance or at ground.) Reference Figure 8.

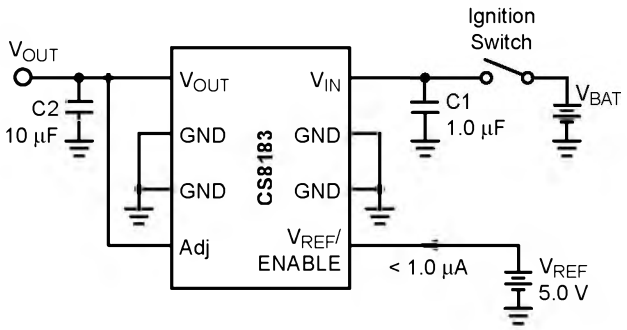


Figure 8.

External Capacitors

Output capacitors for the CS8183 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst–case is determined at the minimum ambient temperature and maximum load expected.

The output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to –40°C, a capacitor rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators."

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 9) is:

$$PD(max) = \{V_{IN}(max) - V_{OUT1}(min)\} I_{OUT1}(max) + \{V_{IN}(max) - V_{OUT2}(min)\} I_{OUT2}(max2) + V_{IN}(max) I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from V_{OUT1},

$V_{OUT2(min)}$ is the minimum output voltage from V_{OUT2},

$I_{OUT1(max)}$ is the maximum output current, for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application,

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of PD(max) is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

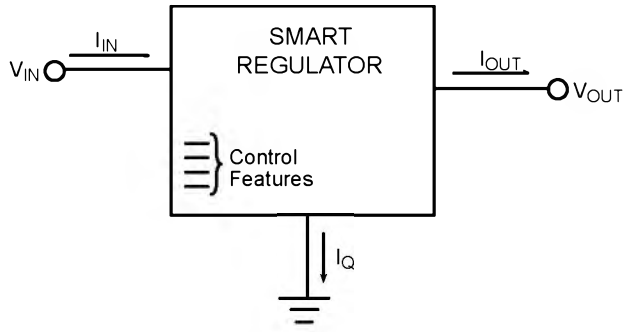


Figure 9. Dual Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.