SONY

CXA1390AQ/AR

S/H and AGC for CCD Camera

Description

The CXA1390AQ/AR are CCD camera's signal processing ICs which extract signals from the CCD output. These bipolar ICs perform correlated double sampling. AGC, color separation, high luminance detection and others. Additionary, these ICs are not affected by irregular pulses which occure during the CCD shutter mode.

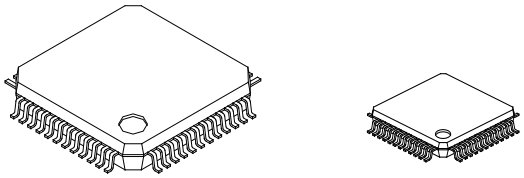
Featuers

- Pin compatible upgraded version of CXA1390Q/R which can be swapped out while using same peripheral chips
- Almost completely corrects irregular pulses and their negative affects
- Correlated double sampling function alllows for the suppression of low band noise in the CCD output
- AGC amplifier, which has High S/N ratio and wide gain control range, enhances the camera sensitivity
- Output for iris adjustment. High luminance detection output
- Usage of Vg (regulator) output allows for the formation of IRIS and AGC LOOP which are not affected by supply voltage functation

Operating Conditions

Supply voltage	V_{CC}	4.75 to 5.25	V

CXA1390AQ	CXA1390AR
48 pin QFP (Plastic)	48 pin LQFP (Plastic)



Application

S/H and AGC for CCD camera

Structure

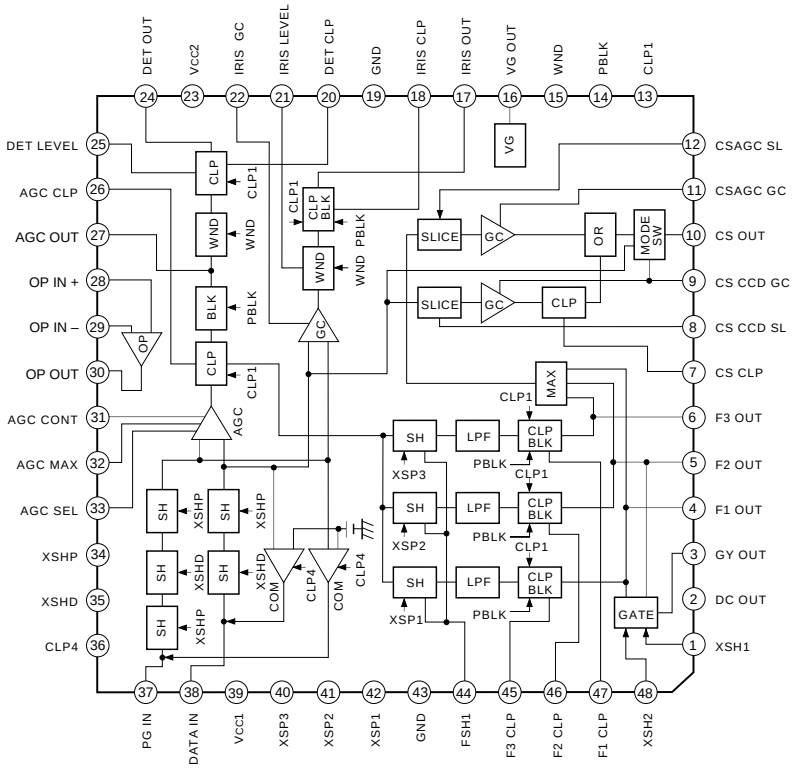
Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	600 (QFP)	mW
		950 (VQFP) *	mW

* (40mm × 40mm, t = 0.8mm with a mounted glass epoxy substrate)

Block Diagram and Pin Configuration (Top View)



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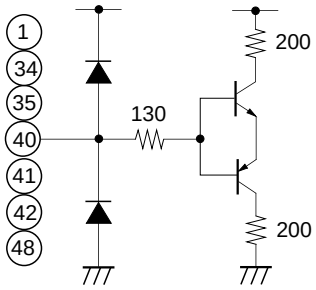
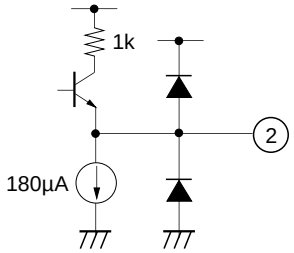
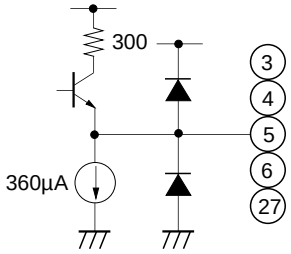
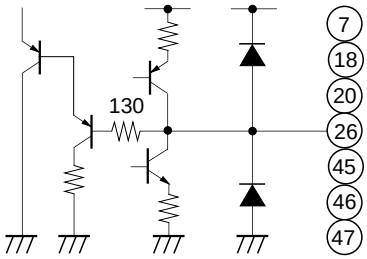
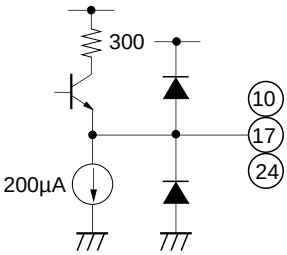
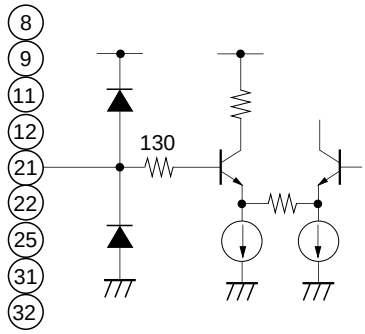
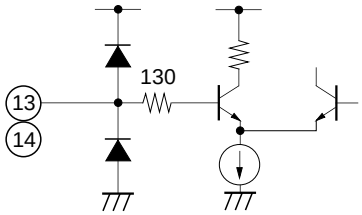
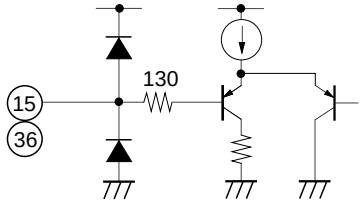
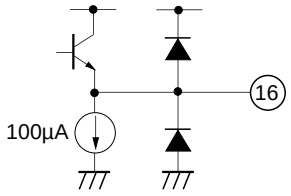
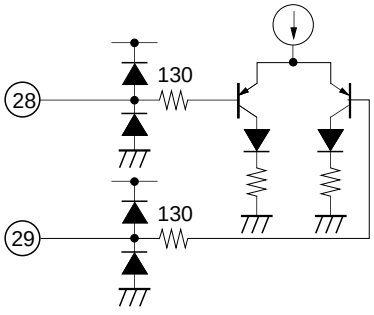
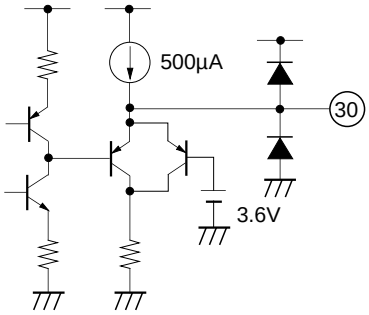
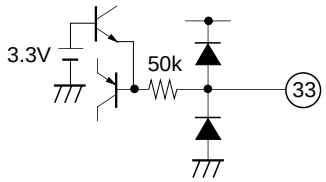
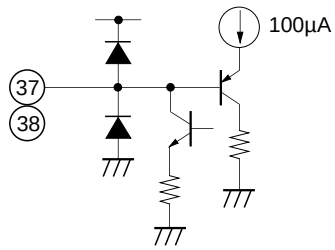
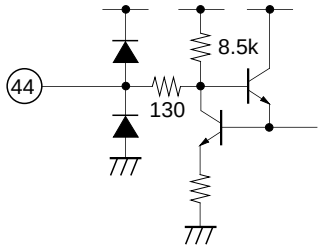
E90941A78

Pin Description and Standard Pin voltage (V_{CC} = 5V)

PIn No.	Symbol	Voltage	Equivalent circuit	Description
1	XSH1	H: 4V and above L: 1V and below		High speed pulse input pin for S/H (active at L)
34	XSHP			
35	XSHD			
40	XSP3			
41	XSP2			
42	XSP1			
48	XSH2			
2	DC OUT	1.8 to 2.1V		DC output pin of f_1 to f_3 output black level
3	GY OUT	Black level 1.8 to 2.1V		Signal output pin
4	F1 OUT			
5	F2 OUT			
6	F3 OUT			
27	AGC OUT			
7	CS CLP	2.6 to 3.3V		Capacitor connecting pin for clamp
18	IRIS CLP	2.0 to 2.6V		
20	DET CLP	1.9 to 2.6V		
26	AGC CLP	2.3 to 2.8V		
45	F3 CLP	2.0 to 2.6V		
46	F2 CLP	2.0 to 2.6V		
47	F1 CLP	2.0 to 2.6V		
10	CS OUT	1.7 to 2.2V		Signal output pin
17	IRIS OUT	1.7 to 2.0V		Signal output pin Vcc fluctuations effect is minor on DC level
24	DET OUT	1.7 to 2.0V		

PIn No.	Symbol	Voltage	Equivalent circuit	Description
8	CS CCD SL	(Test mode at 0V)		Level adjustment pin of high luminance detection pin of the input signal
9	CS CCD GC			Gain adjustment pin of input signal high luminance part
11	CSAGC GC			Gain adjustment pin of high luminance port after AGC
12	CSAGC SL			Level adjustment pin of high luminance detection after AGC
21	IRIS LEVEL			Adjustment pin of IRIS output weighting (Active at WND = L)
22	IRIS GC			Gain adjustment pin of IRIS output
25	DET LEVEL			Adjustment pin of DET output weighting (Active at WND = L)
31	AGC CONT			AGC amplifier gain adjustment pin
32	AGC MAX			AGC amplifier MAX gain adjustment pin
13	CLP1	H: 4V and above L: 1V and below		CLP1 pulse input pin Active at H (OPB clamp)
14	P BLK			Pre BLK pulse input pin Active at L
15	WND			Window pulse input pin Active at L
36	CLP4			CLP4 pulse input pin Active at H
16	VG OUT	2.6 to 3.1V		Regulator output pin (Used for the formation of AGC and IRIS loop)
28	OP IN +	1 to 3.3V		Operation amplifier non inverted input pin
29	OP IN –			Operation amplifier inverted input pin

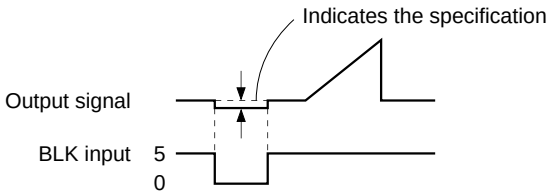
PIn No.	Symbol	Voltage	Equivalent circuit	Description
30	OP OUT	H: 4.2V and above L: 1.2V and below		Output pin
33	AGC SEL	V_{CC}: Low Gain mode GND: High Gain mode		AGC amplifier gain selection pin
37 38	PG IN DATA IN	Black level 2.7 to 3.2V		CCD signal input pin
44	FSHI	1.4 to 1.8V		Adjustment pin for color separation S/H follow up speed (Normally used OPEN)

Electrical Characteristics (Ta = 25°C, V_{CC} = 5.0V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		ID		32	48	65	mA
AGC	CONT Min.	ACON Min.	AGC OUT/DATA IN AGC CONT = 1.5V AGC MAX = 5V AGC SEL = 0V		6	8	dB
	CONT Max.	ACON Max.	AGC OUT/DATA IN AGC CONT = 4.5V AGC MAX = 5V AGC SEL = 0V	30	32		dB
	Max. Min.	MAX Min.	AGC OUT/DATA IN AGC CONT = 4.5V AGC MAX = 1.5V AGC SEL = 0V		17	20	dB
	Gain shift	GSHI	AGC OUT (SEL = 5V) /AGC OUT (SEL = 0V)	–5	–4	–3	dB
	BLK offset	ΔBLK	Note 1)	–10	0	+10	mV
Color separation	Gain	f Gain	Color separation output/AGC OUT (f_1, f_2, f_3)	–0.5	0	+0.5	dB
	BLK offset	f ΔBLK	Note 1)	–10	0	+10	mV
DC OUT		DC		1.8	1.95	2.1	V
Gate Gain		GY	GY OUT/AGC OUT	–0.5	0	+0.5	dB
IRIS	Gain Cont Max.	IR Max.	IRIS OUT/DATA IN IRIS GC = 5V WND = 5V	18	22		dB
	Gain Cont Min.	IR Min.	IRIS OUT/DATA IN IRIS GC = 1.5V WND = 5V		4	8	dB
	Window Level Max.	IRW Max.	Gain Cont Max. ratio (attenuation) IRIS GC = 1.5V IRIS LEVEL = 5V WND = 0V	–1	0		dB
	Window Level Min.	IRW Min.	Gain Cont Max. ratio (attenuation) IRIS GC = 1.5V IRIS LEVEL = 1.5V WND = 0V			–14	dB
DET	Gain	DET G	DET OUT/AGC OUT WND = 5V	–2	–1	+0.5	dB
	Window Level Max.	DET Max.	DET OUT/AGC OUT DET LEVEL = 5V WND = 0V	–2	–1	+0.5	dB
	Window Level Min.	DET Min.	Level Max. ratio DET LEVEL = 1.5V WND = 0V			–13	dB

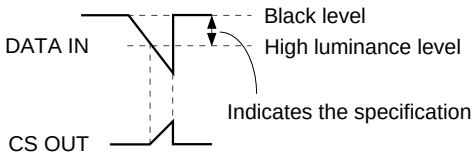
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
CS CCD	Max. Gain	CSC Max.	CSOUT differential/ DATA IN differential CS CCD SL = 4.1V CS CCD GC = 5V PBLK = 0V	13	16		dB
	Min. Gain	CSC Min.	CSOUT differential/ DATA IN differential CS CCD SL = 4.1V CS CCD GC = 1.5V PBLK = 0V		–1	1	dB
	Max. SLICE	CSC Max. SL	Input conversion slice level CS CCD SL = 1.5V Note 1)	0.7			V
	Min. SLICE	CSC Min. SL	Input conversion slice level CS CCD SL = 5V Note 1)		40	100	mV
CS AGC	Max. Gain	CSA Max.	CS OUT DATA IN = 0.2Vpp CS AGC GC = 5V CS AGC SL = 4.2V CS CCD GC = 1.5V CS CCD SL = 1.5V Note 2)	0.5			Vpp
	Min. Gain	CSA Min.	CS OUT differential/ AGC OUTdifferential CS AGC GC = 1.5V CS AGC SL = 4.2V CS CCD GC = 1.5V CS CCD SL = 1.5V Note 2)		–1	1	dB
	Max. SLICE	CSA Max. SL	AGC OUT conversion CS AGC SL = 1.5V Note 3)	1.2			V
	Min. SLICE	CSA Min. SL	AGC OUT conversion CS AGC SL = 5V Note 3)		0.06	0.1	V
TEST mode		TEST	DATA IN = 0.5Vpp CS CCD GC = 0V Note 4)		0.5		Vpp
OP-Amp	H level	OPH	OP IN + = 2.1V OP IN – = 2.0V	4.2			V
	L level	OPL	OP IN + = 2.0V OP IN – = 2.1V		0.9	1.2	V
Vg OUT		Vg	At no load	2.6	2.85	3.1	V

Note 1)



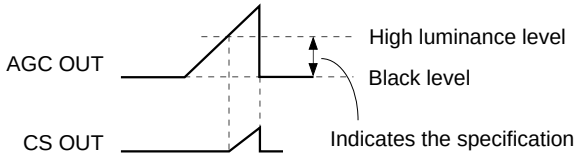
Note 2)

Voltage between DATA IN input black level and the high luminance level determined by CS CCD SL pin voltage.



Note 3)

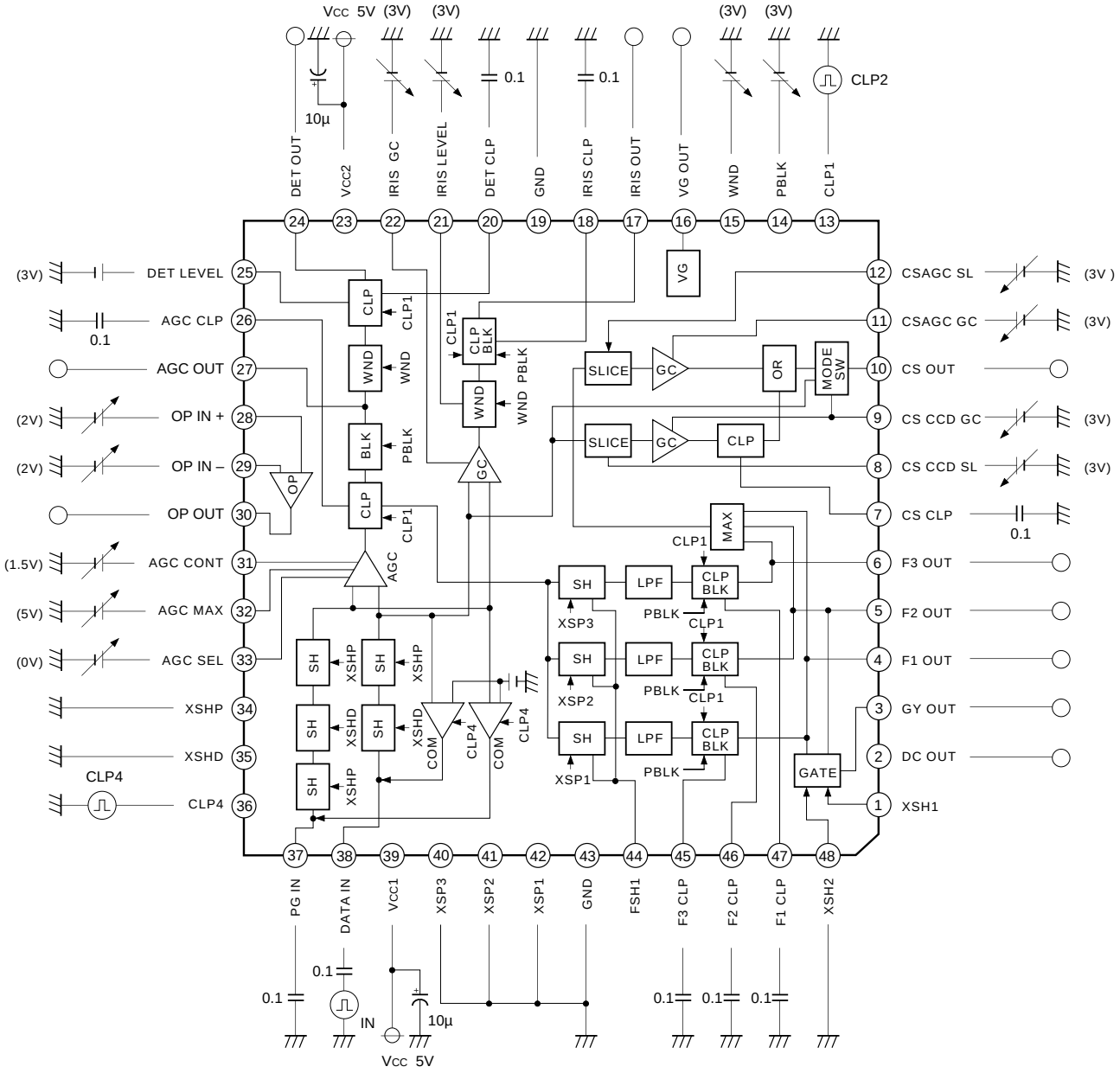
Voltage between the black level at AGC OUT and the high luminance level determined by CS AGC SL pin voltage.



Note 4)

S/H output DATA IN input can be monitored by turning CS CCD GC (Pin 9) to 0V.

Test Circuit

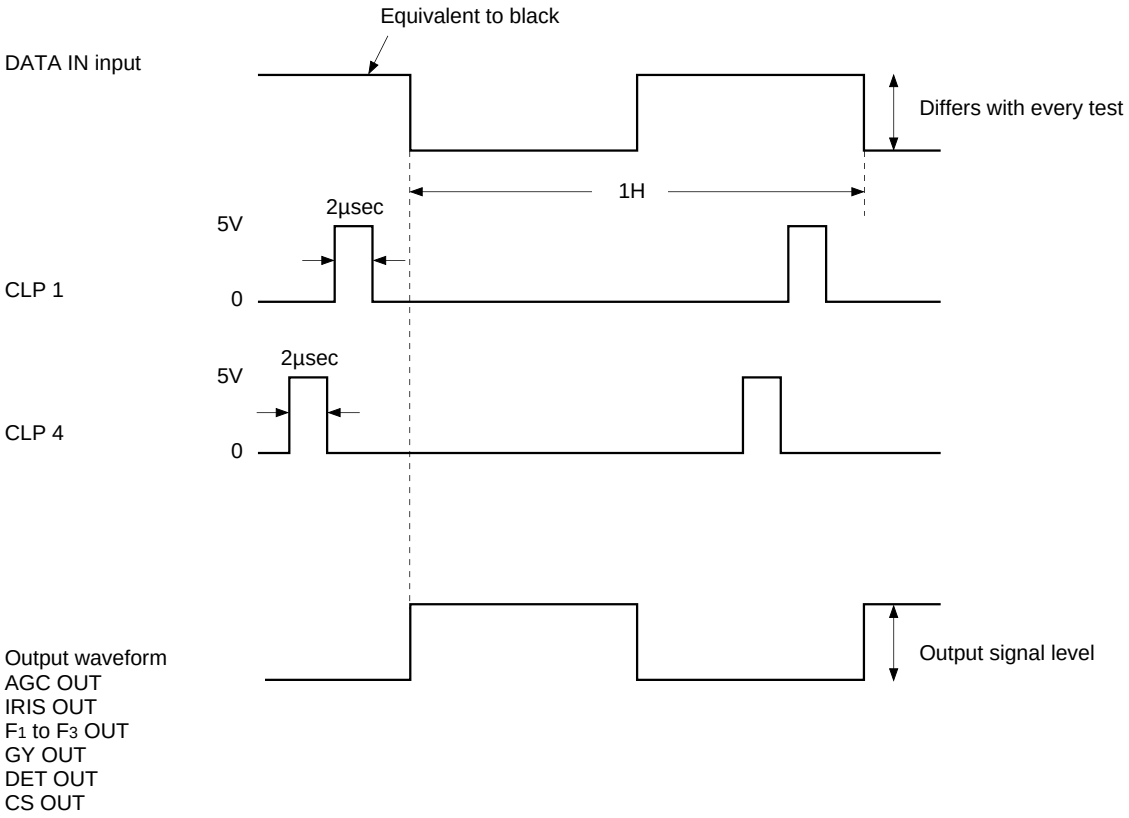


Note 1) Capacitor unit value at µF.

Note 2) Voltage in parentheses are those not specified in the Electrical Characteristics Test Conditions.

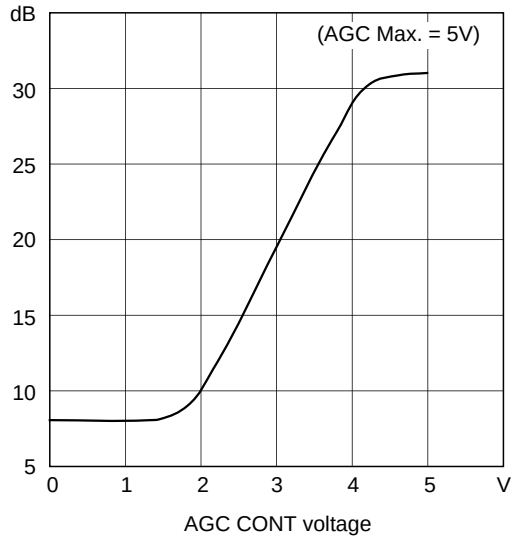
Note 3) —○ indicates a test pin. (For both AC and DC)

Timing Diagram for Testing

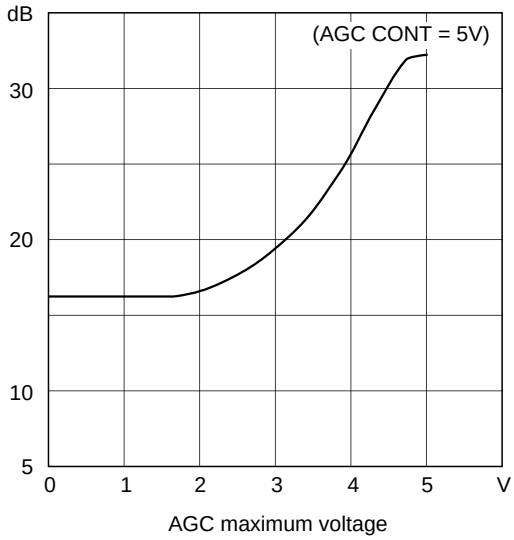


Standard Control Characteristics (V_{CC} = 5V, Ta = 25°C)

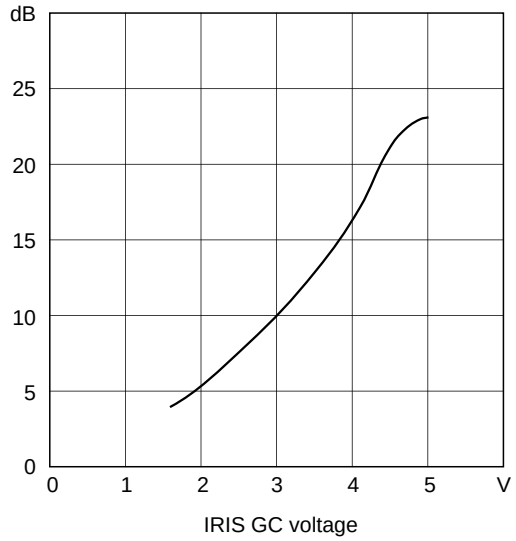
AGC amplifier gain control characteristics



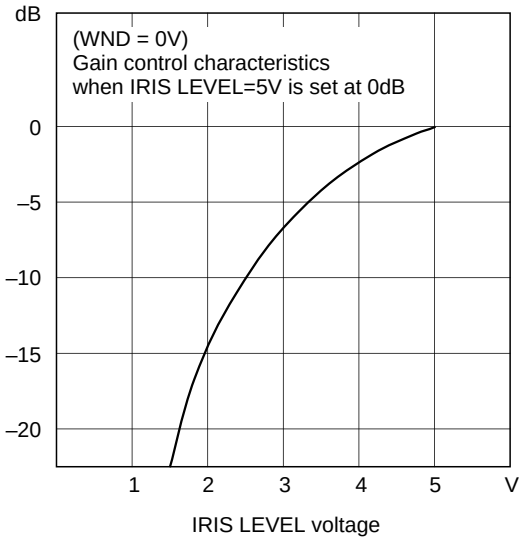
AGC maximum control characteristics



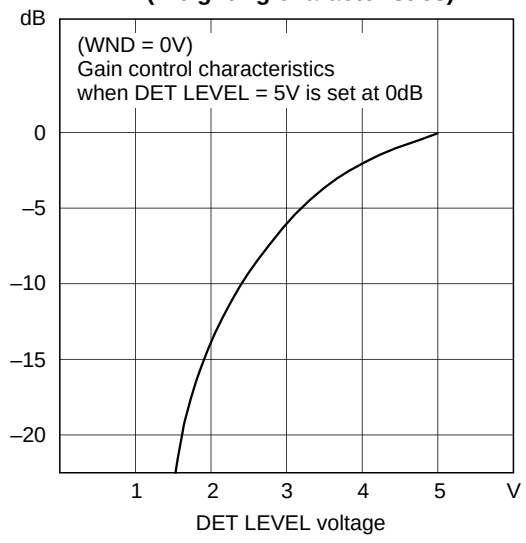
IRIS gain control characteristics



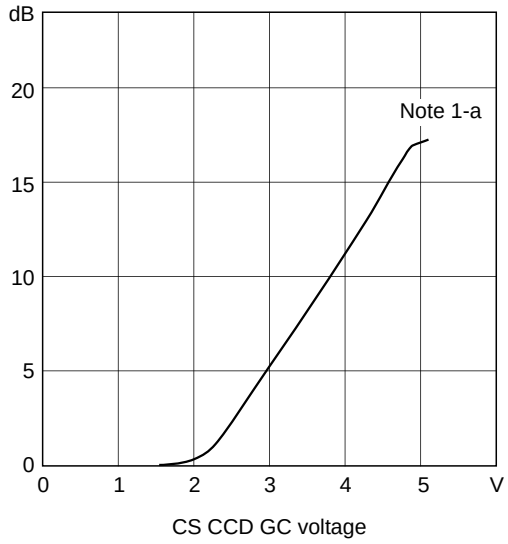
IRIS WINDOW control characteristics (Weighting characteristics)



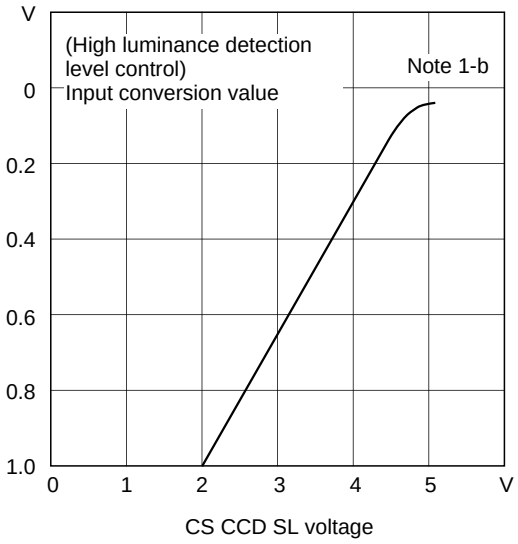
DET WINDOW control characteristics (Weighting characteristics)



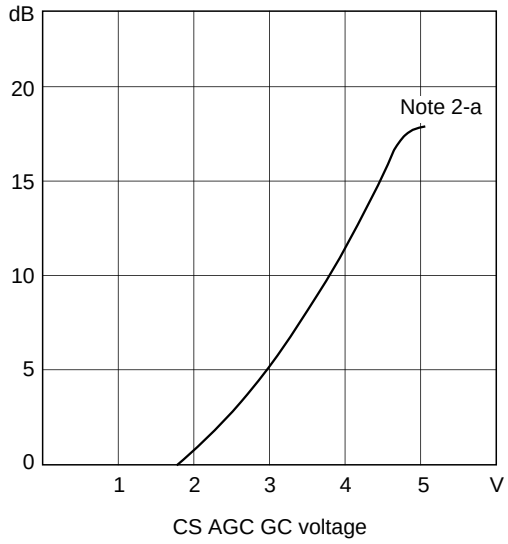
CS CCD gain control characteristics



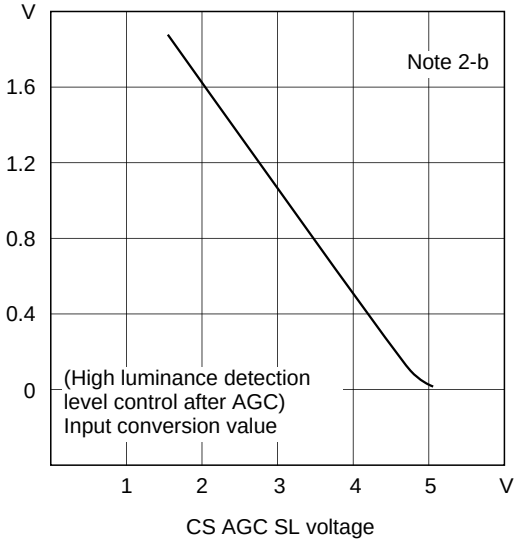
CS CCD slice control characteristics



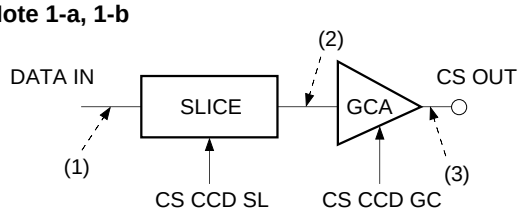
CS AGC gain control characteristics

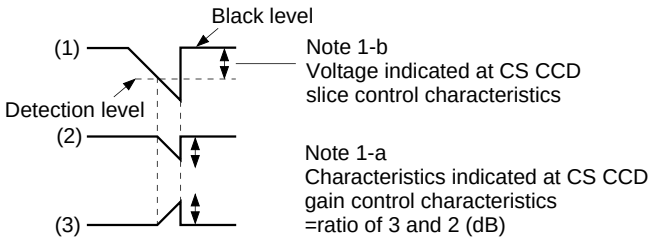


CS AGC slice control characteristics

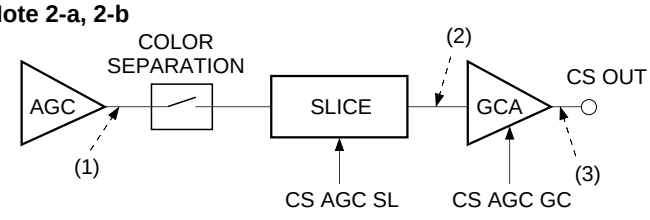


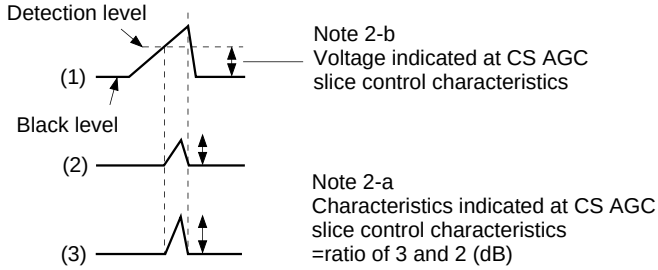
Note 1-a, 1-b





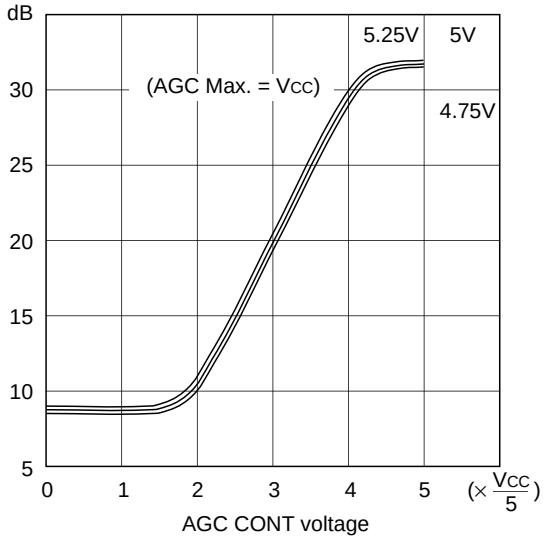
Note 2-a, 2-b



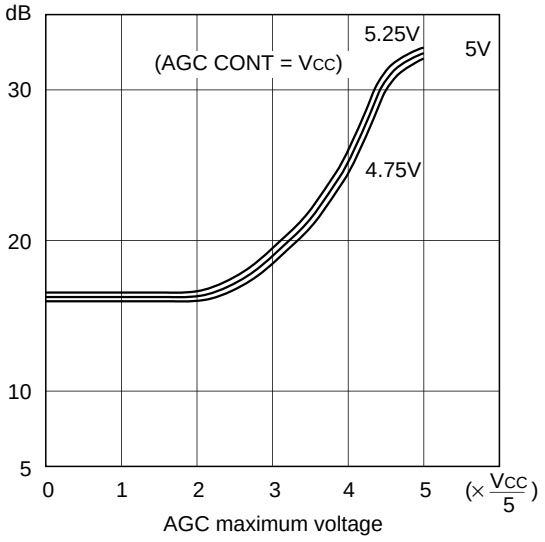


Supply voltage Characteristics Standard Design Documentation (Ta = 25°C)

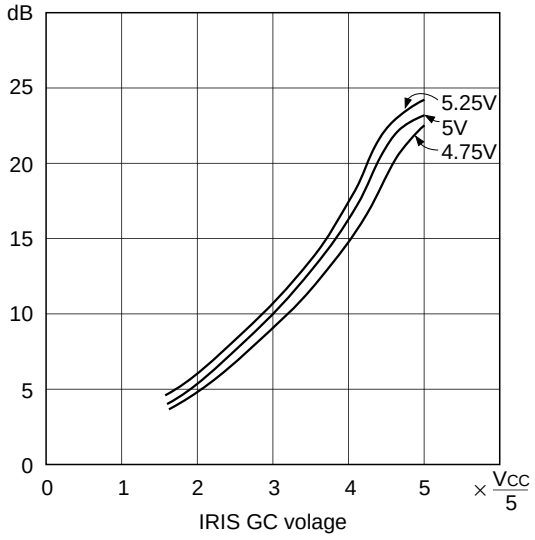
AGC amplifier gain control characteristics



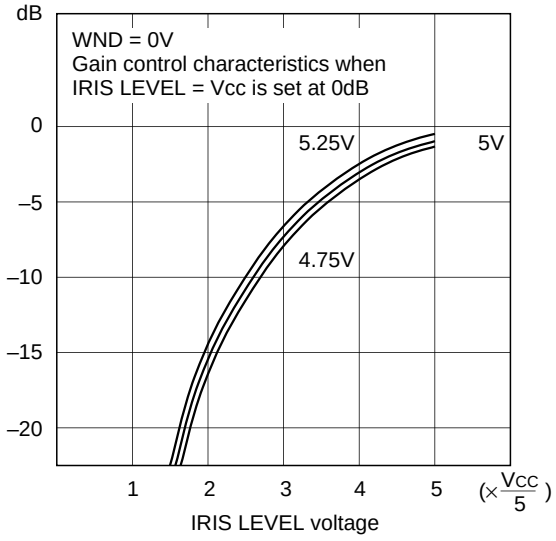
AGC maximum control characteristics



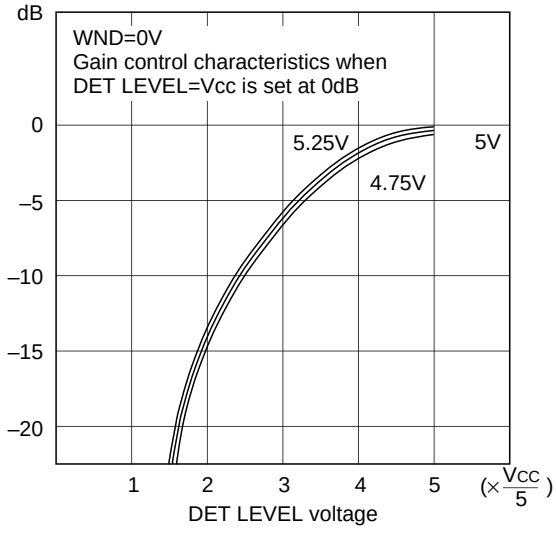
IRIS gain control characteristics



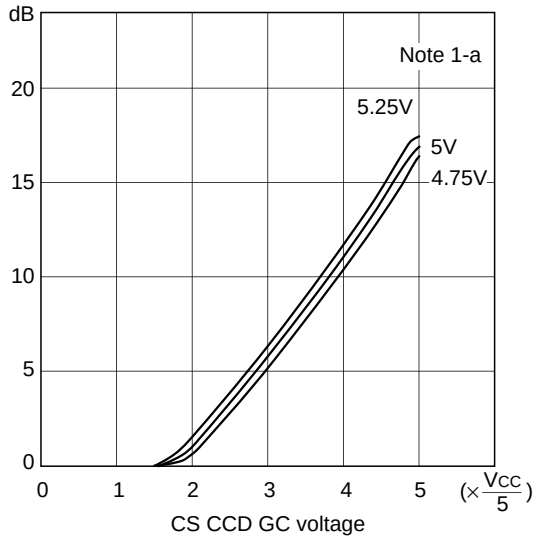
IRIS WINDOW control characeristics (Weighting characteristics)



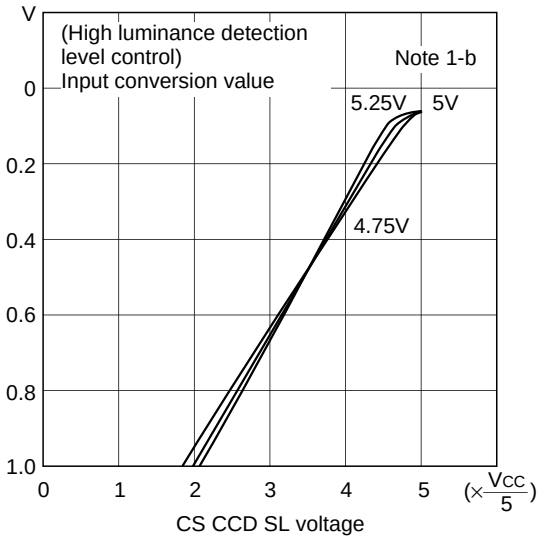
DET WINDOW control (Weighting characteristics)



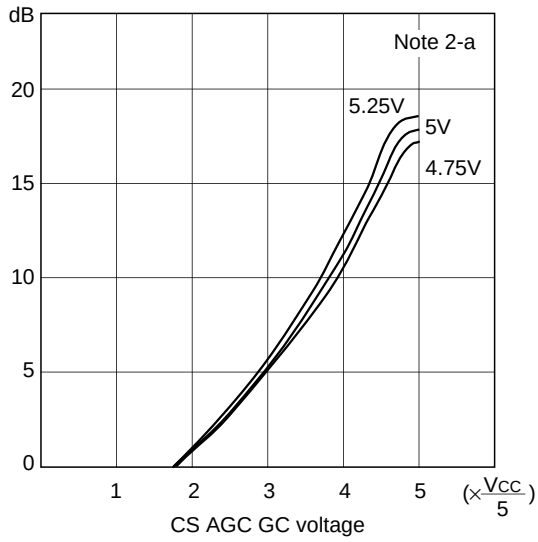
CS CCD gain control characteristics



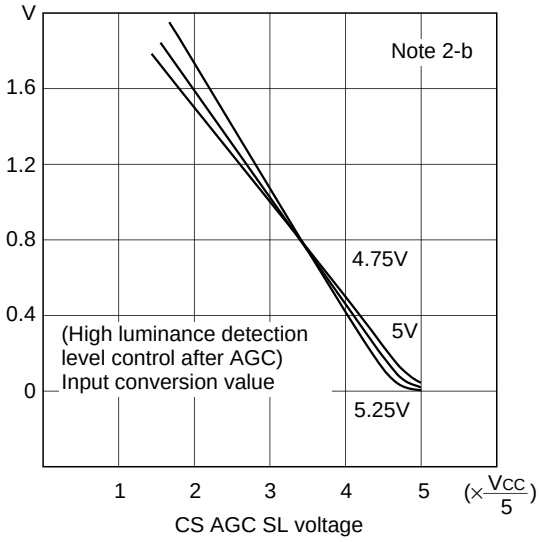
CS CCD slice control characteristics



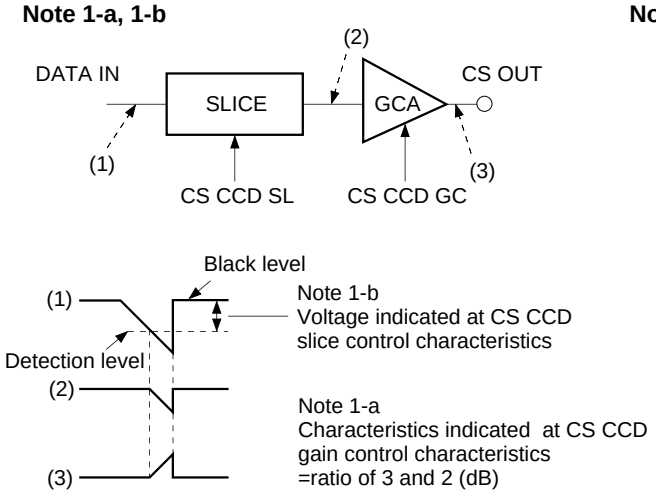
CS AGC gain control characteristics



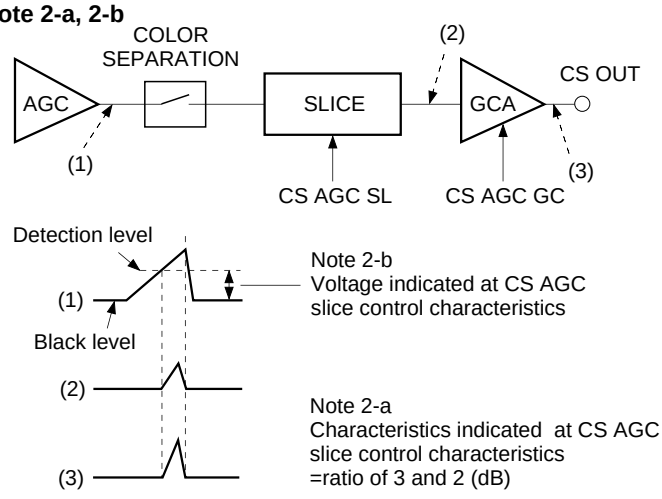
CS AGC slice control characteristics



Note 1-a, 1-b

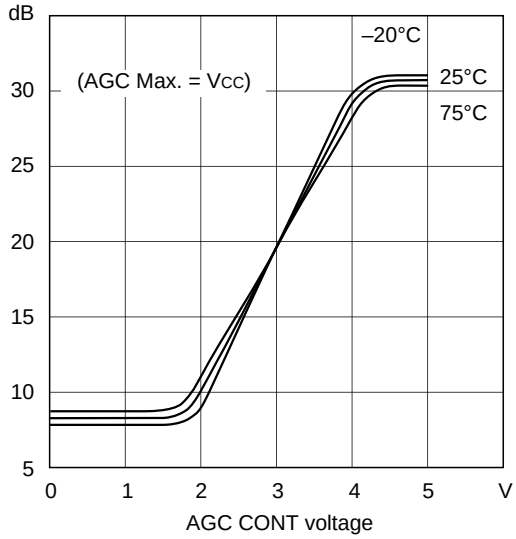


Note 2-a, 2-b

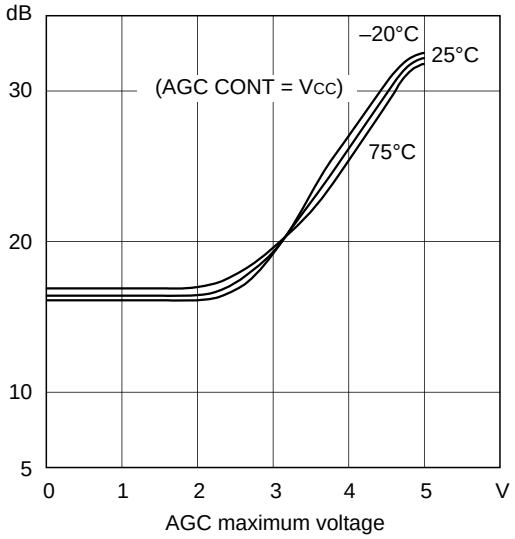


Standard Design Documentation Temperature Characteristics (V_{CC} = 5V)

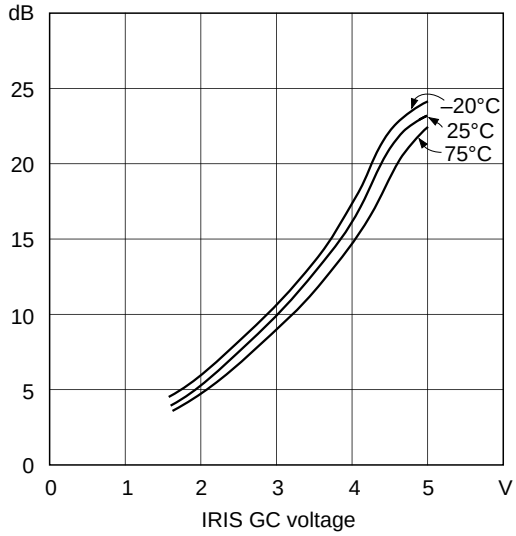
AGC amplifier gain control characteristics



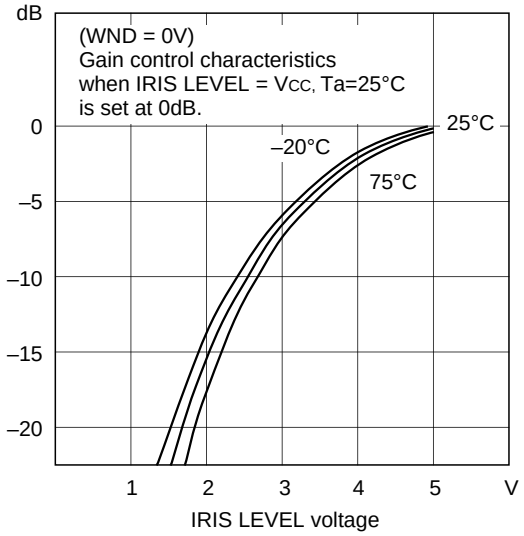
AGC maximum control characteristics



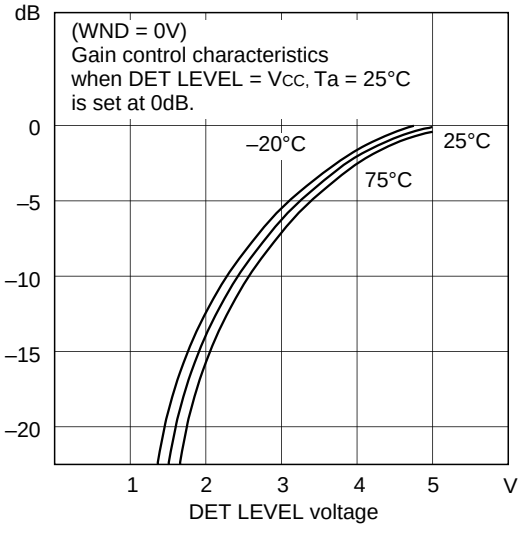
IRIS gain control characteristics



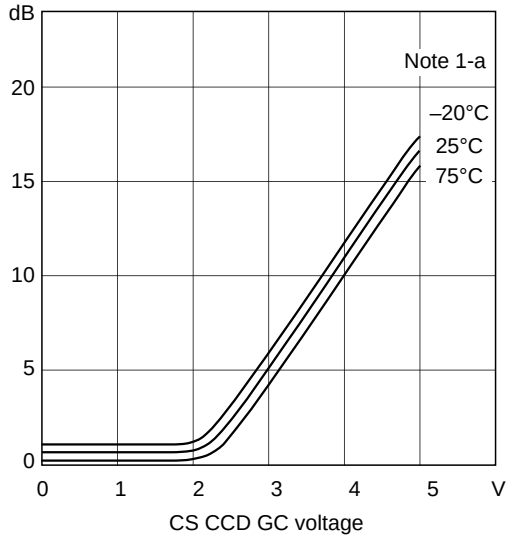
IRIS WINDOW control characteristics (Weighting characteristics)



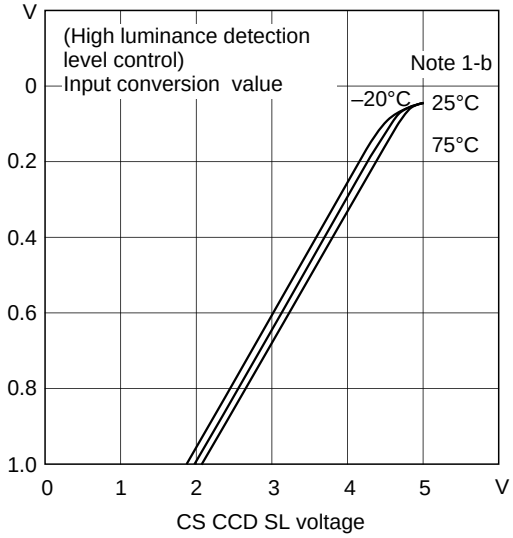
DET WINDOW control (Weighting characteristics)



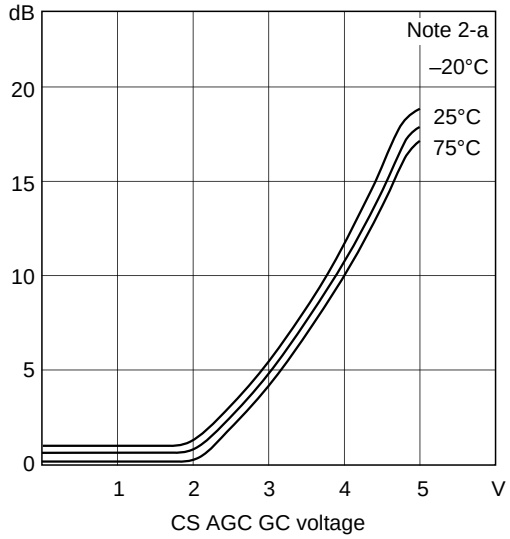
CS CCD gain control characteristics



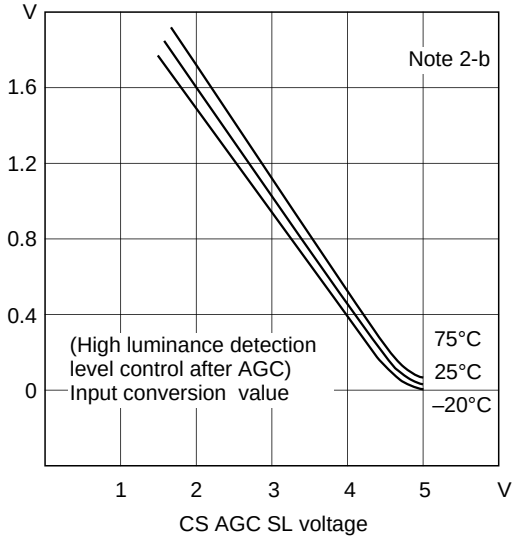
CS CCD slice control characteristics



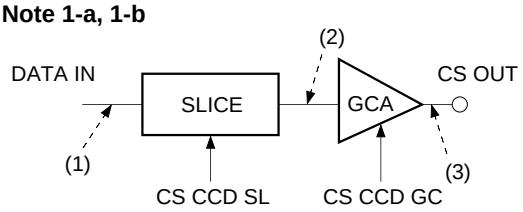
CS AGC gain control characteristics

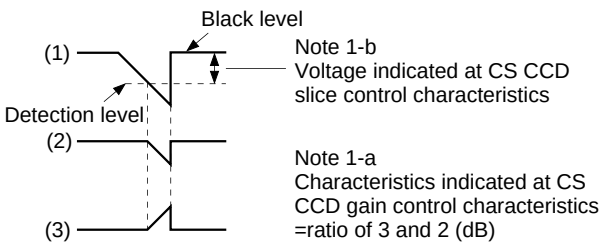


CS AGC slice control characteristics

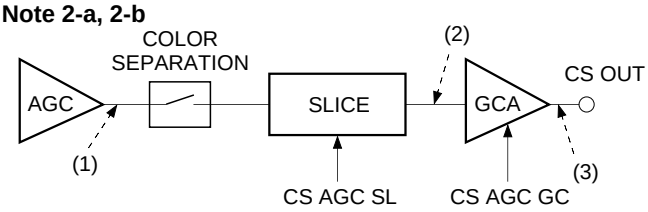


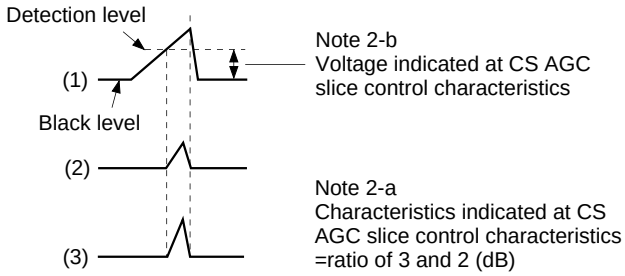
Note 1-a, 1-b



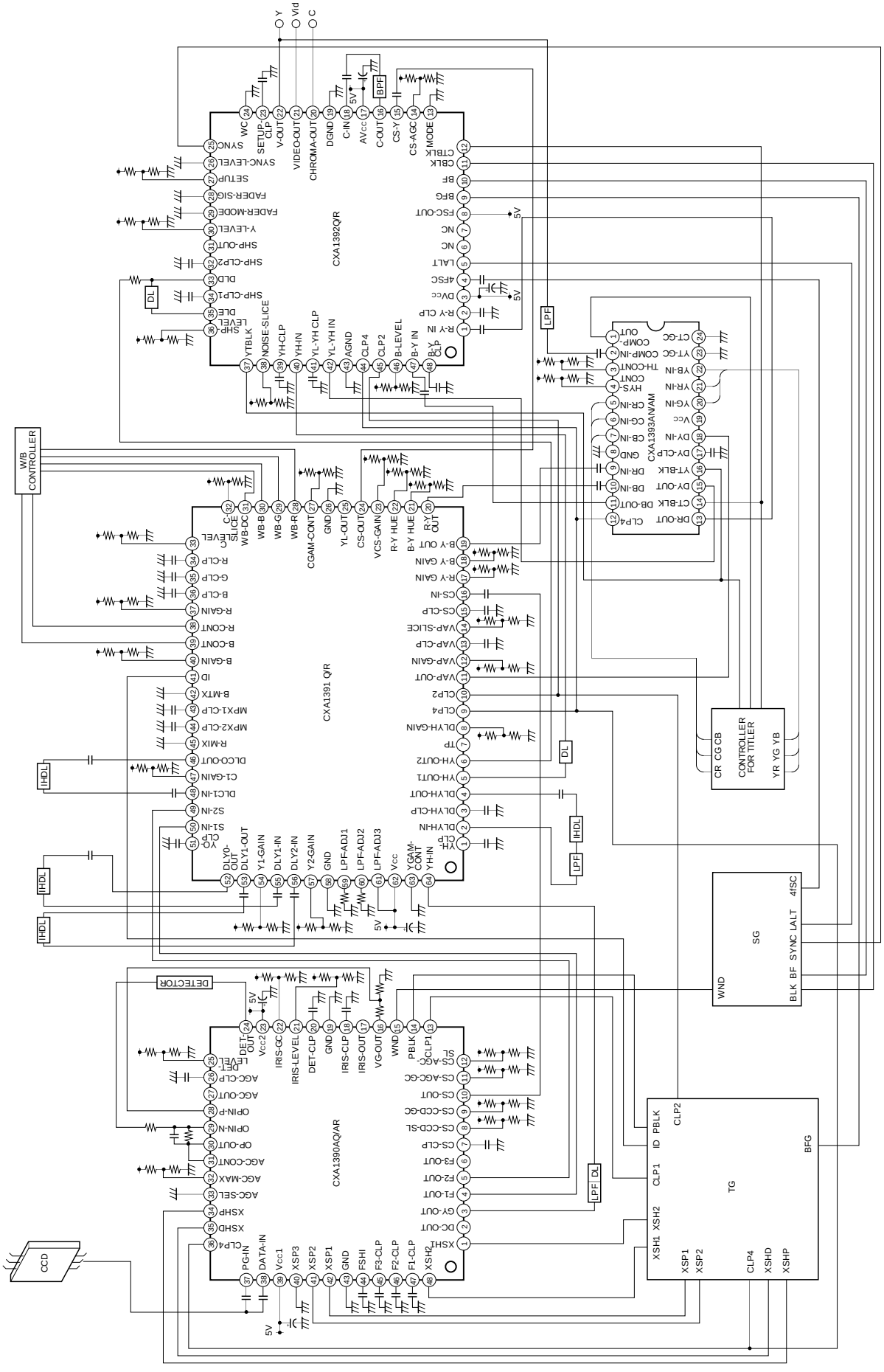


Note 2-a, 2-b





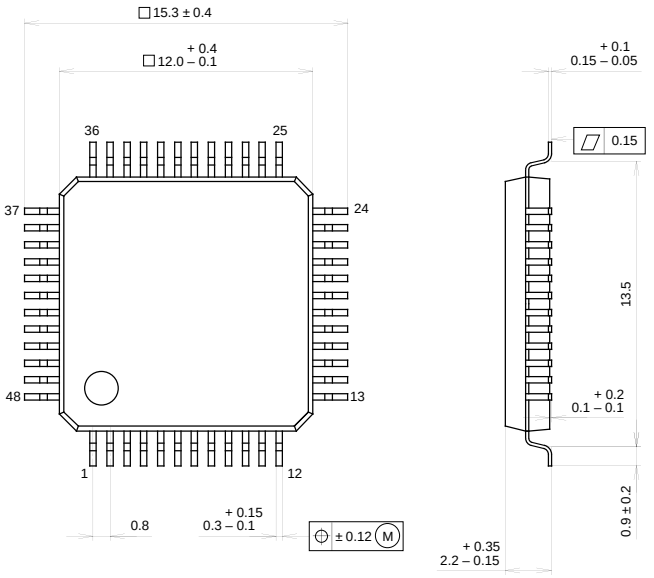
CXA1390 Series System Diagram (The title insertion function can be removed by doing away with CXA1393AN)



Package Outline Unit: mm

CXA1390AQ

48PIN QFP (PLASTIC)



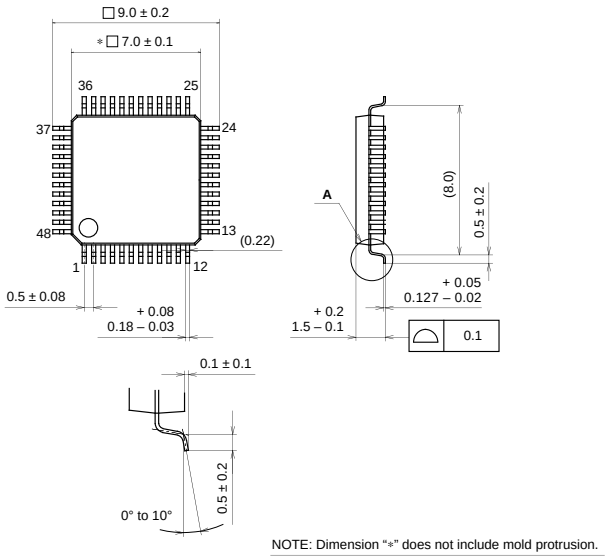
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

SONY CODE	QFP-48P-L04
EIAJ CODE	∗QFP048-P-1212-B
JEDEC CODE	

CXA1390AR

48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g

SONY CODE	LQFP-48P-L01
EIAJ CODE	∗QFP048-P-0707-A
JEDEC CODE	