SONY

CXA1396D

8-bit 125 MSPS Flash A/D Converter

Description

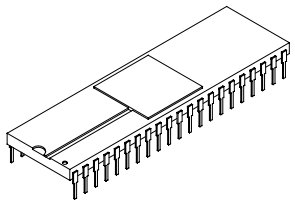
The CXA1396D are 8-bit ultrahigh-speed flash A/D converter ICs capable of digitizing analog signals at the maximum rate of 125 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

The CXA1396D is pin-compatible with the earlier model CX20116. They can replace the earlier models respectively, without any design changes, in most cases. Compared with the earlier models, these new models have been greatly improved in performance, by incorporating advanced process, new circuit design and carefully considered layout.

Features

- Ultrahigh-speed operation with maximum conversion rate of 125 MSPS (Min.)
- Wide analog input bandwidth: 200MHz (Min. for full-scale input)
- Low power consumption: 870mW (Typ.)
- Single power supply: –5.2V
- Low input capacitance
- Built-in integral linearity compensation circuit
- Low error rate
- Operable at 50% clock duty cycle
- Good temperature charactcristics
- Capable of driving 50Ω loads

42 pin DIP (Ceramic)



Structure

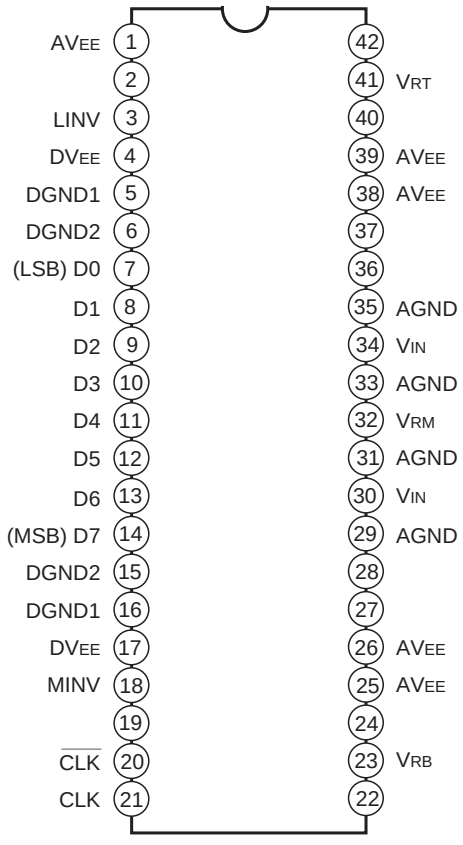
Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- HDTV (high-definition TVs)
- Other apparatus requiring ultrahigh-speed A/D conversion

Pin Configuration

Pins without name are NC pins (not connected).



(Top View)

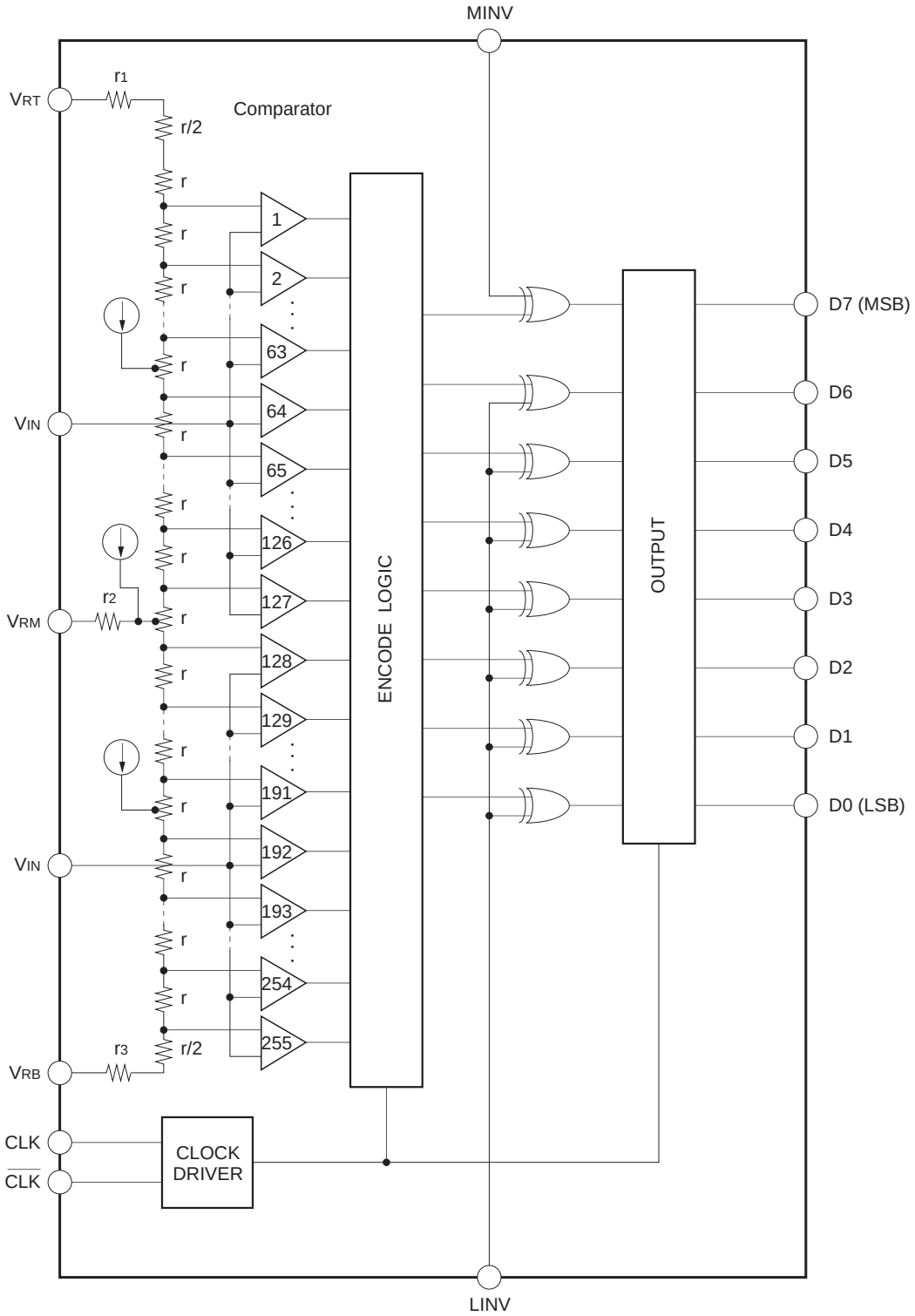
E94521A79-PS

Absolute Maximum Ratings (Ta = 25°C)

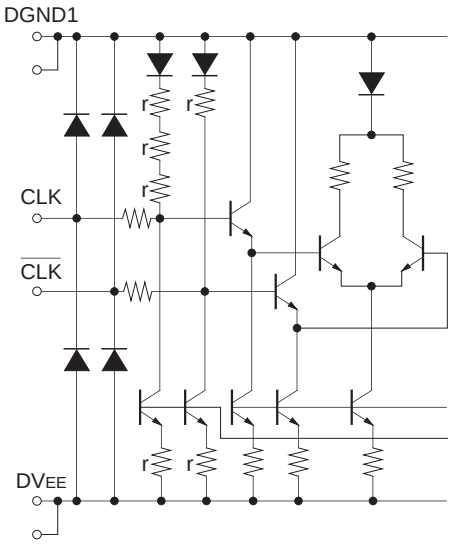
• Supply voltage	AV_{EE}, DV_{EE}	–7 to +0.5	V
• Analog input voltage	V_{IN}	–2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	–2.7 to +0.5	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	–4 to +0.5	V
	$\lvert CLK - \overline{CLK} \rvert$	2.7	V
• V_{RM} pin input curent	I_{VRM}	–3 to +3	mA
• Digital output current	ID_0 to ID_7	–30 to 0	mA
• Storage temperature	Tstg	–65 to +150	°C

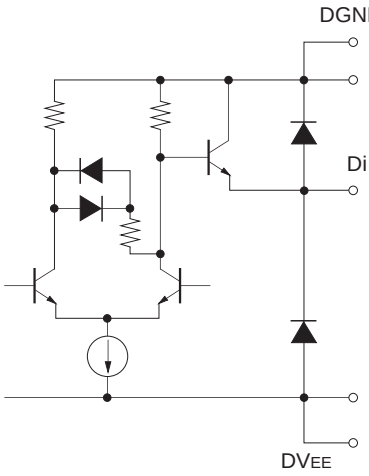
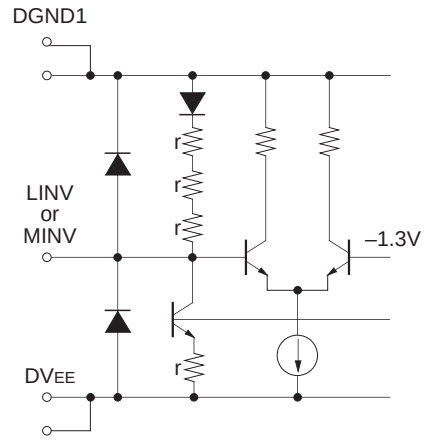
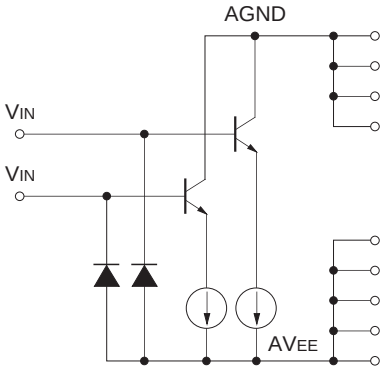
Recommended Operating Conditions		Min.	Typ.	Max.	unit
• Supply voltage	AV_{EE}, DV_{EE}	–5.5	–5.2	–4.95	V
	$AV_{EE} - DV_{EE}$	–0.05	0	+0.05	V
	AGND – DGND	–0.05	0	+0.05	V
• Reference input voltage	V_{RT}	–0.1	0	+0.1	V
	V_{RB}	–2.2	–2.0	–1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Pulse width of clock	T_{PW1}	4.0			ns
	T_{PW0}	4.0			ns
• Operating temperature	Ta	–20		+75	°C

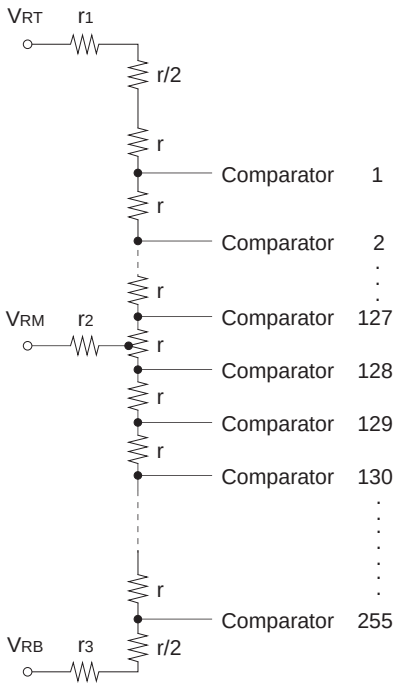
Block Diagram



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
29, 31, 33, 35	AGND	—	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	AV_{EE}	—	–5.2V		Analog V_{EE}. –5.2V (Typ.). Internally connected with DV_{EE} (resistance: 4 to 6Ω). A ceramic chip capacitor of at least 0.1µF should be used to connect to AGND and be placed near the pins.
21	CLK	I	ECL		CLK input
20	$\overline{CLK}$				Complementary input to CLK. With open connection, kept at threshold voltage (–1.3V). Device is operable without $\overline{CLK}$ input, but use of omplementary inputs of CLK and $\overline{CLK}$ is recommended to obtain the stable high-speed operation.
5, 16	DGND1	—	0V		Digital GND for internal circuits.
6, 15	DGND2	—	0V		Digital GND for output transistors.
4, 17	DV_{EE}	—	–5.2V		Digital V_{EE}. Internally connected with AV_{EE} (resistance: 4 to 6Ω). A ceramic chip capacitor of at least 0.1µF should be used to connect to DGND near the pins.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
7	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	D1				Data outputs. External pull-down resistors are required.
9	D2				
10	D3				
11	D4				
12	D5				
13	D6				
14	D7				MSB of data outputs. External pull-down resistor is required.
3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see output code table). With open connection, kept at "L" level.
18	MINV	I	ECL		Input pin for D7(MSB) output polarity inversion (see output code table). With open connection, kept at "L" level.
30, 34	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
23	V_{RB}	I	–2V		Reference voltage (bottom). Typically –2V. A ceramic capacitor of at least 0.1µF and a tantalum capacitor of at least 10µF should be used to connect to AGND near the pins.
32	V_{RM}	I	V_{RB}/2		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
41	V_{RT}	I	0V		Reference voltage (top). Typically 0V. When a voltage except for AGND is applied to this pin, a ceramic capacitor of at least 0.1µF and a tantalum capacitor of at least 10µF should be used to connect to AGND near the pins.
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	NC	—	—		Unused pins. No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

Electrical Characteristics (Ta = 25°C, AV_{EE} = DV_{EE} = –5.2V, V_{RT} = 0V, V_{RB} = –2V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n			8		bits
DC characteristics						
Integral linearity error	E_{IL}	Fc = 125MSPS		±0.3	±0.5	LSB
Differential linearity error	E_{DL}	Fc = 125MSPS		±0.3	±0.5	LSB
Analog input						
Analog input capacitance	C_{IN}	V_{IN} = –1V + 0.07Vrms		17		pF
Analog input resistance	R_{IN}			190		kΩ
Input bias current	I_{IN}	V_{IN} = –1V		130	320	µA
Reference inputs						
Reference resistance	R_{REF}		75	110	155	Ω
Offset voltage V_{RT}	E_{OT}		8	19	32	mV
V_{RB}	E_{OB}		0	15	24	mV
Digital inputs						
Logic H level	V_{IH}		–1.13			V
Logic L level	V_{IL}				–1.50	V
Logic H current	I_{IH}	Input connected to –0.8V	0		50	µA
Logic L current	I_{IL}	Input connected to –1.6V	–50		50	µA
Input capacitance				7		pF
Switching characteristics						
Maximum conversion rate	Fc	Error rate 10^{-9} TPS*1	125			MSPS
Aperture jitter	Taj			10		ps
Sampling delay	Tds			1.5		ns
Output delay	Tdo		3.0	3.6	4.2	ns
H pulse width of clock	T_{PW1}		4.0			ns
L pulse width of clock	T_{PW0}		4.0			ns
Digital outputs						
Logic H level	V_{OH}	R_L = 50Ω to –2V	–1.10			V
Logic L level	V_{OL}	R_L = 50Ω to –2V			–1.62	V
Output rising time	Tr	R_L = 50Ω to –2V, 20% to 80%		0.8		ns
Output falling time	Tf	R_L = 50Ω to –2V, 80% to 20%		1.0		ns
Dynamic characteristics						
Input bandwidth		V_{IN} = 2Vp-p, 3dB down	200			MHz
S/N ratio		Input = 1MHz, FS, Clock = 125MHz		46		dB
		Input = 31.5MHz, FS, Clock = 125MHz		40		dB
Error rate		Input = 31.249MHz, FS, Error > 16LSB, Clock = 125MHz			10^{-9}	TPS*1
Differential gain error	DG	NTSC 40IRE mod.ramp, Fc = 125MSPS		1.0		%
Differential phase error	DP			0.5		deg
Power supply						
Supply current	I_{EE}		–230	–160		mA
Power consumption*2	Pd			870		mW

*1 TPS: times Per Sample

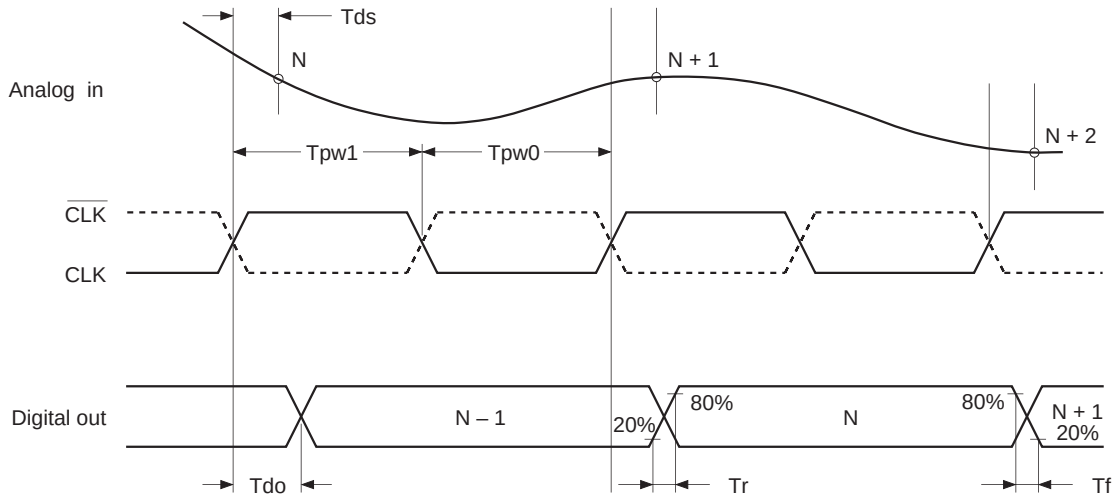
*2 $Pd = I_{EE} \cdot V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$

Output Code Table

V_{IN}*	Step	MINV 1 LINV 1	0 1	1 0	0 0
		D7 D0	D7 D0	D7 D0	D7 D0
0V		0 0 0 ····· 0 0	1 0 0 ····· 0 0	0 1 1 ····· 1 1	1 1 1 ····· 1 1
	0	0 0 0 ····· 0 0	1 0 0 ····· 0 0	0 1 1 ····· 1 1	1 1 1 ····· 1 1
	1	0 0 0 ····· 0 1	1 0 0 ····· 0 1	0 1 1 ····· 1 0	1 1 1 ····· 1 0
		:	:	:	:
		:	:	:	:
–1V	127	0 1 1 ····· 1 1	1 1 1 ····· 1 1	0 0 0 ····· 0 0	1 0 0 ····· 0 0
	128	1 0 0 ····· 0 0	0 0 0 ····· 0 0	1 1 1 ····· 1 1	0 1 1 ····· 1 1
		:	:	:	:
		:	:	:	:
	254	1 1 1 ····· 1 0	0 1 1 ····· 1 0	1 0 0 ····· 0 1	0 0 0 ····· 0 1
	255	1 1 1 ····· 1 1	0 1 1 ····· 1 1	1 0 0 ····· 0 0	0 0 0 ····· 0 0
–2V		1 1 1 ····· 1 1	0 1 1 ····· 1 1	1 0 0 ····· 0 0	0 0 0 ····· 0 0

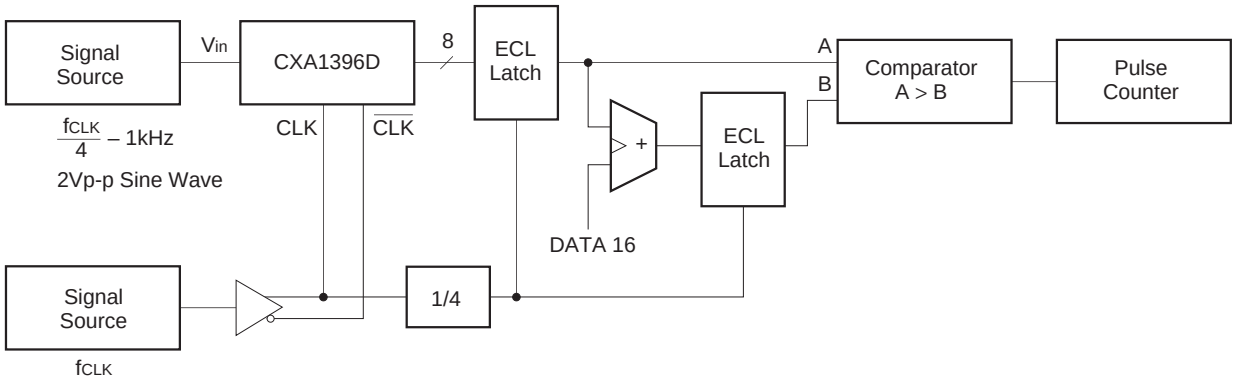
* V_{RT} = 0V, V_{RB} = –2V

Timing diagram

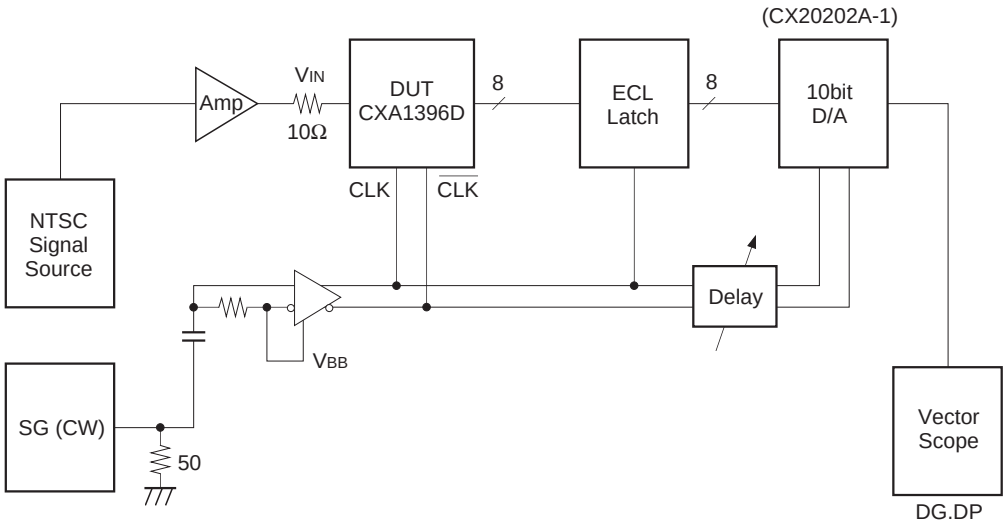


Electrical Characteristics Test Circuit

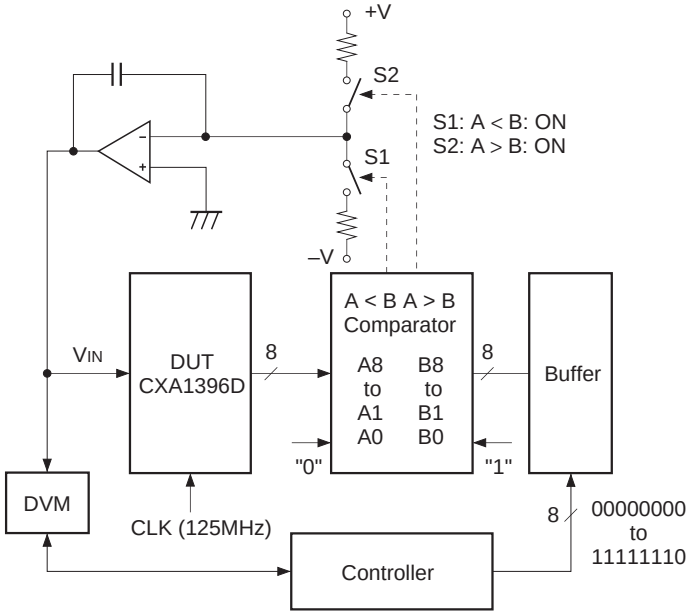
Maximum conversion rate test circuit



Differential gain error test circuit
Differential phase error test circuit

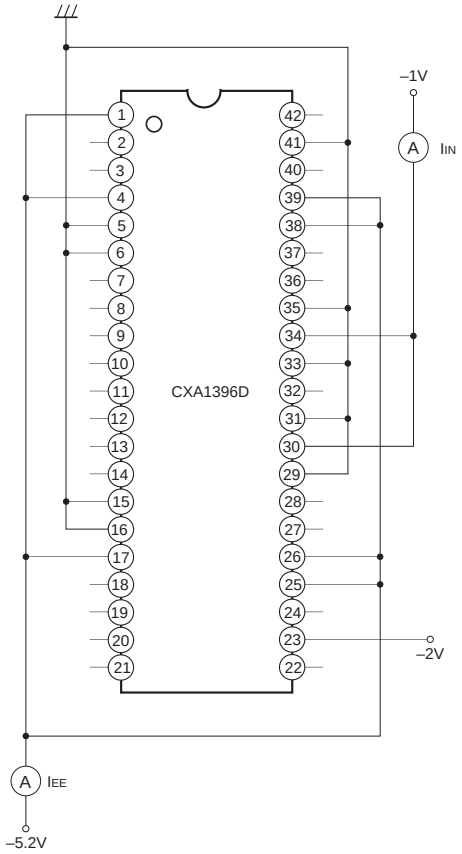


Integral linearity error test circuit
Differential linearity error test circuit

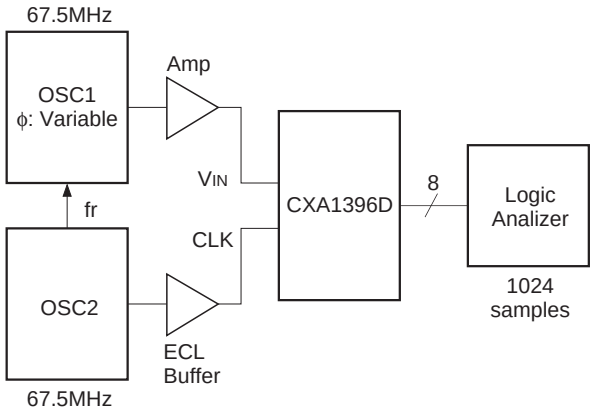


Power Supply Current Test Circuit

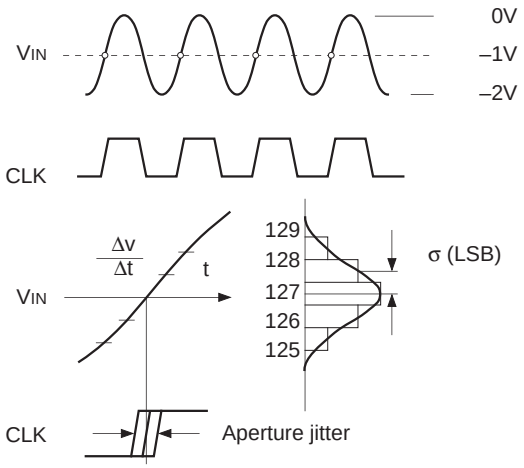
Analog input bias current test circuit



Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



Apeature jitter is defined as follows:

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

8-bit, 125MSPS ADC Evaluation board

Description

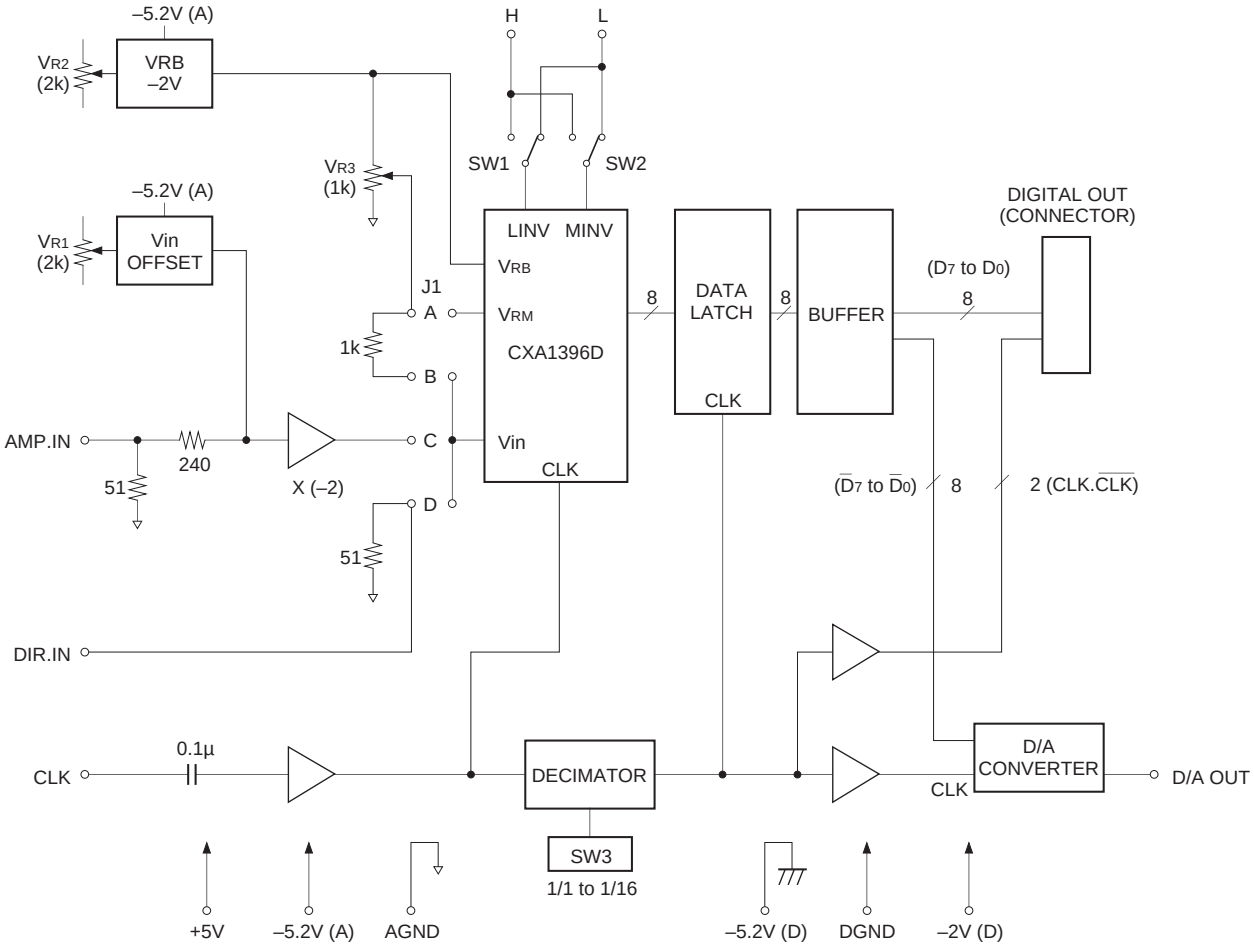
The CXA1396D EVALUATION BOARD WITH DAC is a tool for customers to evaluate the performance of the CXA1396D (8-bit, 125MSPS, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips two sets of analog inputs (the direct input and the buffer amplifier input), the input voltage offset generator, the clock decimator, the output data latches, the 10-bit high-speed DAC, and the 20-pin cable connector for digital outputs.

This evaluation board provides full performance of the CXA1396D and it is designed to facilitate evaluation.

Features

- Resolution: 8bits
- Maximum conversion rate: 125MSPS
- Supply voltage: +5.0V, –5.2V, –2.0V
- Two analog inputs (Direct input, buffer amplifier input)
- Clock level converter: Sine wave to ECL level signal
- Reference voltage adjustment circuit for the A/D converter
- Built-in clock frequency decimation circuit: (1/1 to 1/16)

Fig. 1. Block Diagram



Supply Current

Item	Min.	Typ.	Max.	Unit
–5.2V		0.85	1.0	A
+5.0V		15	30	mA
–2.0V		0.45	0.6	A

(**Note:** Supply current –2.0V is the value when Rn10, Rn11 and Rn12 are not mounted.)

Analog Input (DIR. IN, AMP. IN)

Item	Min.	Typ.	Max.	Unit
Input voltage (DIR. IN)	–2.0		0	V
(AMP. IN) *1	–0.5		+0.5	V
Input impedance		50		Ω

(*1: Adjustable by VR1)

Clock Input (CLK)

Item	Min.	Typ.	Max.	Unit
Input voltage (Peak to Peak)		1.0		Vp-p
Input impedance		50		Ω

Digital Output (D0 to D7)

ECL 10KH level

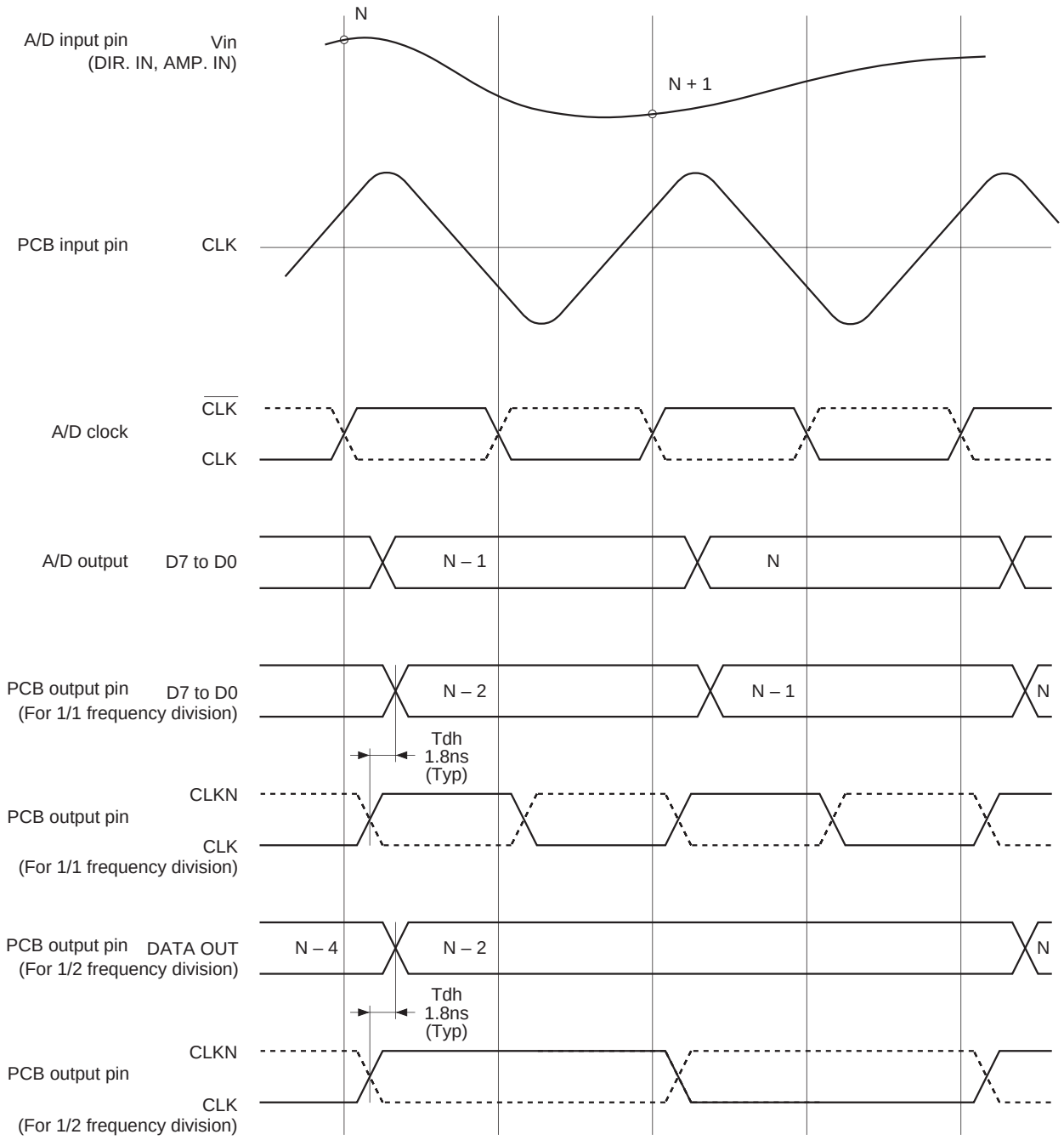
Clock Output

ECL 10KH level, complementary output

Output Code Table

	MINV LINV	0 0	0 1	1 0	1 1
V_{IN}	0V	1 1 1 ····· 1 1	1 0 0 ····· 0 0	0 1 1 ····· 1 1	0 0 0 ····· 0 0
	:	1 1 1 ····· 1 0	1 0 0 ····· 0 1	0 1 1 ····· 1 0	0 0 0 ····· 0 1
	:	:	:	:	:
	:	:	:	:	:
	:	1 0 0 ····· 0 0	1 1 1 ····· 1 1	0 0 0 ····· 0 0	0 1 1 ····· 1 1
	:	0 1 1 ····· 1 1	0 0 0 ····· 0 0	1 1 1 ····· 1 1	1 0 0 ····· 0 0
	:	:	:	:	:
	:	:	:	:	:
	:	0 0 0 ····· 0 1	0 1 1 ····· 1 0	1 0 0 ····· 0 1	1 1 1 ····· 1 0
	–2V	0 0 0 ····· 0 0	0 1 1 ····· 1 1	1 0 0 ····· 0 0	1 1 1 ····· 1 1

Fig. 2. Timing Chart



Adjustment Methods and Notes on Operation

1) Vin Offset (VR1)
The volume to adjust the signal range (0V center assumed) with the A/D converter input range when a waveform is input through AMP. IN.

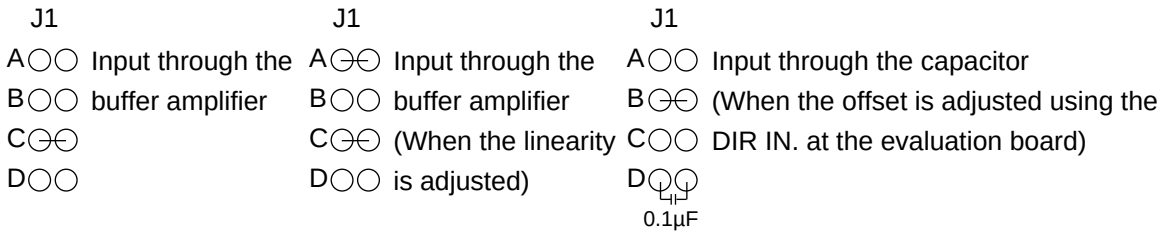
2) A/D Full Scale (VR2)
The volume to adjust A/D converter VRB voltage.

3) Linearity (VR3)
The volume to adjust VRM (linearity) voltage. When DIR. IN input selected and it is supplied through the capacitor, VR3 can be used to adjust the input offset voltage.

4) D/A Full Scale (VR4)
The volume to adjust D/A output full scale (–1V).

5) J1 (Input selection)
A: Shorts to adjust VRM voltage.
B: Shorts to supply DC voltage to Vin.
C: Shorts to select AMP.IN input.
D: Shorts to select DIR.IN input.

[Jumper Position at Shipment]



6) SW1
The switch for LINV High/Low.

7) SW2
The switch for MINV High/Low.

8) SW3 (Decimation)
The switch to select clock frequency decimation.
Switch position: decimation ratio
0: 1/1
1: 1/2
2: 1/4
3: 1/8
4: 1/16

9) SW4 (D/A INV)
The switch for D/A converter output inversion.

10) Rn10, Rn11 and Rn12 are not mounted at shipment. They are not required during evaluation.

11) Waveform probe pins P5 and P8 through P28 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mil, and there is ϕ1.2mm through hole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).

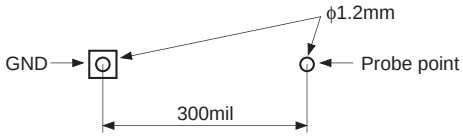
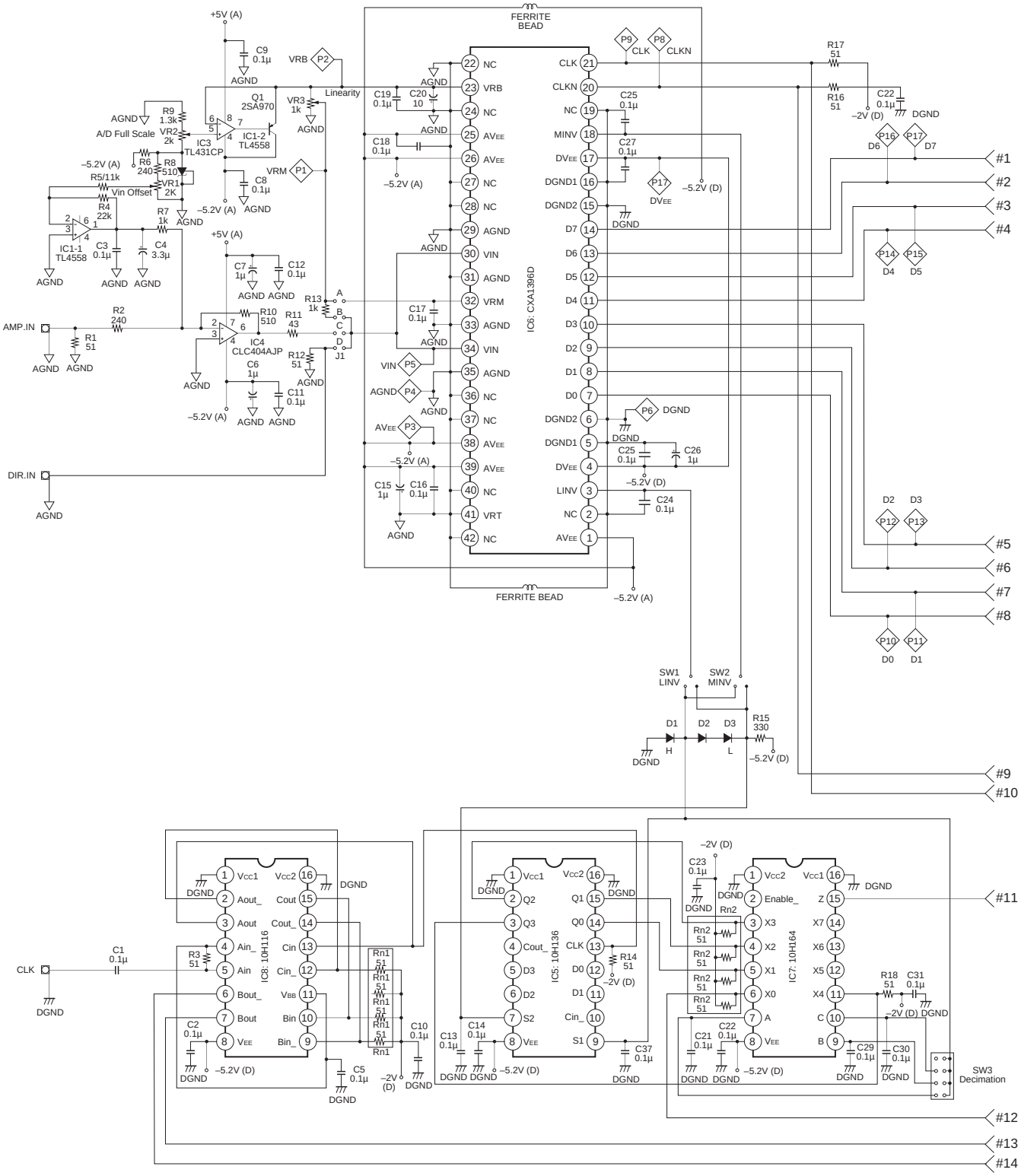


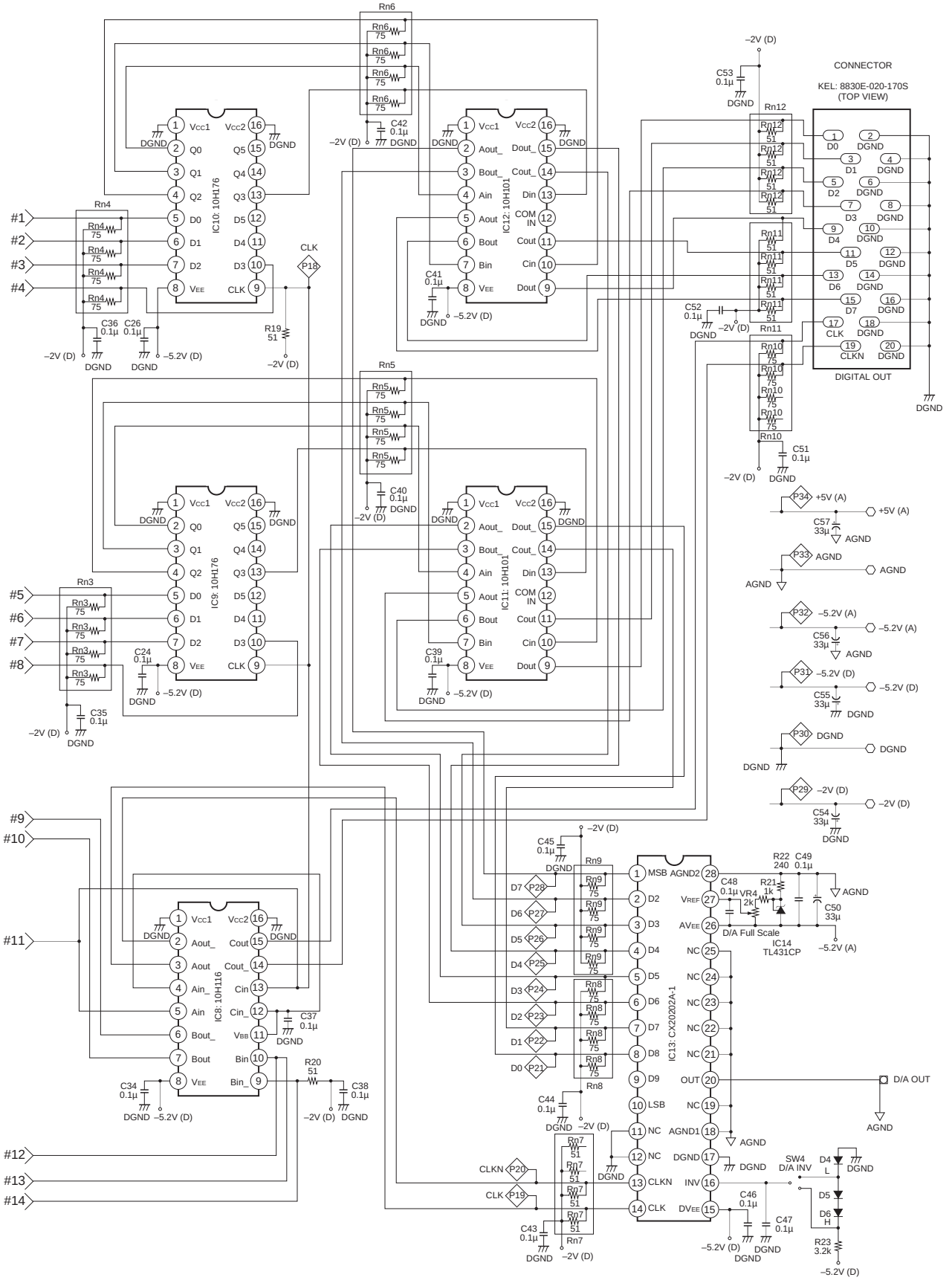
Fig. 3

12) D/A converter (IC13) input data (waveform probe pins P21 through P28) are the complementary signals of the decimated A/D converter outputs. Those are inverted again in the D/A converter so that the direction of reproduced waveform can agree with the A/D input signal converter.

13) The part unmber of the digital output connector is KEL 8830E-020-170S. A corresponding connector and cable assembly is JUNKOSMA KBO020MCG50BI.

PCB Circuit Schematic




CONNECTOR
KEL: 8830E-020-170S
(TOP VIEW)
DIGITAL OUT
IC10: 10H176
IC12: 10H101
IC9: 10H176
IC11: 10H101
IC8: 10H116
IC13: CX20202A-1
IC14
TL431CP
D/A Full Scale
D/A OUT
SW4
D/A INV
+5V (A)
–5.2V (A)
–5.2V (D)
–2V (D)
AGND
DGND

Characteristic Graph

Fig. 5. Gain vs. Input frequency

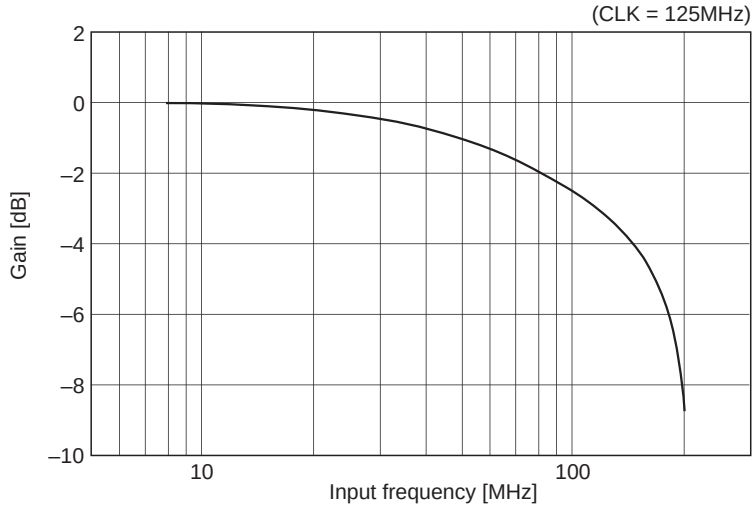


Fig. 6. SNR vs. Input frequency

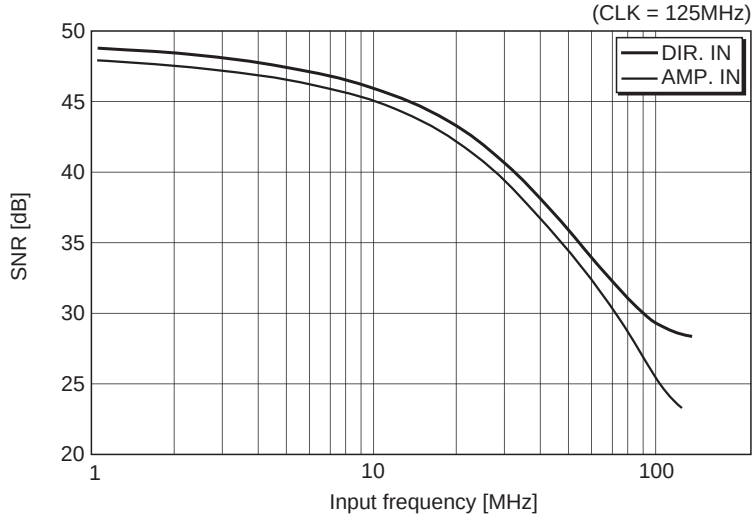
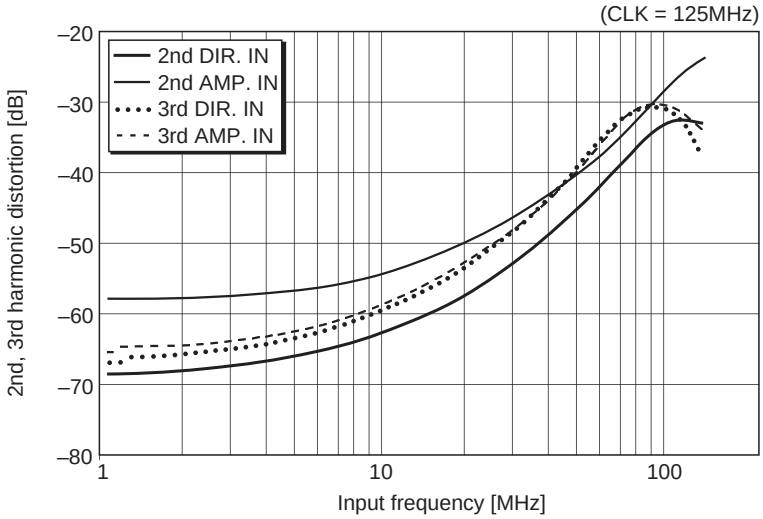


Fig. 7. 2nd, 3rd harmonic distortion vs. Input frequency

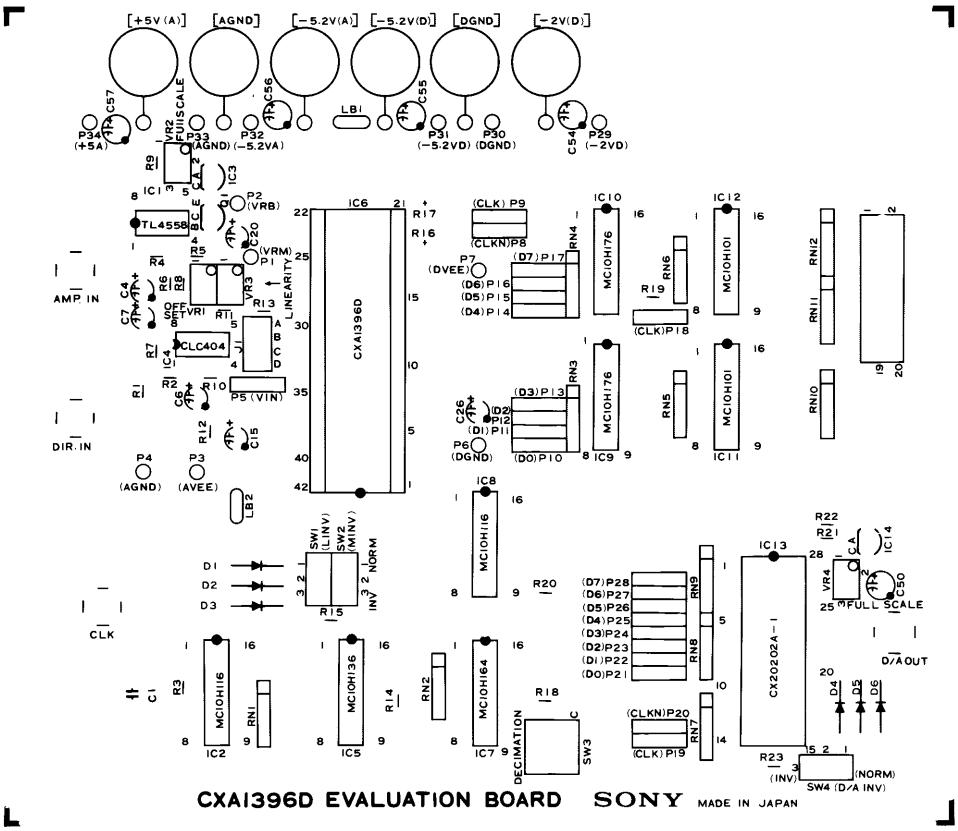


Measurement data

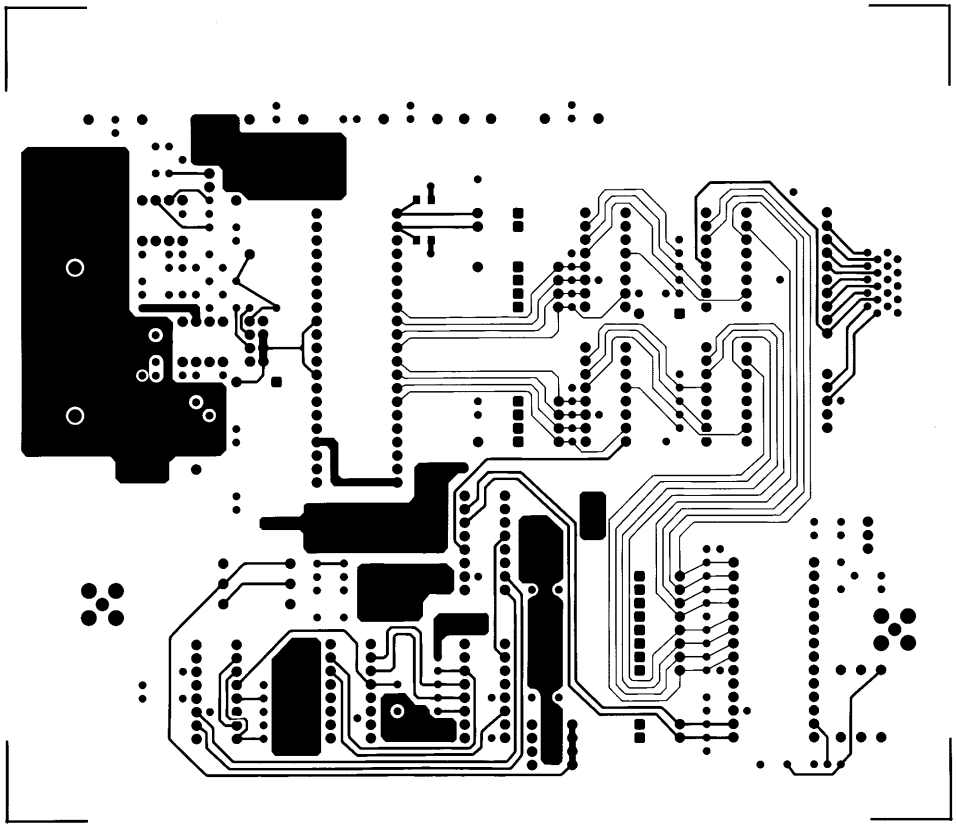
Figs. 5, 6 and 7 show the characteristic graphs.

DIR. IN is the characteristic where the signal is directry input to the ADC and AMP. IN is the characteristic where the signal is input to ADC through the amplifier.

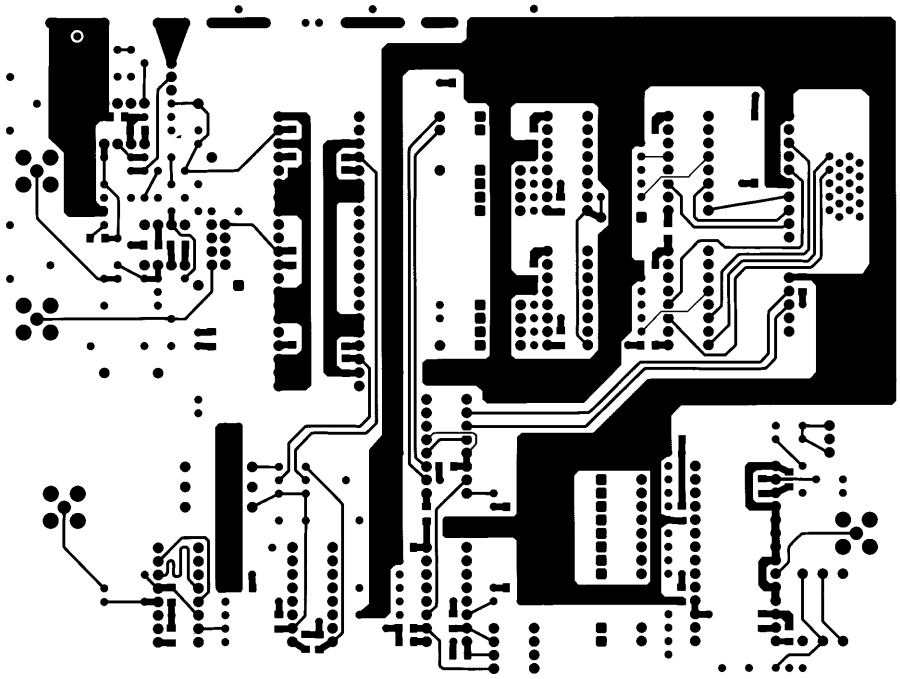
Parts Layout



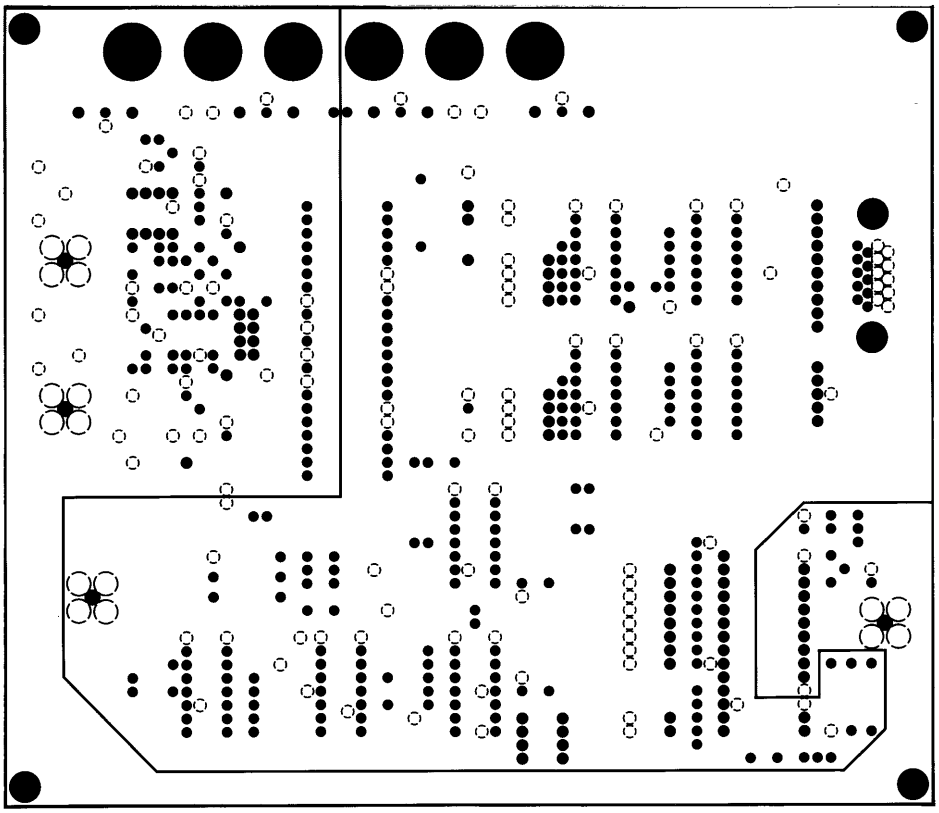
Printed Pattern



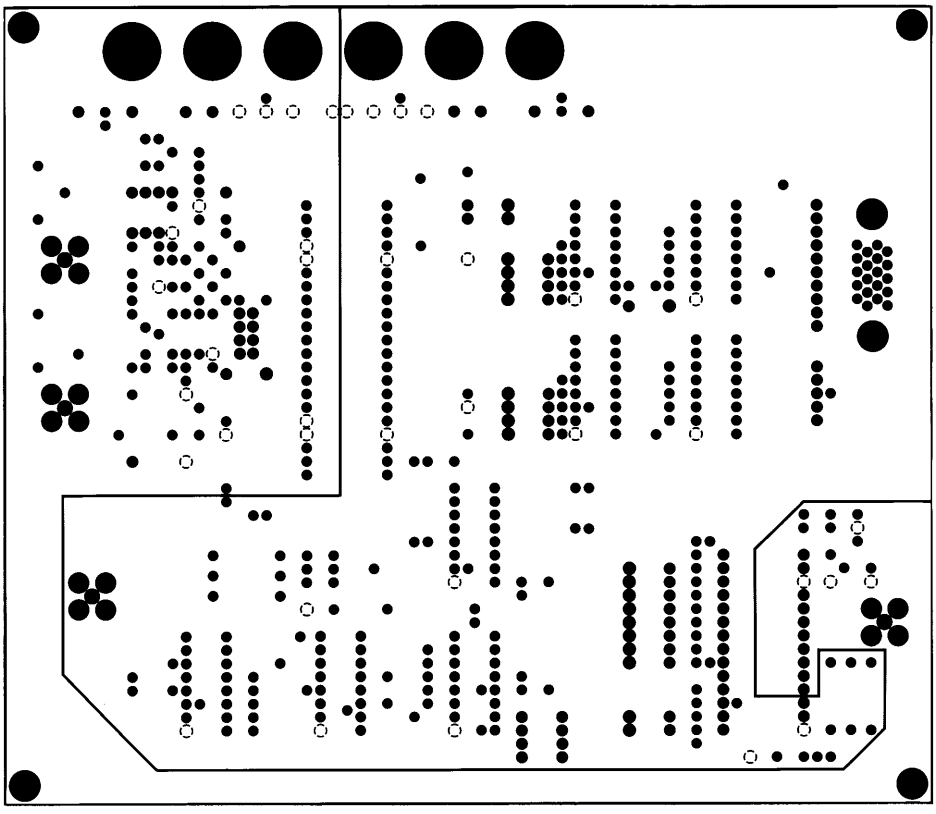
1st layer Component plane (Top View)



4th layer Solder plane (Top View)



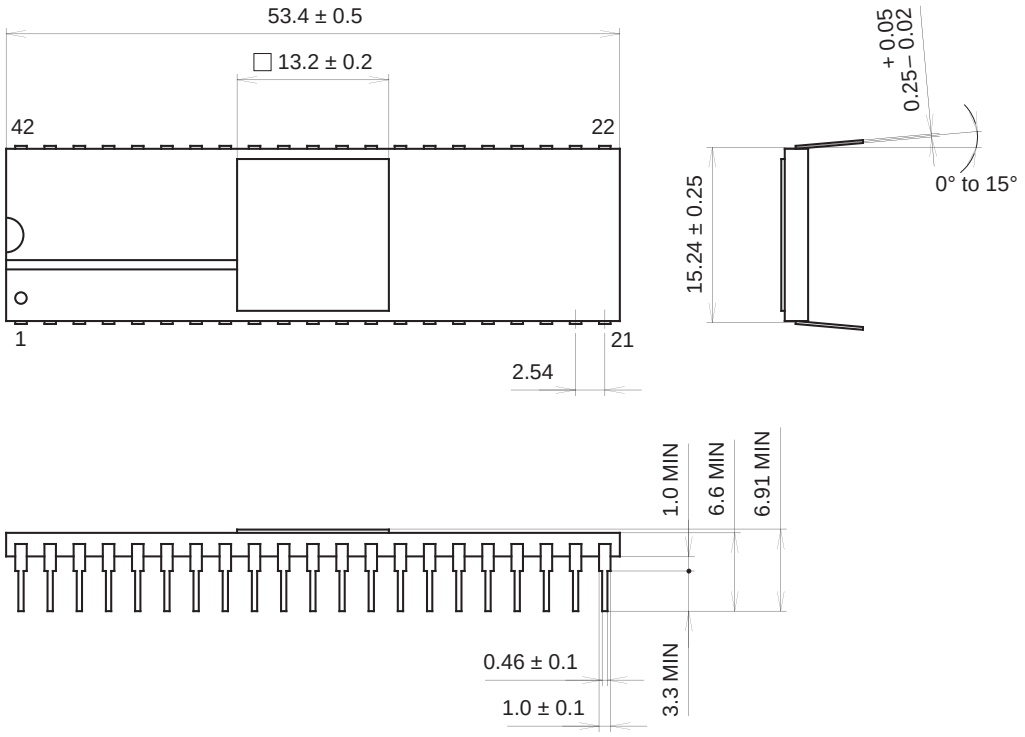
2nd layer GND plane (Top View)



3rd layer Power supply plane (Top View)

Package Outline Unit: mm

42PIN DIP (CERAMIC) 600mil



SONY CODE	DIP-42C-01
EIAJ CODE	∗DIP042-C-0600-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	6.7g