SONY

CXA2149Q

I²C-Bus-Compatible Audio/Video Switch

Description

The CXA2149Q is a video and audio switch IC featuring I²C bus compatibility for TV's. The IC has input pins that are compatible with the SCART protocols. It offers other features such as an electronic mute function with switching noise reduction (zero cross detection), electronic volume control, automatic SYNC pulse detection, and group delay control.

Features

- 3 CVBS inputs.
- 2 CVBS outputs.
- Group delay control on TV and CVIN1.
- SYNC ID on TV and CVIN1.
- 3 Y/C inputs.
- 2 Y/C outputs.
- 6 L/R/2 inputs.
- 3 L/R/2 outputs.
- Mode inputs compatible with the SCART protocol.
- 3 Y/C mixer circuits.
- Audio muting via software control.
- External muting input.
- Audio switching noise elimination circuit.
- Volume adjustment via software control on L/R channel 3.
- Wide band video amplifiers (20 MHz, –3 dB).
- Wide audio dynamic range (3 Vrms typ)
- Serial control via I²C bus.
- Separate control of video and audio switches.
- High impedance maintained by I²C lines (SDA, SCL) even when power is off.
- Configurable dual slave address 90/92.
- I²C bus 5 and 3.3 V compatible.

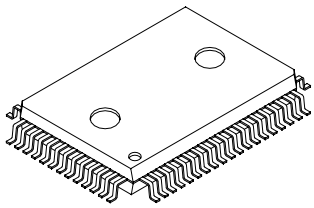
Applications

TV's

Structure

Bipolar silicon monolithic IC

64 pin QFP (Plastic)



Absolute Maximum Ratings

(Ta=25 °C unless stated)

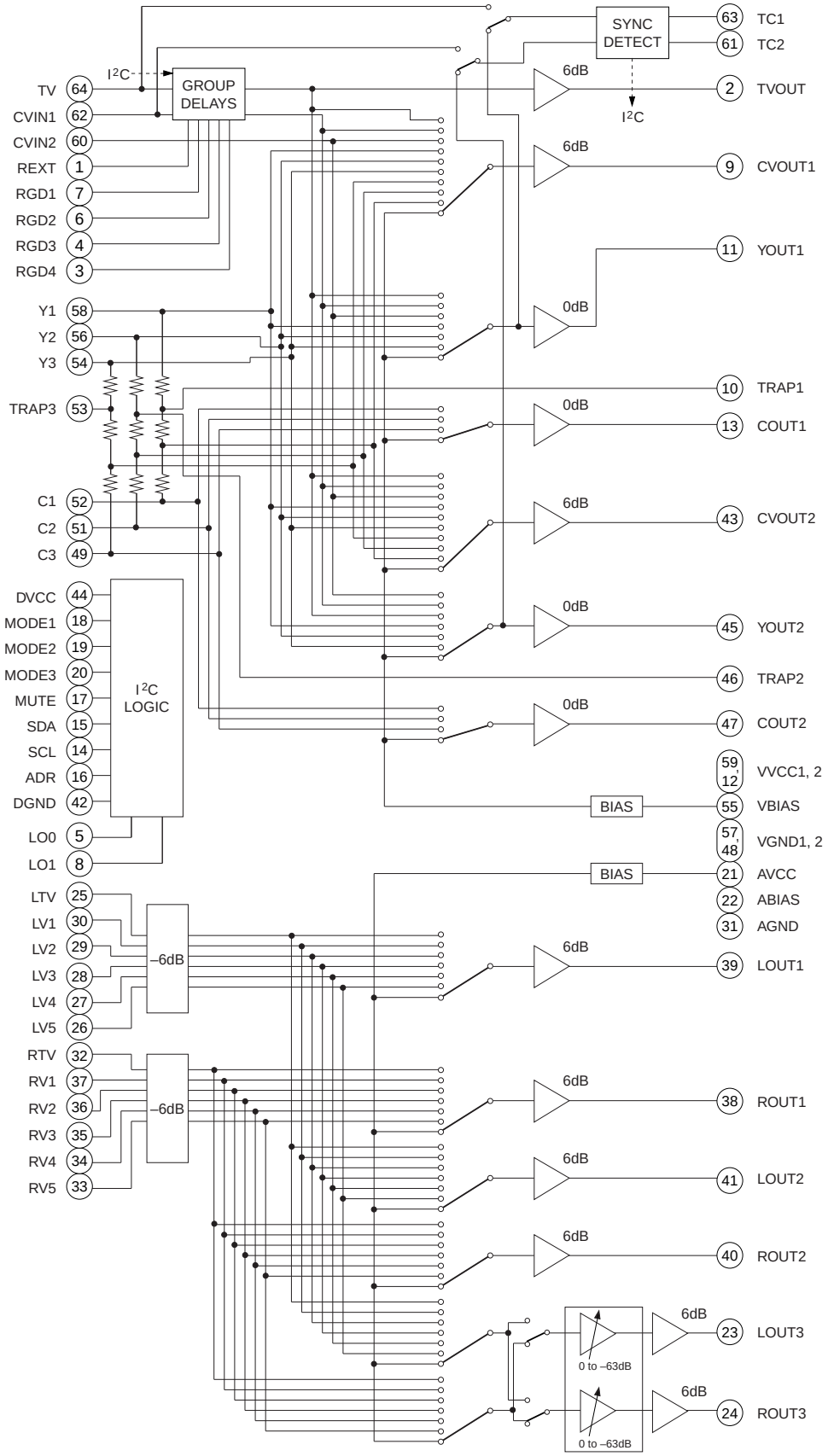
• Supply voltage	V_{CC}	12	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	900	mW

Operating Conditions

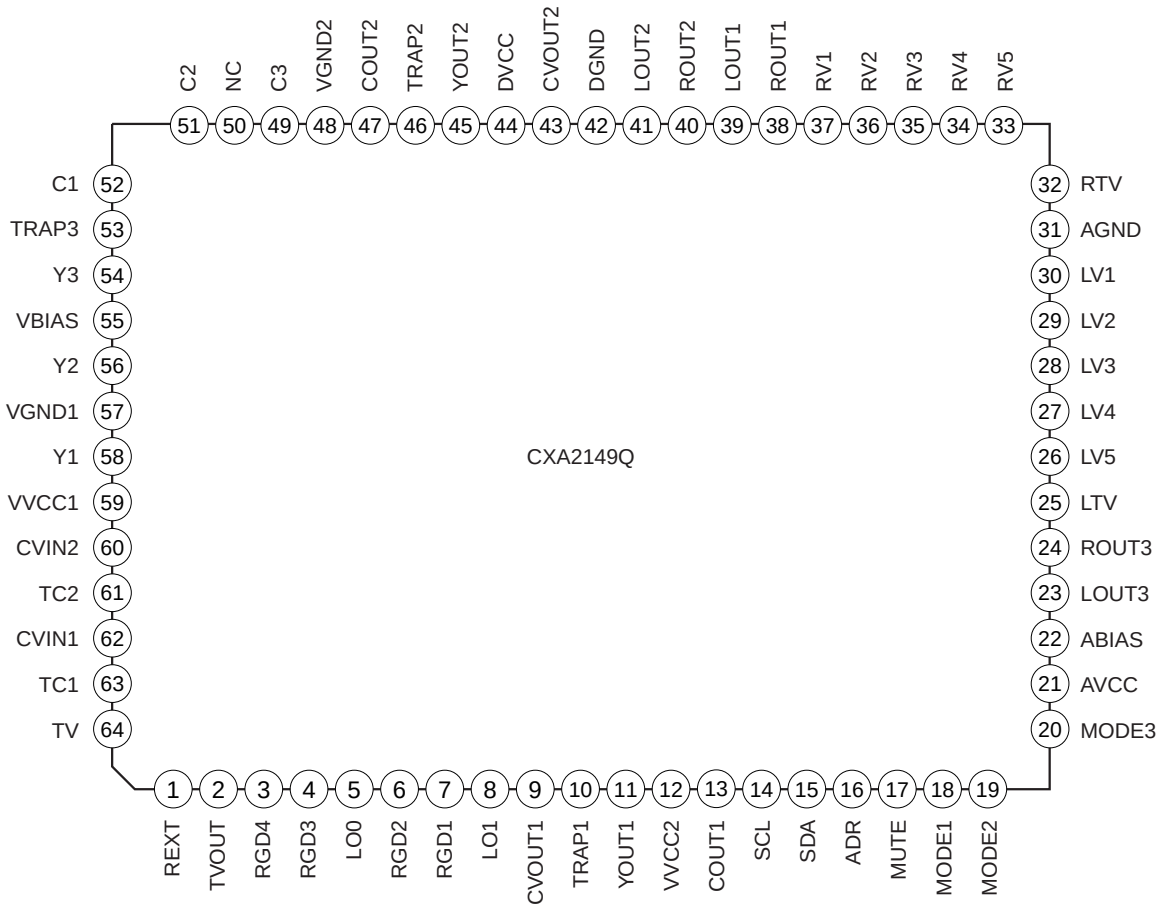
• Supply voltage	V_{CC}	9+/–0.5	V
• Typical supply current		75	mA
• Operating temperature	Topr	–20 to +75	°C

E99946-TE

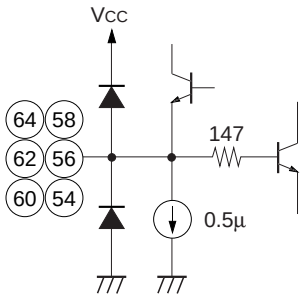
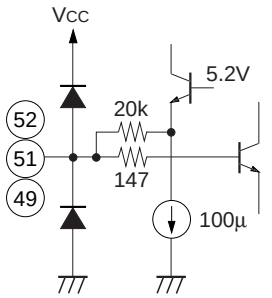
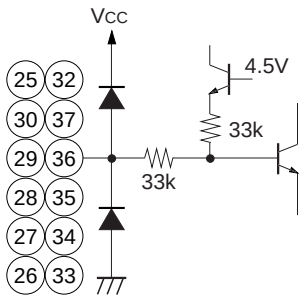
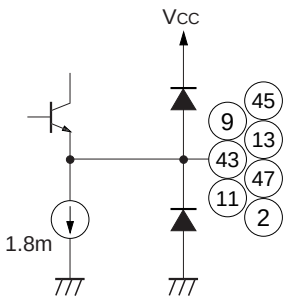
Block Diagram

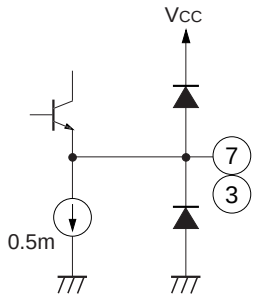
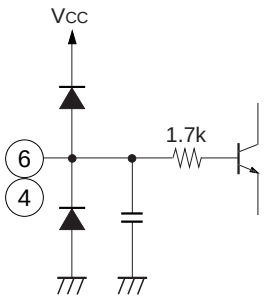
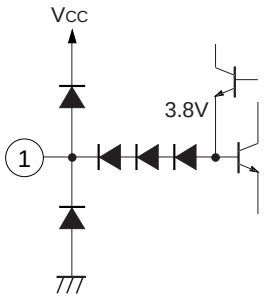


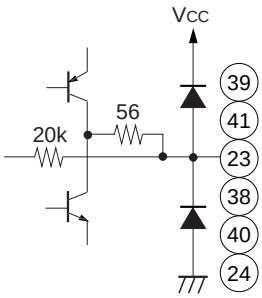
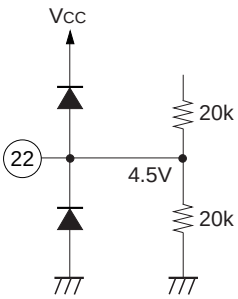
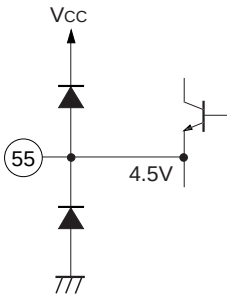
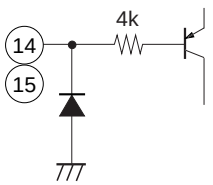
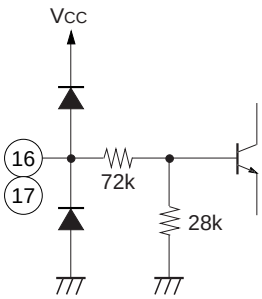
Pin Configuration

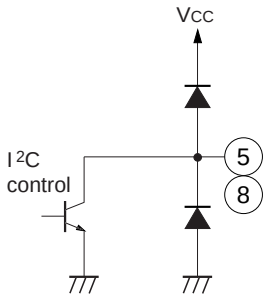
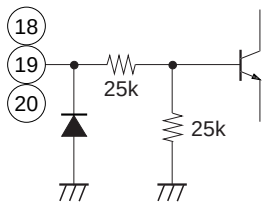
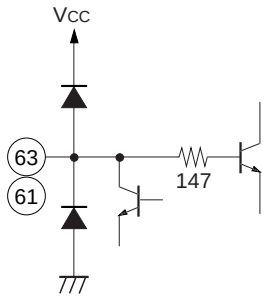
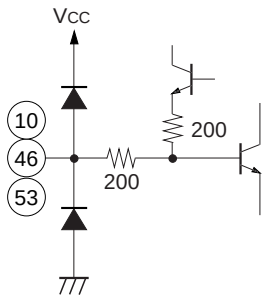


Pin Description

Pin No	Symbol	Pin voltage (V)	Equivalent circuit	Description
64 62 60	TV CVIN1 CVIN2	3.9		Video signal inputs.
58 56 54	Y1 Y2 Y3			Luminance signal inputs.
52 51 49	C1 C2 C3	4.5		Chrominance signal inputs.
25 30 29 28 27 26 32 37 36 35 34 33	LTV LV1 LV2 LV3 LV4 LV5 RTV RV1 RV2 RV3 RV4 RV5	4.5		Audio signal inputs.
9 43	CVOUT1 CVOUT2	3.8		Composite video signal outputs.
11 45	YOUT1 YOUT2	3.5		Luminance signal outputs.
13 47	COUT1 COUT2	4.5		Chrominance signal outputs.
2	TVOUT	3.8		TV signal group delayed output.

Pin No	Symbol	Pin voltage (V)	Equivalent circuit	Description
7 3	RGD1 RGD4	4.5		Group delay output to external filter.
6 4	RGD2 RGD3	4.5		Group delay inputs from external filter.
1	REXT	1.7		Pin connection for 39 kΩ group delay setting resistor. Pin voltage is group delay control dependent.
44	DVCC	9		Digital supply.
59	VVCC1			Video supply.
12	VVCC2			Video supply.
21	AVCC			Audio supply.
42	DGND	0		Digital ground.
57	VGND1			Video ground.
48	VGND2			Video ground.
31	AGND			Audio ground.

Pin No	Symbol	Pin voltage (V)	Equivalent circuit	Description
39 41 23 38 40 24	LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3	4.5		Audio signal outputs.
22	ABIAS	4.5		Internal reference bias for audio circuits. A capacitor is connected from this pin to GND.
55	VBIAS	4.5		Internal reference bias for video circuits. A capacitor is connected from this pin to GND.
14	SCL			I²C bus clock line.
15	SDA			I²C bus data line.
16	ADR			Slave address control.
17	MUTE			Audio signal output mute.

Pin No	Symbol	Pin voltage (V)	Equivalent circuit	Description
5 8	LO0 LO1			Open collector logic outputs.
18 19 20	MODE1 MODE2 MODE3			Function SCART inputs from SCART connectors.
63 61	TC1 TC2	5		Video detect time constant capacitor connection pins.
10 46 53	TRAP1 TRAP2 TRAP3	3.5		Connects trap circuit for subcarrier.

Note. Pin voltages indicated the approximate DC voltage levels with no signals inputs.

Electrical Characteristics (Ta=25 °C, V_{CC}=9 V unless stated.)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		8.5	9.0	9.5	V
Supply current	I_{CC}		40	75	100	mA

I²C (Operation of the I²C using either a 3.3 or 5 V supply on the external controller is possible)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	5	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	SDA 3 mA sink	0	—	0.4	V
Max. clock frequency	f_{SCL}		0	—	100	kHz
Min. waiting time for data change	t_{BUF}		4.5	—	—	µs
Min. waiting time for data transfer start	t_{HD}STA		4	—	—	µs
Low level clock pulse width	t_L		4.7	—	—	µs
High level clock pulse width	t_H		4	—	—	µs
Min. waiting time for start preparation	t_{SU}STA		4.7	—	—	µs
Min. data hold time	t_{HD}DAT		5	—	—	s
Min data preparation time	t_{SU}DAT		250	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Min. waiting time for stop preparation	t_{SU}STO		4.7	50	—	µs

Audio System

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gain		f=1 kHz, 1 Vp-p I/P.				
Channel 1/Channel 2	FGV_{A1}		–0.5	0	0.5	dB
Channel 3 (max.)	VGV_{AF}		–0.5	0	0.5	dB
Channel 3 (min.)	VGV_{A0}		–68	–63	–58	dB
–3 dB bandwidth	FBW_A	1 Vp-p I/P, 1 kHz serving as 0 dB ref.	—	1	—	MHz
Total harmonic distortion	THD	f=1 kHz, 0.5 Vp-p I/P with a 400 Hz to 80 kHz passband.	—	0.01	0.05	%
Input dynamic range	VDR_A	f=100 kHz, distortion at O/P less than 0.3 %	2.8	3.0	—	Vrms
Crosstalk	VCt_A	f=1 kHz, 1 Vp-p I/P, measure other outputs.	—	–90	–76	dB
Ripple rejection ratio	RR_A	f=100 Hz, 0.3 Vp-p signal applied to AVCC	—	–55	—	dB
Output DC offset	Voff	Offset voltage between I/P and O/P.	–30	0	30	mV
Input impedance	Zin		—	66	—	kΩ
Output impedance	Zout		—	20	—	Ω
Phase difference	VPD_A	f=1 kHz, 1 Vrms input. Compare left and right channels.	—	0.1	—	Deg
S/N ratio	S/N_A	f=1 kHz, 1 Vp-p input with a 20 Hz to 20 kHz passband. See note 1.	85	90	—	dB
Mute	Amute	f=1 kHz, 1 Vp-p input.	—	–90	–70	dB
Volume control		f=1 kHz, 0.5 Vp-p input.				
Fine	FEVC		0.6	1	1.4	dB
Coarse	CEVC		7.6	8	8.4	dB

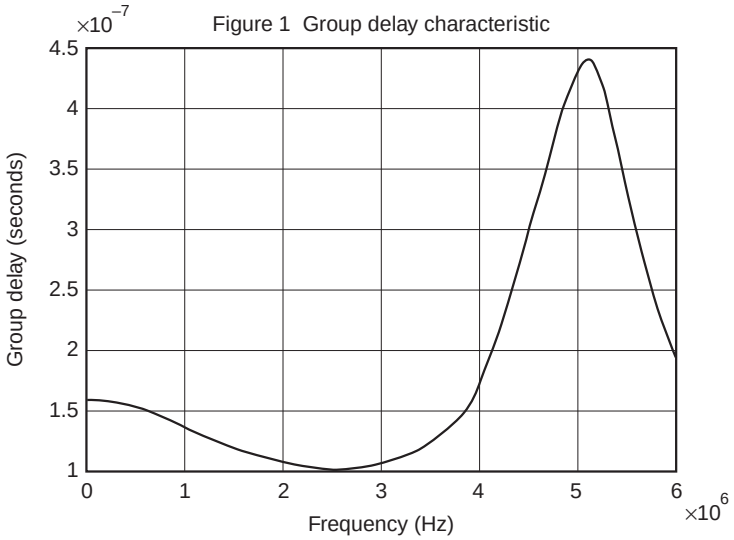
Audio System Notes

1. Channel 3 should be set at maximum volume.

Video System

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CVOUT1/2 gain	GV_{CV}	f=200 kHz, 0.3 Vp-p I/P.	5.5	6	6.5	dB
Y/COUT1/2 gain	GV_{YC}	f=200 kHz, 0.3 Vp-p I/P.	–0.5	0	0.5	dB
–3 dB bandwidth	F_{BWV1}	0.3 Vp-p I/P. See note 1.	15	20	—	MHz
–3 dB bandwidth Y/C mixer	F_{BWV2}	0.3 Vp-p I/P. See note 1.	10	15	—	MHz
Input level, TV and CVIN1	V_{RIV}	f=200 kHz, distortion at O/P less than 1 %, GD=OFF	1.4	—	—	Vp-p
Input dynamic range, CVIN2 and Y inputs.	V_{DRV}	f=200 kHz, distortion at O/P less than 1.0 %.	1.7	—	—	Vp-p
Crosstalk	V_{CTV}	f=4.43 MHz, 0.7 Vp-p I/P, measure other outputs.	—	–55	—	dB
S/N ratio	S/N_V	Ratio of 0.7 Vp-p white level to 'black line' noise. 5 kHz to 5 MHz passband. See note 2.	—	72	—	dB
Differential gain	DG	1.4 Vp-p 5 step staircase, modulated with 150 mVp-p 4.43 MHz.	–1.5	0	1.5	%
Differential phase	DP	As above.	–1.5	0	1.5	Deg
Group delay	GD	f=200 kHz, 0.7 Vp-p. See figure 1 and note 3.	200	250	350	ns
SYNC identification detected when	$SYNC_1$	See note 4.				
SYNC amplitude			100	—	—	mV
SYNC duty cycle		64 µs period.	91	—	—	%
not detected when						
SYNC amplitude			—	—	30	mV
SYNC duty cycle		64 µs period.	—	—	84	%

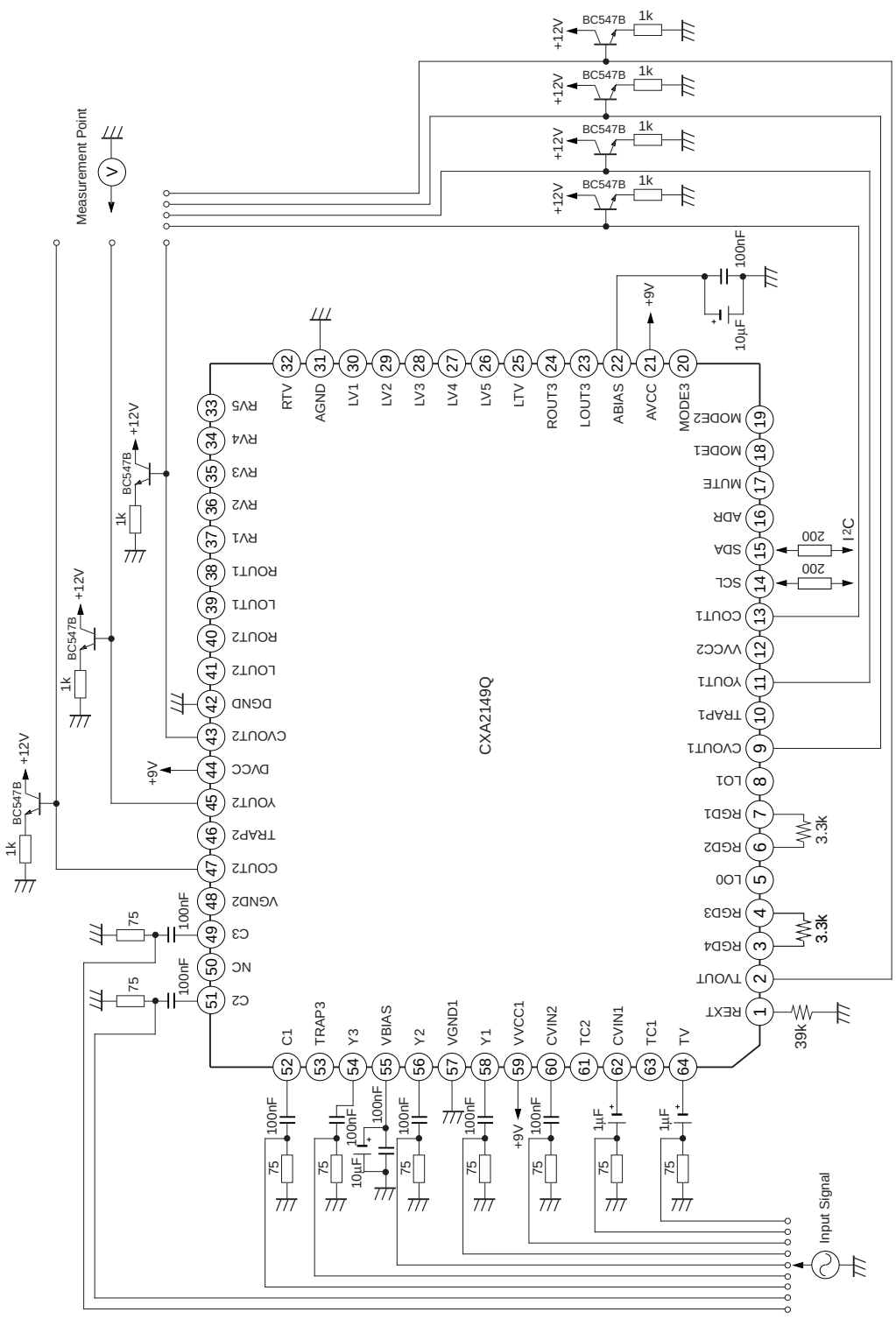
Figure 1 Group delay characteristic



Video System Notes

1. 200 kHz is taken to be 0 dB for the purpose of this measurement. Where applicable, the group delay function will be turned off to make this measurement.
2. Weighted using CCIR567.
3. This group delay characteristic, figure 1, is for the B, G specifications. It does not take into account the input and output delays inherent within the AV switch.
4. The sync detection circuits operate on the video sources that have been switched into the TV and CVIN1 channels, respectively.
   The internal SYNC discriminator circuit functions in the following way. The SYNC tip of the incoming video input is clamped to a fixed level and the signal is then compared in magnitude with an internal threshold voltage. If the signal is smaller than the threshold level the IC determines that the SYNC does not exist. Conversely, if the signal is found to be greater than the threshold then the duty cycle of signal is passed to the duty discrimination circuit. The discriminator circuit will identify whether the duty cycle of the signal is above 91 % at which point SYNC is detected, or below 84 % when SYNC is not detected.
   To prevent occasional video disturbances such as IF noise from the tuner causing malfunctioning of the SYNC detector, a time constant of approximately 14 line periods is applied during which the status of the SYNC detection is maintained.

Video Test Configuration

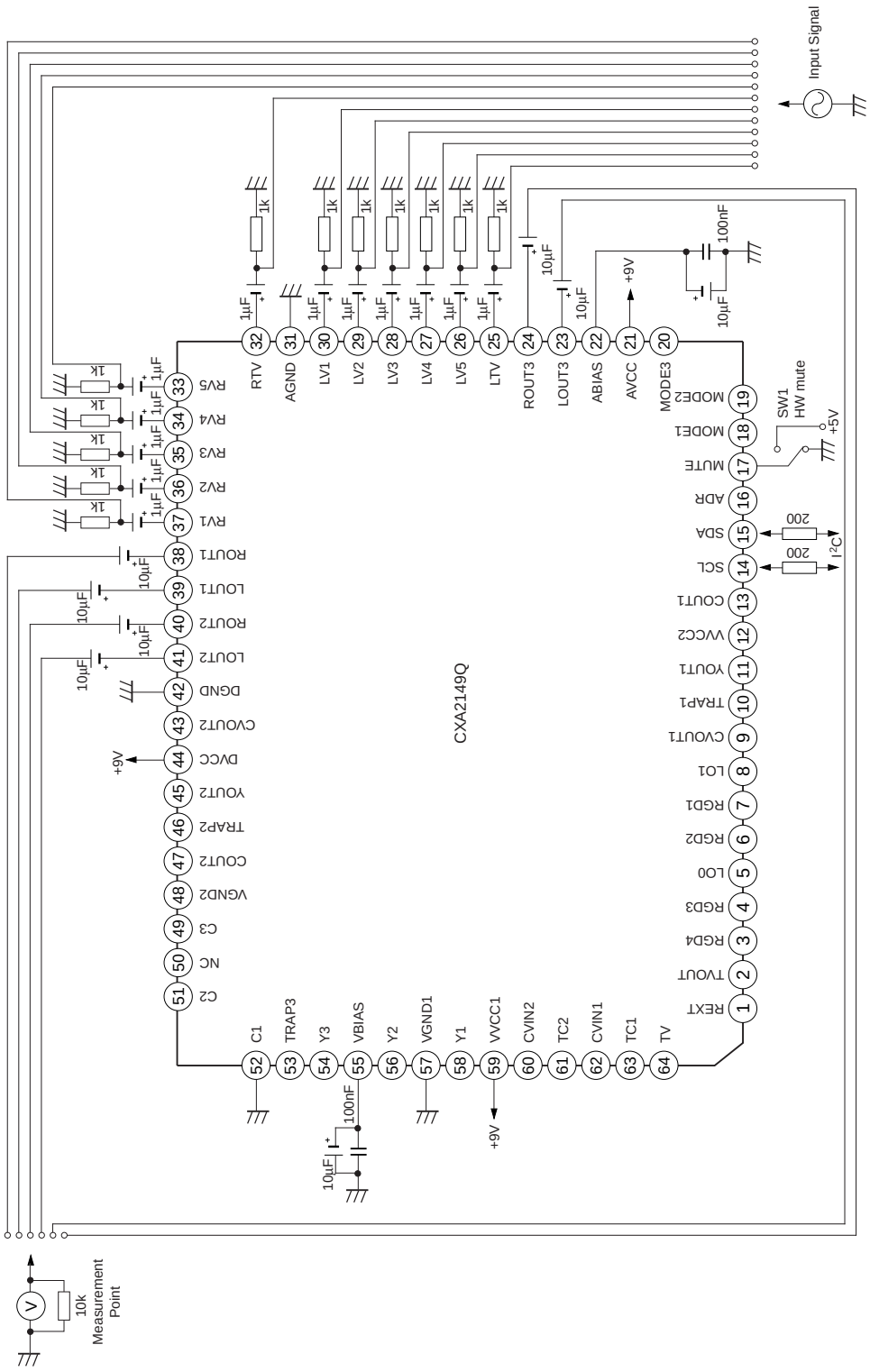


Video System Test Configuration (gain, dynamic range, bandwidth, signal to noise, crosstalk, differential gain, differential phase, sync ID, group delay)
Signals applied to inputs on pins 64, 62, 60, 58, 56, 54, 52, 51, 49
Output signal measured form pins 9, 11, 13, 43, 45, 47

Notes:

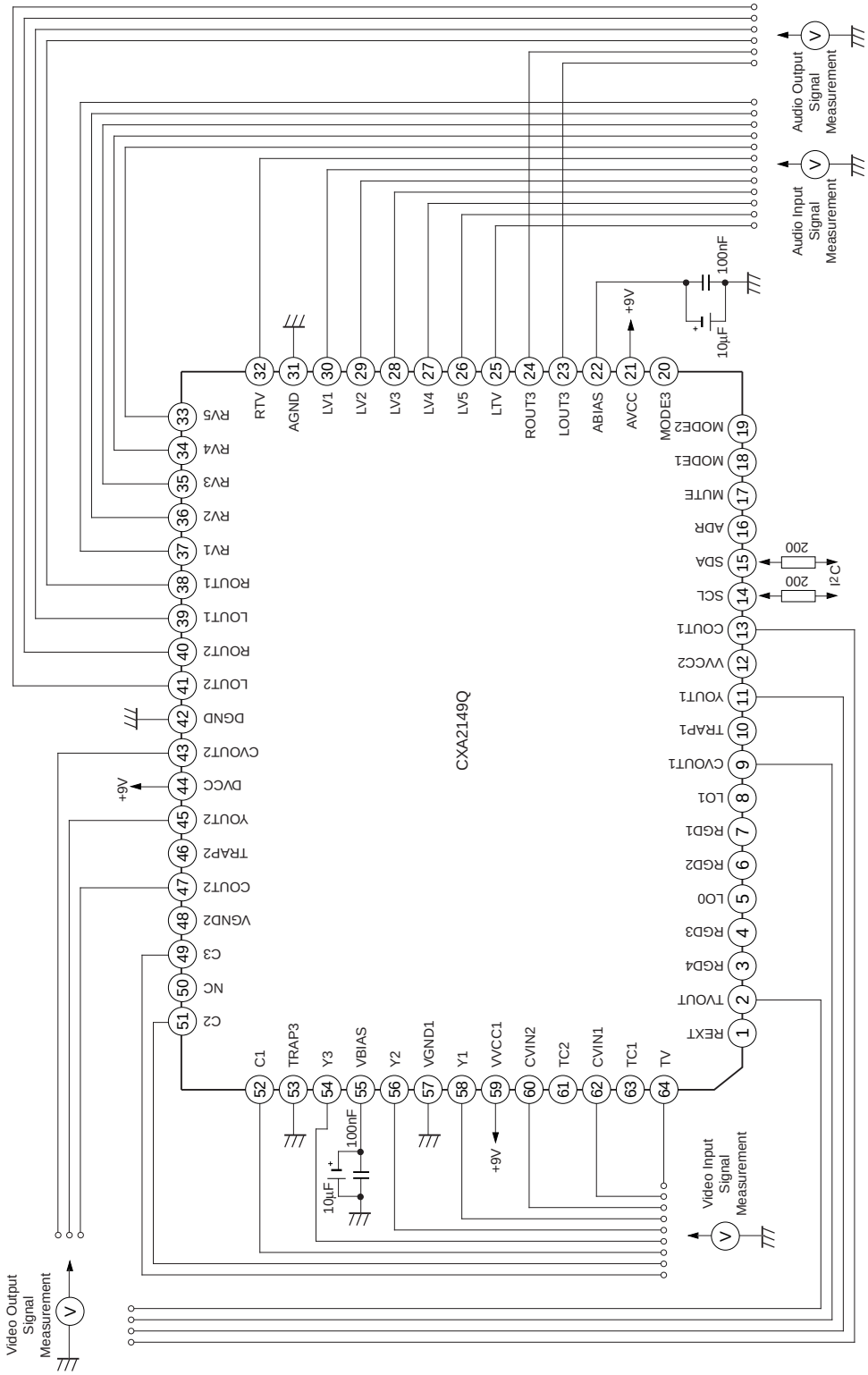
1) All +9 V supplies de-coupled close to supply pins 21, 44, 59 with 10 nF ceramic capacitor.
2) Refer to application schematic for external pin configuration of group delay and sync detect circuits.
3) Input signal assumes 75 ohm video driver. All video outputs are loaded with an emitter follower during tests.

Audio Test Configuration



Audio System Test Configuration (gain, dynamic range, signal to noise, crosstalk, distortion, volume control, ZCD and mute)
Signals applied to inputs on pins 25, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37
Output signal measured form pins 23, 24, 39, 40, 41
Notes:
1) All +9 V supplies de-coupled close to supply pins 21, 44, 59 with 10 nF ceramic capacitor.
2) When muting audio using hardware mute, SW1 is closed.

DC Test Configuration



DC Tests (Audio and Video System)

Notes:
1) All +9 V supplies de-coupled close to supply pins 21, 44, 59 with 10 nF ceramic capacitor.
2) All video outputs are loaded with an emitter follower during test.

I²C Bus Register Assignment

Status Register

Slave Address	1	0	0	1	0	0	ADR	R/W
Data1	SYNC1 Status	SYNC2 status	Mode Status					POR

Control Registers

Slave Address	1	0	0	1	0	0	ADR	R/W
Data1	GD1 Switch	GD2 Switch	CVOUT1			CVOUT2		
Data2	LO0 Control	LO1 Control	YCOUT1			YCOUT2		
Data3	ZCD Switch	AOUT3 Mute	AOUT1			AOUT2		
Data4	Group Delay					AOUT3		
Data5	AOUT3 Volume Control Coarse			AOUT3 Volume Control Fine			AOUT3L/R Switch	
Data6	GD1 Switch	GD2 Switch	SYNC1 Switch	SYNC2 Switch	*	*	*	*

Note.

1. The names CVOUT1, YCOUT1, AOUT1 etc., refer to the particular output or outputs that the register controls.
2. * Register undefined.

Status Register Descriptions

SYNC Detection Circuits Data1 Bit 6 (SYNC1) and Bit 7 (SYNC2)
Indicates whether a video signal is present or not. SYNC1 takes its input from TV and YOUT1. SYNC2 takes its input from CVIN1 and YOUT2.

SYNC1 or SYNC2 bit	Meaning
0	no SYNC
1	SYNC present

Mode Status Data1 Bits 1 to 5

The mode inputs from the SCART ports are driven at three different voltage levels to indicate the mode format of the port. These inputs are detected and then encoded to the status register in the following manner.

Input pin voltage	Meaning
0 to 2 V	Internal TV
4.5 to 7 V	External 16:9
9.5 to 12 V	External 4:3

Mode status bits	Meaning for MODE1	Meaning for MODE2	Meaning for MODE3
00000	Internal TV	Internal TV	Internal TV
00001	External 16:9	Internal TV	Internal TV
00010	External 4:3	Internal TV	Internal TV
00011	Internal TV	External 16:9	Internal TV
00100	External 16:9	External 16:9	Internal TV
00101	External 4:3	External 16:9	Internal TV
00110	Internal TV	External 4:3	Internal TV
00111	External 16:9	External 4:3	Internal TV
01000	External 4:3	External 4:3	Internal TV
01001	Internal TV	Internal TV	External 16:9
01010	External 16:9	Internal TV	External 16:9
01011	External 4:3	Internal TV	External 16:9
01100	Internal TV	External 16:9	External 16:9
01101	External 16:9	External 16:9	External 16:9
01110	External 4:3	External 16:9	External 16:9
01111	Internal TV	External 4:3	External 16:9
10000	External 16:9	External 4:3	External 16:9
10001	External 4:3	External 4:3	External 16:9
10010	Internal TV	Internal TV	External 4:3
10011	External 16:9	Internal TV	External 4:3
10100	External 4:3	Internal TV	External 4:3
10101	Internal TV	External 16:9	External 4:3
10110	External 16:9	External 16:9	External 4:3
10111	External 4:3	External 16:9	External 4:3
11000	Internal TV	External 4:3	External 4:3
11001	External 16:9	External 4:3	External 4:3
11010	External 4:3	External 4:3	External 4:3
11011 to 11111	Not used	Not used	Not used

Power on Reset Data1 Bit 0

After power on this bit will be set to 1 when DVCC, pin44, passes through a defined threshold level. The control registers are then defined as below. After the first write command the bit will be reset to 0.

CVOUT1=CVOUT2=1001, LO0 switch=LO1 switch=1, YCOUT1=YCOUT2=111,
ZCD switch=AOUT3 mute=1, AOUT1=AOUT2=111, Group delay=10000,
AOUT3=111, AOUT3 volume control coarse=AOUT3 volume control fine=111,
AOUT3L/R switch=00, GD1 switch=GD2 switch=1, SYNC1 switch=SYNC2 switch=1.

Control Register Descriptions

Video Inputs

CVOUT1 Data1 Bits 4 to 7

These bits select the input signal that will be output on the CVOUT1 pin.

CVOUT1	Input or function selected
0000	TV
0001	CVin1
0010	CVin2
0011	Y1
0100	Y2
0101	Y3
0110	Y1+C1
0111	Y2+C2
1000	Y3+C3
1001	Mute
1010 to 1111	Not used

CVOUT2 Data1 Bits 0 to 3

These bits select the input signal that will be output on the CVOUT2 pin.

CVOUT2	Input or function selected
0000	TV
0001	CVin1
0010	CVin2
0011	Y1
0100	Y2
0101	Y3
0110	Y1+C1
0111	Y2+C2
1000	Y3+C3
1001	Mute
1010 to 111	Not used

YCOUT1 Data2 Bits 3 to 5

These bits select the input signals that will be output on the YOUT1/COUT1 pins.

YCOUT1/2	Input or function selected
000	TV and Mute
001	CVin1 and Mute
010	CVin2 and Mute
011	Mute and Mute
100	Y1 and C1
101	Y2 and C2
110	Y3 and C3
111	Mute and Mute

YCOUT2 Data2 Bits 0 to 2

These bits select the input signals that will be output on the YOUT2/COUT2 pins.

YCOUT2	Input or function selected
000	TV and Mute
001	CVin1 and Mute
010	CVin2 and Mute
011	Mute and Mute
100	Y1 and C1
101	Y2 and C2
110	Y3 and C3
111	Mute and Mute

Audio Inputs

AOUT1 Data3 Bits 3 to 5
These bits select the input signal that will be output on the ROUT1 and LOUT1.

AOUT1 bits	Input or function selected
000	Mute
001	LTV and RTV
010	LV1 and RV1
011	LV2 and RV2
100	LV3 and RV3
101	LV4 and RV4
110	LV5 and RV5
111	Mute

AOUT2 Data3 Bits 0 to 2
These bits select the input signal that will be output on ROUT2 and LOUT2

AOUT2 bits	Input or function selected
000	Mute
001	LTV and RTV
010	LV1 and RV1
011	LV2 and RV2
100	LV3 and RV3
101	LV4 and RV4
110	LV5 and RV5
111	Mute

AOUT3 Data4 Bits 0 to 2
These bits select the input signal that will be output on ROUT3 and LOUT3

AOUT3 bits	Input or function selected
000	Mute
001	LTV and RTV
010	LV1 and RV1
011	LV2 and RV2
100	LV3 and RV3
101	LV4 and RV4
110	LV5 and RV5
111	Mute

Group Delay Switches Data1 Bit 7 (GD1 Switch) and Bit 6 (GD2 Switch)
Switch the respective group delay function on or off. GD2 switches on and off the group delay on the TV input and GD1 switches on and off the group delay on the CVIN1 input.

GD1 ro GD2 bit	Group delay function
0	off
1	on

Group Delay Control Data4 Bits 3 to 7
Used to control the variation in group delay. If no adjustment is required then set a value 10000.

Group Delay bits	Change in the Max. delay frequency
00000	–800 kHz
11111	+800 kH

AOUT3 Volume Control Coarse Data5 Bits 5 to 7
Selects the gain for the internal audio amplifiers in 8 dB steps.

Coarse bits	Gain of AOUT3 channels
000	0 dB
111	–56 dB

AOUT3 Volume Control Fine Data5 Bits 2 to 4
Selects sthe gain for the internal audio amplifiers in 1 dB steps.

Fine bits	Gain of AOUT3 channels
000	0 dB
111	–7 dB

AOUT3L/R Switch Data5 Bits 0 and 1
Controls which of channel 3’s left or right channels is output to LOUT3 and ROUT3, respectively.

AOUT3L/R bits	Output to LOUT3 and ROUT3
00	Normal
01	Left channel
10	Right channel
11	Inverted

AOUT3 Mute Switch Data3 Bit 6
Mutes the LOUT3 and ROUT3 channels at the electronic volume control output so that a click free audio channel change can take place.

AOUT3 mute bit	Meaning
0	Mute off
1	Mute on

The normal sequence for a click free channel change is as follows:-
1. Mute the channel 3 outputs (AOUT3 mute=1) with zero cross detection on (ZCD switch=1).
2. Change the channel 3 audio source, AOUT3L/R control.
3. Un-mute the channel 3 outputs still with zero cross detection on.

LO0 or LO1 Control Data2 Bit 7 (LO0 control) and Bit 6 (LO1 control)
Used to control the switching of the open collector outputs. The output transistor emitters are connected to digital ground. Each output is capable of sinking 1 mA.

LO0 ro LO1 bit	Collector output
0	Low impedance
1	High impedance

Zero Cross Detection Switch Data3 Bit 7
Switches the ZCD function on or off. When the ZCD is on, a volume control change or mute instruction sent via the I²C bus will only be implemented when a minimal, ie., zero cross, signal amplitude is detected.

ZCD bit	Meaning
0	ZCD off
1	ZCD on

SYNC ID Switches Data6 Bit 5 (SYNC1 Switch) and Bit 4 (SYNC2 Switch)
Switches the respective SYNC ID circuit to an input our output. SYNC1 switches between the TV input and YOUT1 output. SYNC2 switches between the CVIN1 input and YOUT2 output.

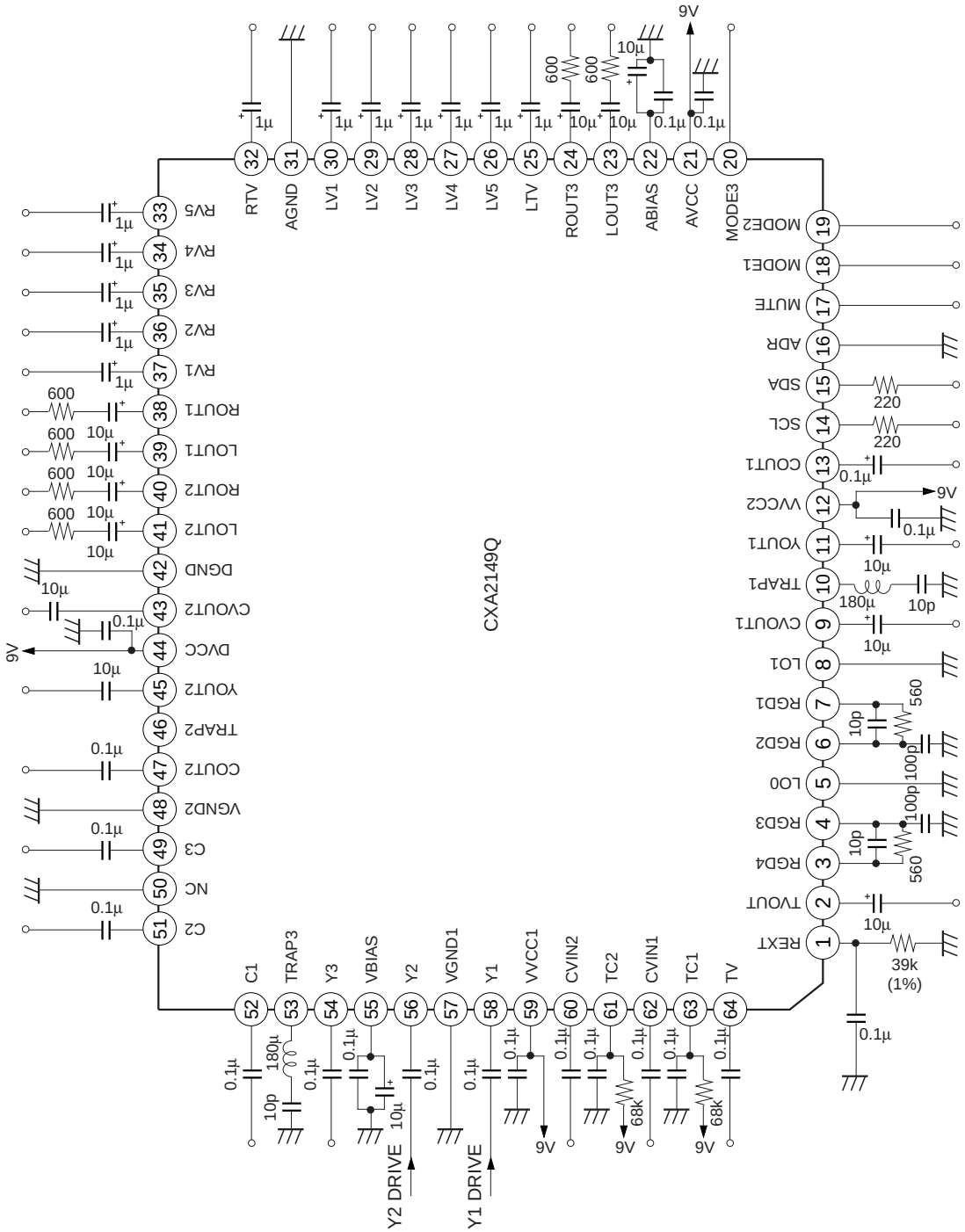
SYNC1 or SYNC2 bit	Input to SYNC ID
0	YOUT1 and YOUT2
1	YV and CVIN1

External Logic Inputs and Output
Hardware Mute
The hardware mute (pin 17) provided will mute all audio outputs when the pin voltage exceeds 2.5 V.
In this case the muting will be instantaneous.

SCART Modes
Three Mode inputs (pins 18, 19 and 20) are used to allow the format identification of up to three SCART ports. See the description for mode status.

LO0 and LO1 Logic Outputs
LO0 and LO1 are open collector output I²C controllable logic switch for any external switching functions an application may require. See the description for LO0 and LO1 control.

Application Diagram



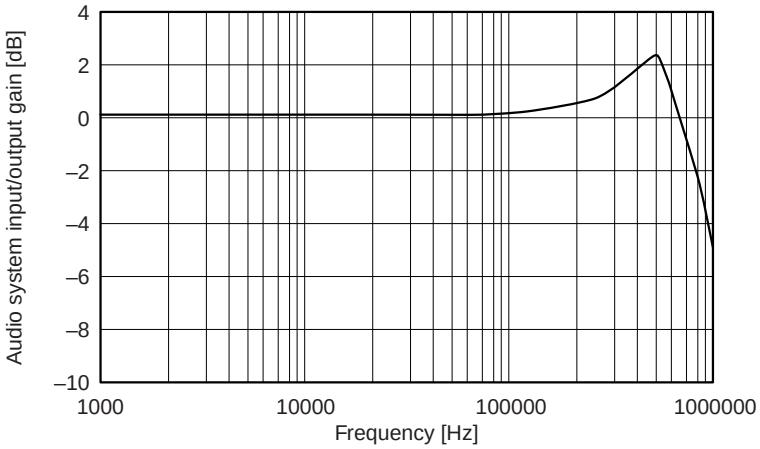
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Applications Notes (see circuits diagram on next page).

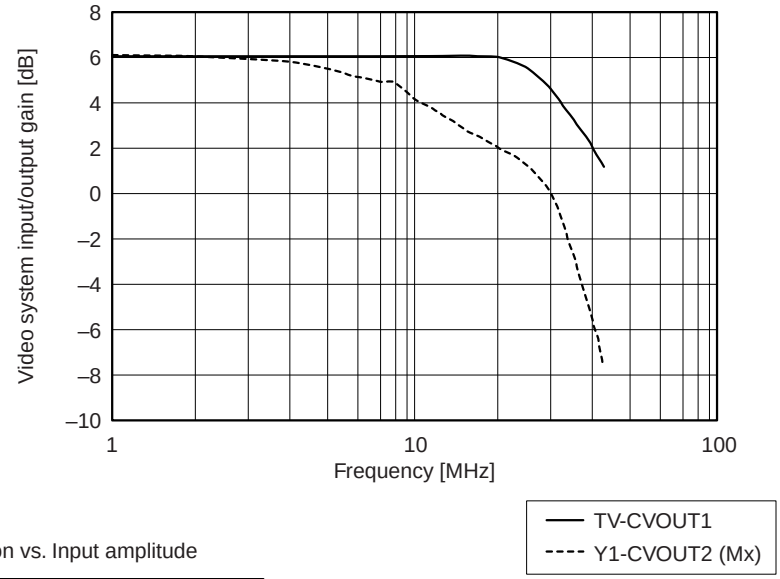
1. Care should be taken with polarity sensitive capacitors. The respective bias voltages for audio and video inputs and outputs are as follows.
   C1, C2, C3, COUT1 and COUT2 are biased at approximately 4.5 V.
   TV, CVIN1, CVIN2, Y1, Y2 and Y3 are SYNC tip clamped at approximately 3.9 V.
   CVOUT1, CVOUT2, TVOUT have their SYNC tip output at approximately 3.5 V.
   YOUT1, YOUT2 have their SYNC tip output at approximately 3.3 V.
   ABIAS and VBIAS are equal to approximately 4.5 V.
2. Connect ADR to V_{CC} when wishing to set the slave address to 92H.
3. Setting the MUTE pin to 2.5 V or more can mute the audio outputs.
4. TRAP1, TRAP2 and TRAP3 are set for a 3.58 MHz subcarrier. For a 4.43 MHz subcarrier typical values for the two traps would be 47 µ and 27 p, respectively. Values may require adjustment dependent upon the application. Each trap gives 6 dB's of attenuation at the desired frequency.
5. LO0 and LO1 connected to ground when not required.
6. Connect all NC to ground in application.

Example of Representative Characteristics

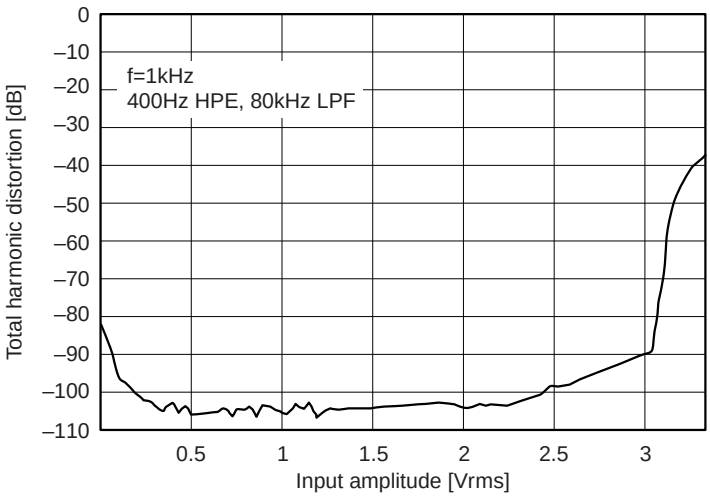
Typical audio system frequency response LTV-LOUT1



Video system typical frequency response

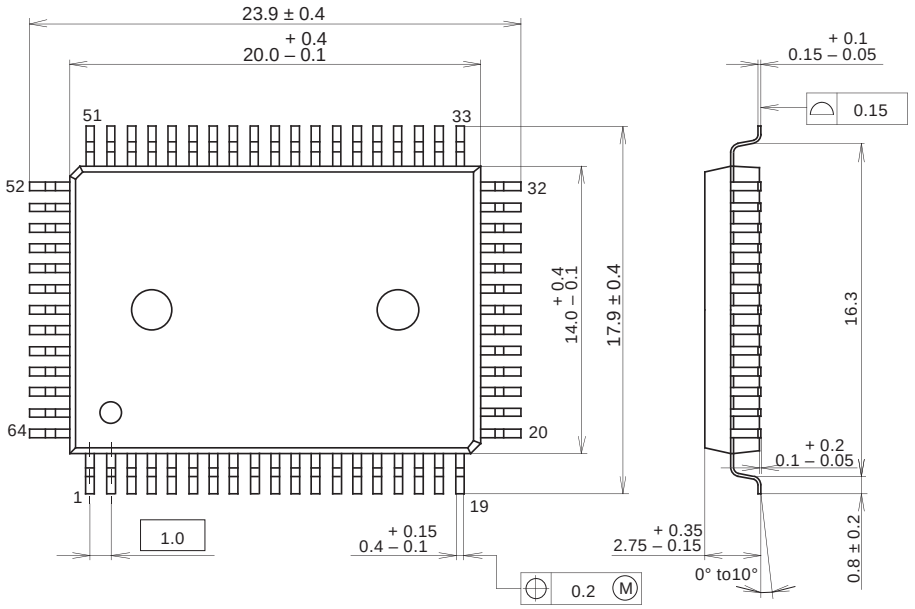


Typical audio system distortion vs. Input amplitude



Package Outline Unit : mm

64PIN QFP(PLASTIC)



SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g