SONY

CXA3018R

Demodulator for Satellite Receivers

Description

The CXA3018R is an IC designed for video signal demodulation for satellite broadcasting. This IC has most of the functions needed for demodulation, and provides stable video detection in combination with the CXA3008N.

Features

- PLL demodulation characteristics through built-in IF AGC
- Compatible with both NTSC and PAL
- Applicable for 8 systems worldwide
- Keyed AFT input pin to support MUSE reception
- Output pin for 1st AGC control
- Built-in video clamp circuit
- C/N detection circuit
- Single 5 V power supply operation

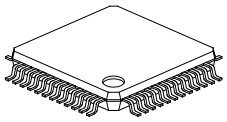
Applications

NTSC/PAL system satellite receivers, etc.

Structure

Bipolar silicon monolithic IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25 °C)

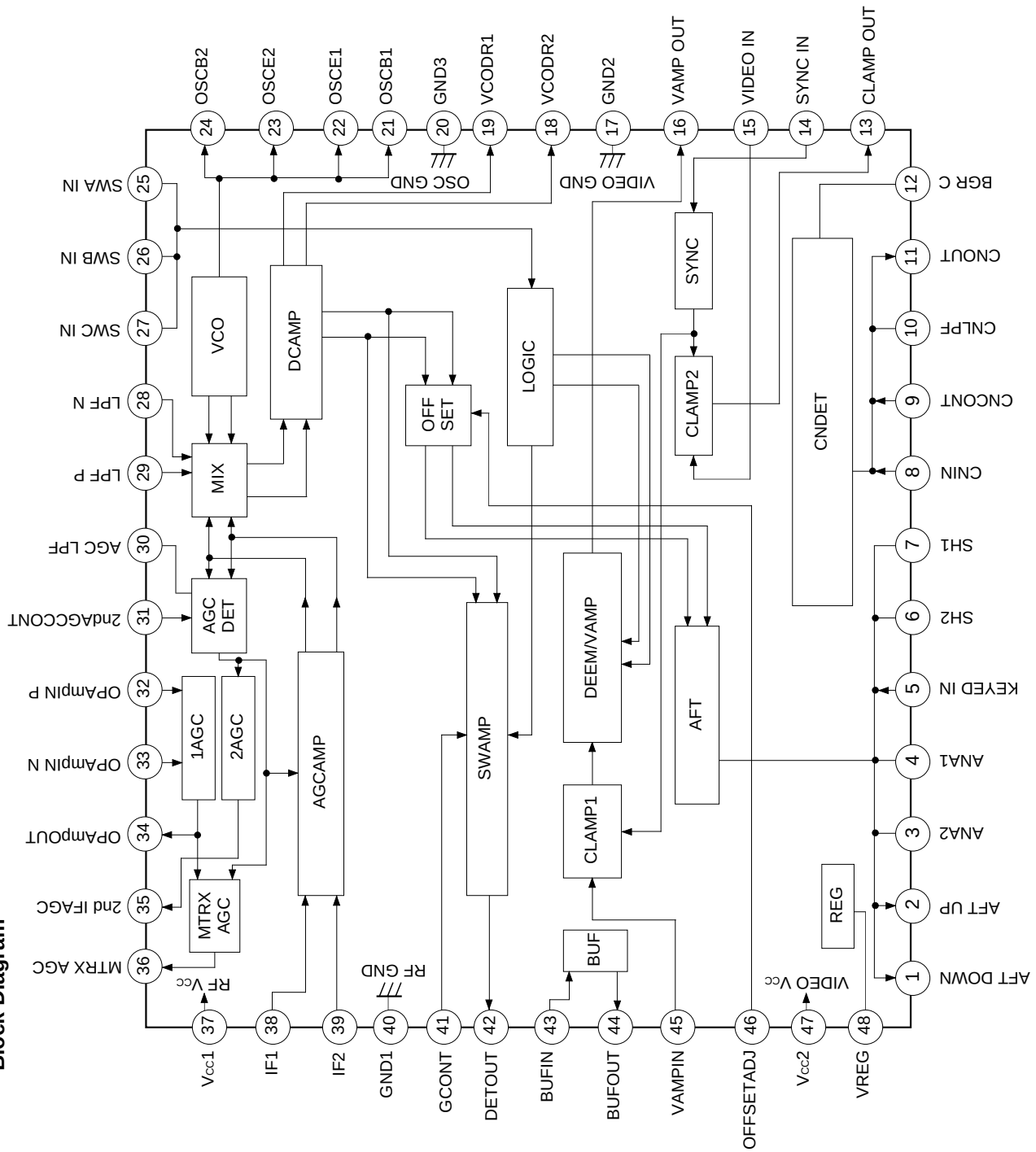
• Supply voltage	V_{CC}	–0.3 to 7.0	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Operating Supply Voltage

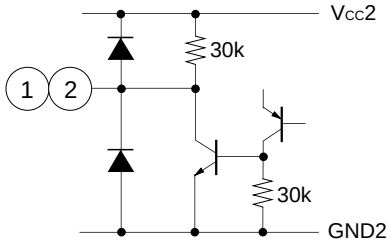
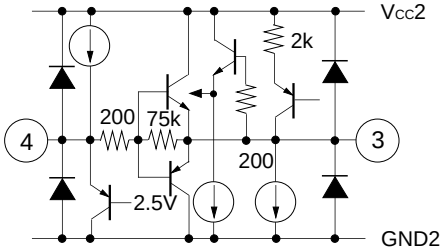
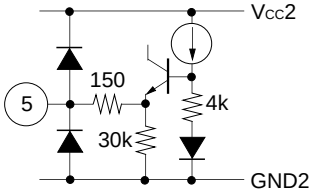
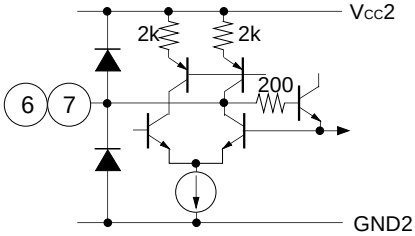
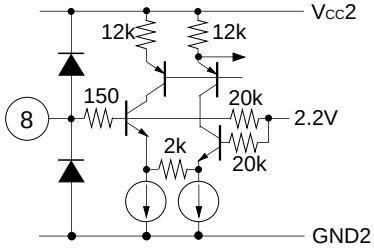
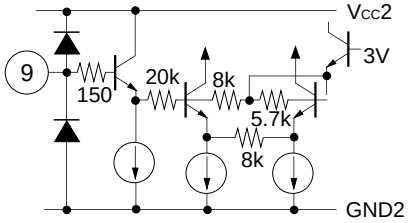
V_{CC}	4.50 to 5.50	V

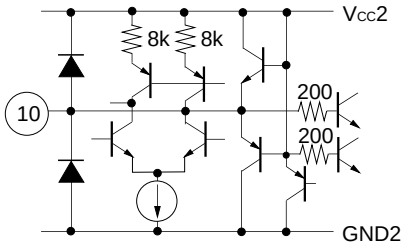
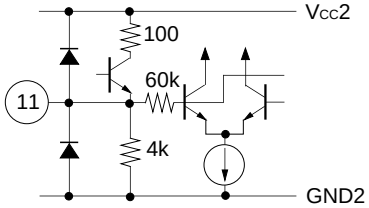
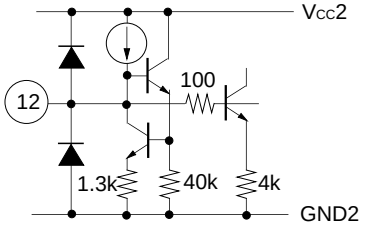
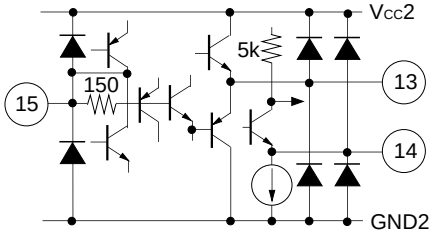
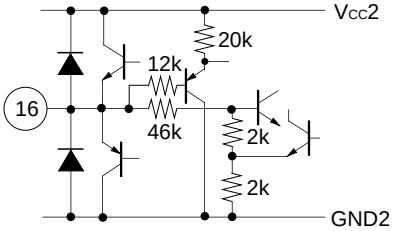
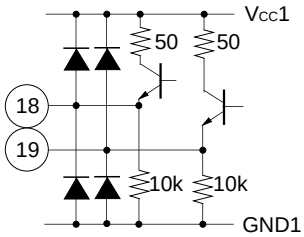
E95719-TE

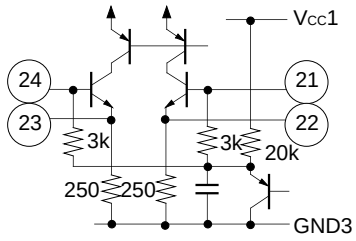
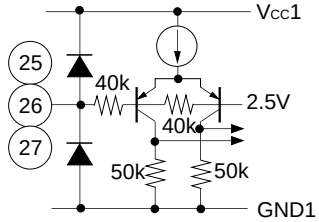
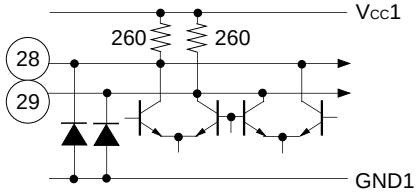
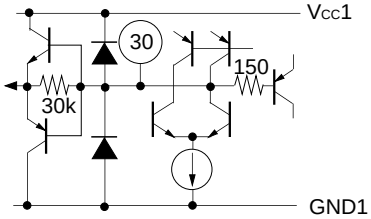
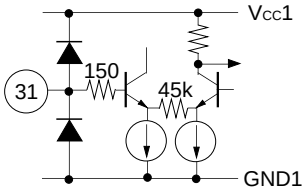
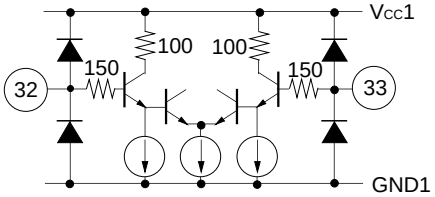
Block Diagram

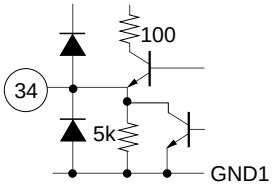
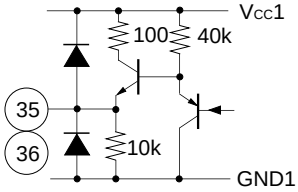
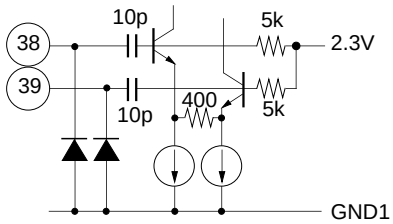
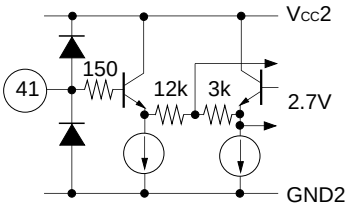
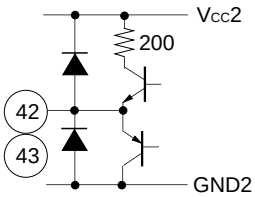
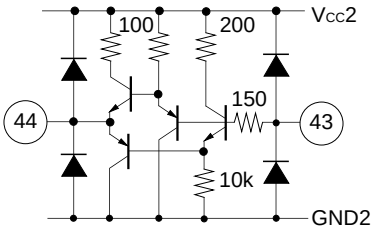


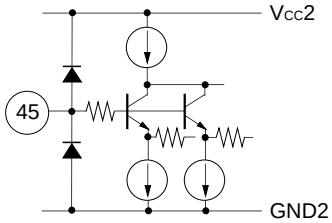
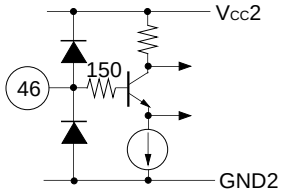
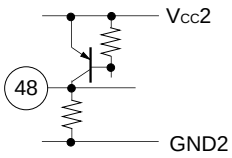
Pin Description

Pin No.	Symbol	Typical pin voltage DC	Typical pin voltage AC	Equivalent circuit	Description
1	AFT UP	4.9 V or 0.1 V			AFT block digital output pins.
2	AFT DOWN				
3	ANA2	1.3 V to 3.2 V			AFT block filter pin. Connect to Pin 4 with a 47 kΩ resistor and to GND with a 10 µF capacitor.
4	ANA1	3.1 V			AFT block reference output pin.
5	KEYED-IN	0.3V			AFT block keyed input pin.
6	SH2	3.0 V to 3.5 V			AFT block sample-and-hold signal output pins. Connect to GND with a 0.1 µF capacitor.
7	SH1	3.0 V to 3.5 V			
8	CNIN	2.1V	–50 to –20 dBm		C/N detection block signal input pin.
9	CNCONT	1.6 V to 4.4 V			C/N detection block gain adjustment pin.

Pin No.	Symbol	Typical pin voltage DC	Typical pin voltage AC	Equivalent circuit	Description
10	CNLPF	2.9 V			C/N detection block filter pin. Connect to GND with a 0.01 µF capacitor.
11	CNOUT	1.2 V to 3.7 V			C/N detection block output pin. Connect to GND with a 1nF capacitor.
12	BGR-C	0.9 V			C/N detection block reference output pin. Connect to GND with a 1 µF capacitor.
13	CLAMP OUT	2.0 V	1.0 Vp-p		Clamp block video output pin.
14	SYNC IN	1.4 V			Clamp block sync input pin.
15	VIDEO IN	2.0 V	1.0 Vp-p		Clamp block video input pin.
16	VAMP OUT	2.0 V	1.0 Vp-p		Video amplifier block video output pin.
17	GND2	0 V			GND pin.
18	VCODR2	2.0 V to 3.0 V			PLL detection output pins.
19	VCODR1				

Pin No.	Symbol	Typical pin voltage DC	Typical pin voltage AC	Equivalent circuit	Description
20	GND3	0 V			GND pin.
21	VCOB1	1.4 V			VCO constant setting pins.
22	VCOE1	0.7 V			
23	VCOE2	0.7 V			
24	VCOB2	1.4 V			
25	SW A-IN	—			Switching amplifier and video amplifier mode setting pins.
26	SW B-IN				
27	SW C-IN				
28	LPF-N	4.5 V			Mixer constant setting pins.
29	LPF-P				
30	AGC-LPF	2.9 V to 3.0 V			AGC detection block filter pin. Connect to GND with a 0.01 µF capacitor.
31	2ndAGC CONT	1.0 V to 3.0 V			AGC detection block gain adjustment pin.
32	OPAmp IN-P	—			AGC detection block 1st AGC input pins.
33	OPAmp IN-N				

Pin No.	Symbol	Typical pin voltage DC	Typical pin voltage AC	Equivalent circuit	Description
34	OPAmp OUT	0.3 V or 3.5 V			AGC detection block 1st AGC digital output pin.
35	2nd IF AGC	2.0 V to 3.0 V			AGC detection block 2nd AGC analog output pin.
36	MTRX-AGC	2.0 V to 3.5 V			AGC detection block MTRX-AGC analog output pin.
37	Vcc1	5 V			Positive power supply pin.
38	IF1				AGC block IF input pins.
39	IF2				
40	GND1	0 V			GND pin.
41	GCONT	2.0 V to 4.0 V			Switching amplifier block gain adjustment pin.
42	DETOUT	2.45 V	200 mVp-p		Switching amplifier block video output pin.
43	BUFIN	2.0 V	200 mVp-p		BUFF video input pin.
44	BUFOUT				BUFF video output pin.

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
45	VAMPIN	2.5 V	100 mVp-p		Video amplifier block video input pin.
46	OFFSET ADJ	2.0 V to 4.0 V			AFT block offset adjustment pin.
47	Vcc2	5 V			Positive power supply pin.
48	VREG	4.1 V			Reference voltage output pin. Connect to GND with a 10 µF capacitor.

Electrical Characteristics

DC Characteristics (Ta = 25 °C, V_{CC} = 5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Current consumption	37, 47	ICC		70	100	130	mA
2	AGC-1 High output voltage	34	VAGC1H	Pin 31=3.0V	3.0	3.5	3.7	V
3	AGC-1 Low output voltage	34	VAGC1L	Pin 32=2.5V	0.1	0.3	1.0	
4	AGC-2 High output voltage	35	VAGC2H	Vin=–10dBm, Pin 31=3.0V	2.5	2.9	3.3	
5	AGC-2 Low output voltage	35	VAGC2L	Vin=–60dBm, Pin 31=3.0V	1.5		2.6	
6	AGC-MTRX High output voltage	36	VMTRH	Vin=–10dBm, Pin 31=3V, Pin 32=2.5V	3.0	3.5	3.7	
7	AGC-MTRX Low output voltage	36	VMTRL	Vin=–60dBm, Pin 31=3V, Pin 32=2.5V	1.5	2.3	2.7	
8	VCODR1/2 output voltage	18, 19	VVCD	400MHz input	2.0	2.5	3.0	
9	VCODR1/2 driver current capacitance	18, 19	IVCD	Load resistance R_L = 1 kΩ	2.0	2.5	—	mA
10	VREG output voltage	48	VREG		3.9	4.15	4.4	V

AC Characteristics (AGC) (Ta = 25 °C, V_{CC} = 5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
11	IF input frequency	38, 39	fin		—	400	—	MHz
12	IF input level	38, 39	Vin	One amplitude at balance input	–60		–10	dBm
13	1st AGC change point (input level)	34	AGC1	Pin 31=2.5V, Pin 32=2.5V		–40		
14	1st AGC control sensitivity	34	ΔAGC1	Slope of variation	—	0.8	—	V/dB
15	1st AGC adjustment sensitivity	34	AGC1/V	Variation of change point / Pin 32 DC variation	—	42	—	dB/V
16	2nd AGC control sensitivity	35	ΔAGC2	Slope of variation	–24	–18	–12	mV/dB
17	2nd AGC adjustment sensitivity	35	AGC2/V	Variation of change point / Pin 31 DC variation	3	11	18	dB/V
18	AGC-MTRX control sensitivity	36	ΔMTRX	Slope of variation	—	0.3	—	V/dB

AC Characteristics (PLL) (Ta = 25 °C, V_{CC} = 5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
21	VCO conversion sensitivity		ß	∗1	32	37	42	MHz/V
22	VCO oscillator frequency		fosc	∗1	—	400	—	MHz
23	PLL capture range		CAP	Sum of the positive / negative ∗1	—	40	—	
24	DETOUT level	42	VOUT	Dev.=17MHzpp	0.60	0.68	0.76	Vp-p
25	DETOUT level variable range	42	VdB	VOUT=0dB, p41=±0.5V	–3.0	—	2.5	dB
26	GCONT adjustment sensitivity	42	ΔVOUT	Output level / Pin 41 DC variation	5	7	9	dB/V
27	DETOUT frequency response (8 MHz)	42	VOUTf	8MHz/1MHz	–1.0	0.0	1.0	dB

∗1 Varies according to external constant (coil, varicap).

This characteristic is for NTSC. Also, operates with 480 MHz for PAL.

AC Characteristics (Video) (Ta = 25 °C, V_{CC} = 5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
31	CLAMP OUT output level	13	VCO	Dev.=17MHzpp	—	1.0	—	Vp-p
32	CLAMPOUT frequency response	13	VCOf	VAMPIN input 5MHz / 1MHz	–1.6	0.0	1.6	dB
33	IF → clamp output frequency response (5 MHz)	13	VCOfA	IF input 5MHz/1MHz	–2.5	0.0	2.5	
34	IF → clamp output DG	13	DGA	IF input ∗1	0	1.8	5	%
35	IF → clamp output DP	13	DPA	IF input ∗1	–4	0	4	deg
36	fsc beat suppression	13	IMA	IF input	40	45	—	dB
37	Dispersal elimination ratio	13	DISP1	IF input	40	45	—	
38	CLAMPOUT residual dispersal distortion	13	DISP2	IF input	—	0.5	1.0	IRE
39	IF → clamp output S/N	13	CSN	IF input	55	64	—	dB

∗1 Varies according to external constant (coil, varicap).

AC Characteristics (AFT/CN) (Ta = 25 °C, V_{CC} = 5 V, See the Electrical Characteristics Measurement Circuit.)

∗1: Input voltage VCNIN enable to adjust output voltage VCNO = 2 V

	Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
41	AFT f0 adjustment range		fAFT	Offset from 2nd IF	–5	—	+5	MHz
42	AFToffset adjustment sensitivity		fAFT/V	f0 variation / Pin 46 DC variation	–18	–9	–3	MHz/V
43	AFTdead zone width		fAFT/D		90	180	360	kHz
44	AFTUP/AFTDOWN Low	1, 2	AFTL		0	0.1	0.4	V
45	AFTUP/AFTDOWN High	1, 2	AFTH		4.7	4.9	V_{CC}	V
46	CN detection level	11	VCNO	–40dB input (Pin 9=3V)	1.6	2.0	2.4	V
47	CN adjustment range	11, 9	VCNOW	–40dB input (Pin 9=2 to 4V) Variation from VCNO	–0.15	—	0.25	V
48	CN sensitivity	11, 8	ΔVCN	CNOUT voltage / CNIN input level (–50 to –30dBm)	–60	–50	–40	mV/dB
49	CN adjustment sensitivity	11, 8	VCN/Vc	Input level variation / Pin 9 DC variation In case of adjusting output voltage VCNO=2 V	–10	–7.5	–5	dB/V

SWAMP Control Table

Gain control applicable to satellite receivers

	Pin 25 SWA	Pin 26 SWB	Pin 27 SWC	Format	Satellite	Deviation (MHz/V)	Gain deviation against BS (dB)	Remarks
1	H	H	H	NTSC	BS	17.0	0.0	positive
2	H	H	L		JC-SAT	15.8	0.7	positive
3	H	L	H		SCC	18.0	–0.5	positive
4	H	L	L		ASIA-SAT (NTSC)	21.6	–1.8	negative
5	L	H	H	PAL	COPER NICUS	22.5	–2.3	positive
6	L	H	L		U-TEL SAT	25.0	–3.2	positive
7	L	L	H		ASTRA	16.0	0.5	positive
8	L	L	L		ASIA-SAT (PAL)	20.0	–1.4	negative

Control Table

Pin No.	Symbol	LOW			HIGH			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.		
5	KEYEDIN	0.0		0.1	0.3			V	AFT clamp circuit ON when pulse input is Low during keyed AFT
14	SYNCIN			0.8				V	Clamp circuit ON when Low
25	SWA	0.0		2.0	3.0		V_{CC}	V	Gain SW applicable to satellite receivers
26	SWB	0.0		2.0	3.0		V_{CC}	V	
27	SWC	0.0		2.0	3.0		V_{CC}	V	

Description of Operation

This IC consists of the following six function blocks. First, the signal flow is explained briefly, followed by the functions of each block.

(1) AGC block
(2) FM demodulation block
(3) SWAMP block of video signal processor
(4) CLAMP & VAMP blocks of video signal processor
(5) AFT block
(6) C/N detection block

The 2nd IF differential signal input to Pins 38 and 39 passes through the AGC block to stabilize the signal level and is then input to the FM demodulation block. The FM demodulated signal is then input to the SWAMP and AFT blocks of video signal processor.
The SWAMP block outputs the detective signal from DETOUT after adjusting the gain to support worldwide video systems. The detective signal output becomes the final video signal by being input to the CLAMP & VAMP blocks through an external de-emphasis time constant block and an LPF. Also, part of the detective signal output is input to the C/N detection block through an external BPF.
The AFT block detects the frequency lag of the 2nd IF signal by the voltage value of the detective signal output, and outputs a command signal to the external frequency conversion block in order to correct the local frequency.
The C/N detection block detects noise outside the video band and has a voltage output to indicate the C/N noise level that is input (1st IF signal) to the receiver.

(1) AGC block

The 2nd IF differential signal is input to Pins 38 and 39 to fix the signal level with the AGC block. Connect a capacitor which fixes the AGC loop time constant to Pin 30, and apply an adjustment voltage at the output setting level of this AGC (2nd AGC) to Pin 31. The 2nd AGC control voltage is output from Pin 35. Apply the starting level adjustment voltage of the 1st AGC for the 1st IF to Pin 32. Input the Pin 35 output to Pin 33 through a 10 kΩ resistor and the Pin 36 output through a 0.1 µF capacitor. Output the 1st AGC control voltage from Pin 34, and output the voltage obtained by adding the 1st AGC control voltage of the Pin 34 output to the 2nd AGC control voltage of the Pin 35 output from Pin 36.

(2) FM demodulation block

The FM demodulation block is a PLL demodulator which consists of an oscillator (OSC), phase discriminator and DCAMP. Connect the oscillator resonance circuit to Pins 21 to 24 and the loop filter to Pins 28 and 29. The DCAMP differential output comes from Pins 18 and 19, and this output is used as the drive voltage for the varicap that comprises the oscillator.

(3) SWAMP block of video signal processor

The SWAMP block of video signal processor amplifies only gains selected by LOGIC and outputs detective signal output from Pin 42. The output from Pin 42 is output externally as the DETOUT (detective output) signal. This signal enters an internal buffer from Pin 43 through the de-emphasis time constant block, and is then output again from Pin 44. The Pin 44 BUFOUT output is input to VAMPIN after the high frequency component outside of the video band is removed by an external LPF.
LOGIC controls SWAMP according to corresponding satellite switching commands (3 bits) input from Pins 25 to 27. In addition, the SWAMP gain is finely adjusted by applying the DETOUT level adjustment voltage from Pin 41.

(4) CLAMP & VAMP blocks of video signal processor

The signal input from VAMPIN is sync-tip clamped by CLAMP1 and input to the VAMP block. VAMP selects NTSC or PAL gain according to the NTSC/PAL switching commands from the LOGIC block. The gain is output from Pin 16 after being amplified to the proper level (1 Vp-p for sync tip to 100 % WHITE). The Pin 16 output signal is input to CLAMP2 from Pin 15 where it is sync-tip clamped again. CLAMP1 & 2 are enabled by the CLAMP pulse which is input to Pin 14. The CLAMP1 & 2 blocks eliminate the triangular wave components (15 to 30 Hz) which overlap with the video signal for the energy diffusing signal. The final video signal is output from Pin 13.

(5) AFT block

This block detects frequency error in the 2nd IF signal as a voltage displacement from the FM demodulation signal which is input to the AFT block, and outputs the two values of High (5 V) or Low (0 V) from Pins 1 and 2. High indicates the frequency change command (active-High). Furthermore, High output from both pins indicates the dead zone. Connecting an LPF capacitor to Pin 3, applying the reference voltage to Pin 4, and connecting a resistor between Pins 3 and 4 changes the AFTAMP gain, thereby allowing the dead zone width to be changed. Input the keyed pulse for keyed AFT to Pin 5. The Pin 5 voltage should be 0 V during mean value AFT. Connect sample-and-hold capacitors to Pins 6 and 7. Apply the offset adjustment voltage to Pin 46 to cancel the effects of the DC offset inside the IC.

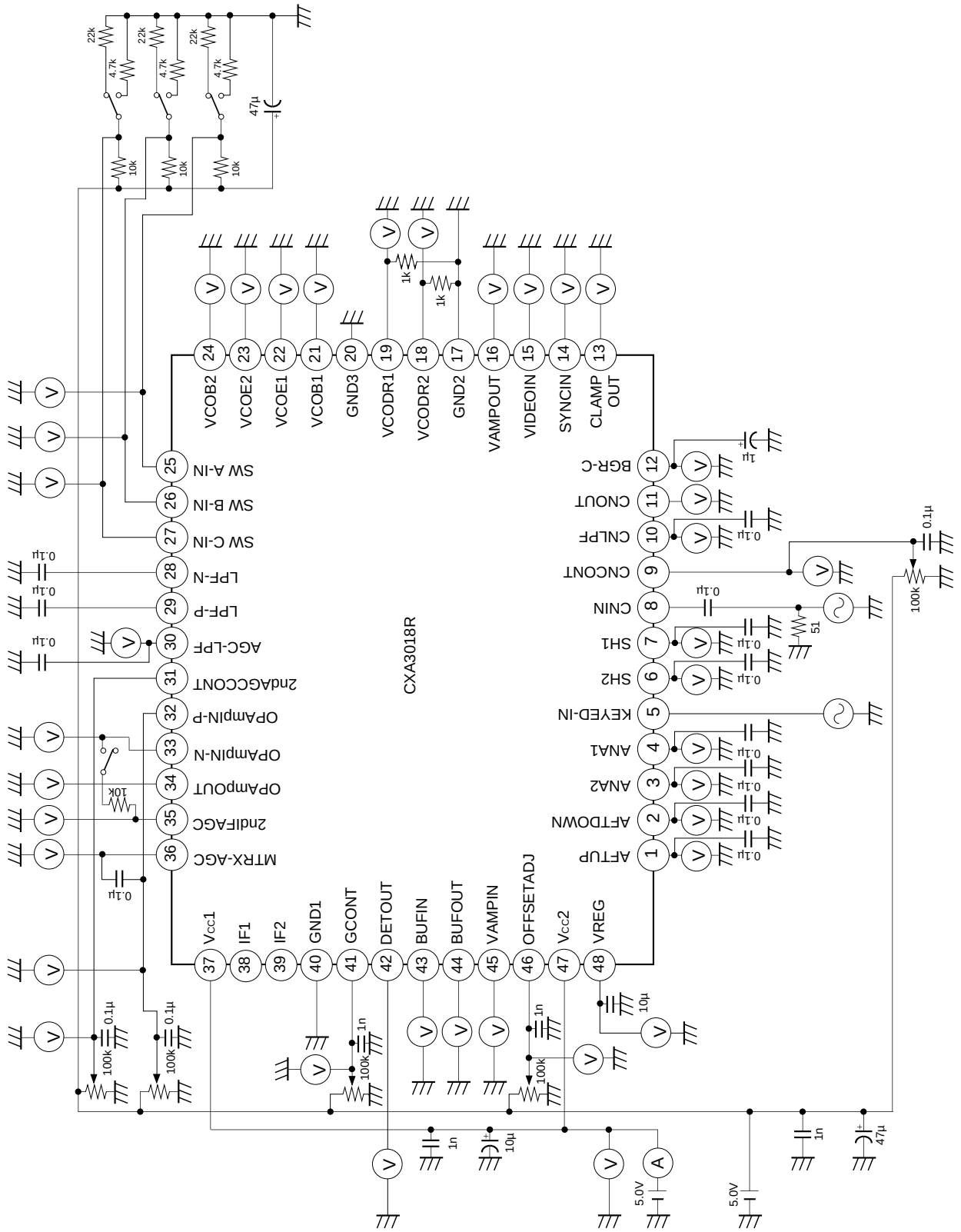
(6) C/N detection block

Extract the noise component from the DETOUT signal output from Pin 42 with an external BPF and input it to the C/N detection block from Pin 8. Output the C/N conversion output from Pin 11. Apply the C/N detection adjustment voltage to Pin 9, connect an LPF capacitor to Pin 10, and connect a decoupling capacitor for the voltage source for correcting temperature characteristics to Pin 12.

(7) Other

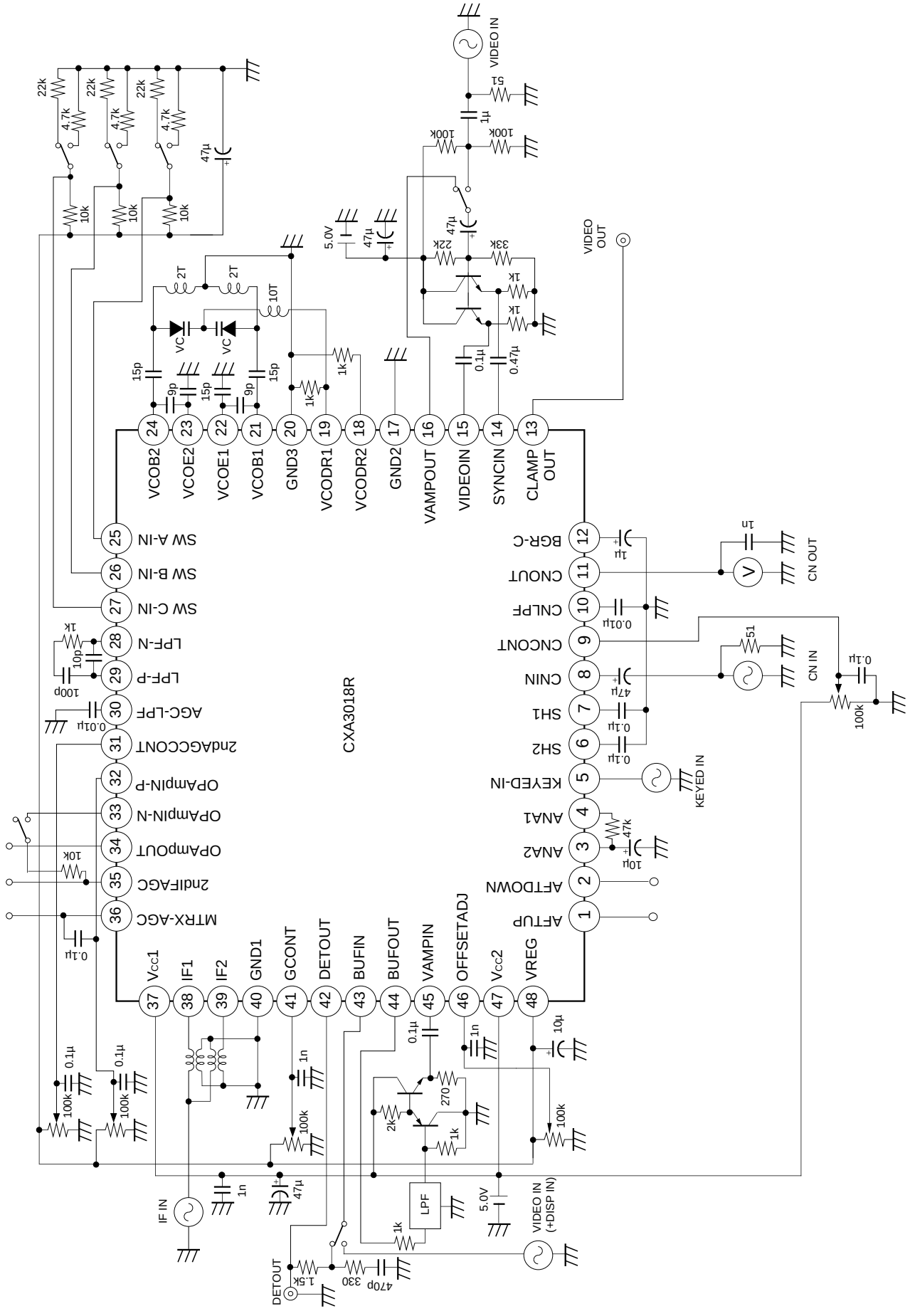
Connect a capacitor to cancel the regulator voltage noise to Pin 48, and use this output as the reference voltage for internal adjustment.

Electrical Characteristics Measurement Circuit 1

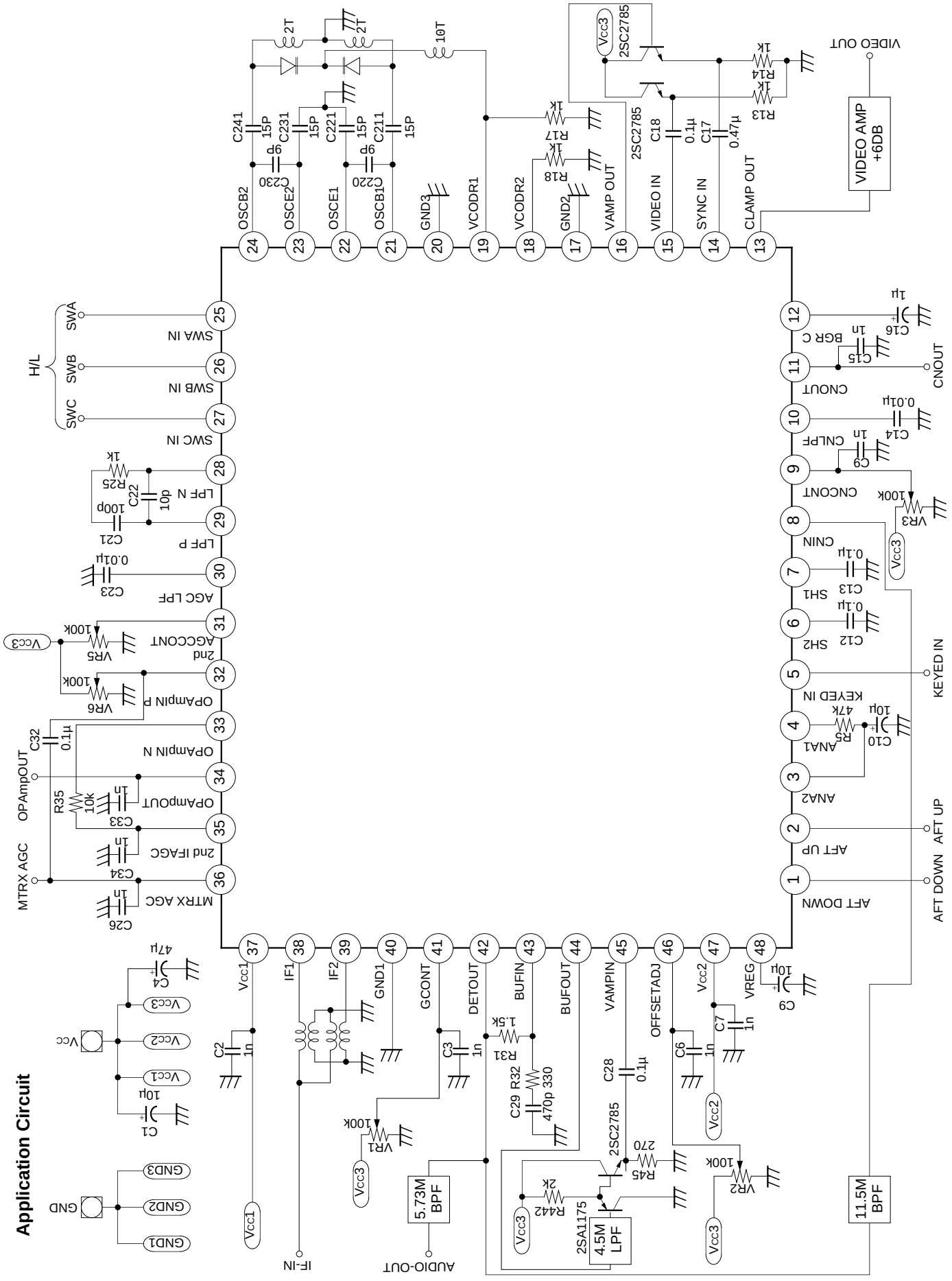


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Electrical Characteristics Measurement Circuit 2

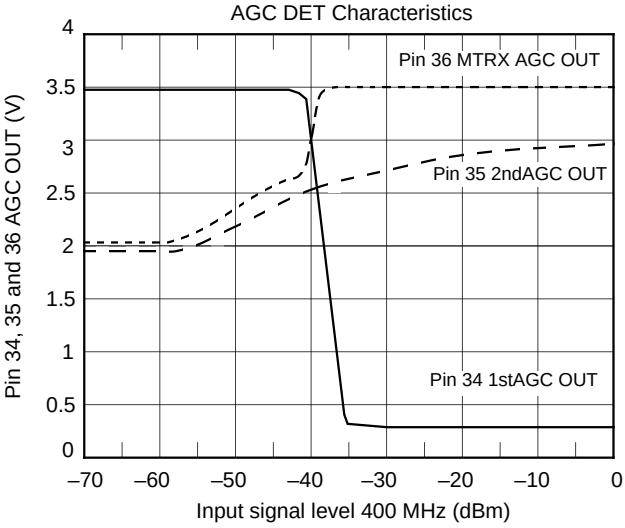


Application Circuit

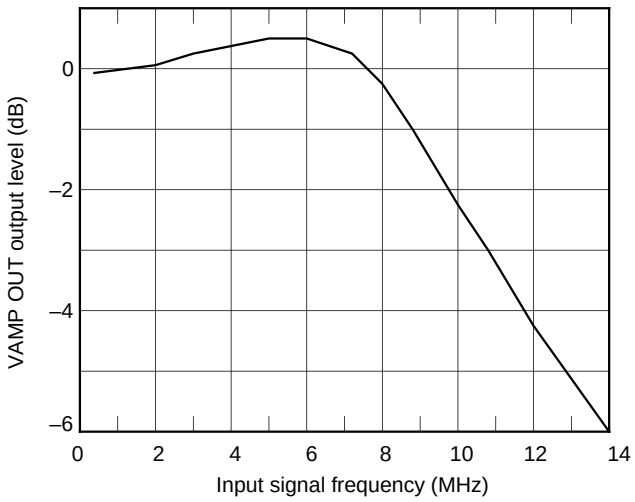


Pin 31 (2ndAGCCONT)=2.5V
Pin 32 (OPAmpIN-p)=2.5V

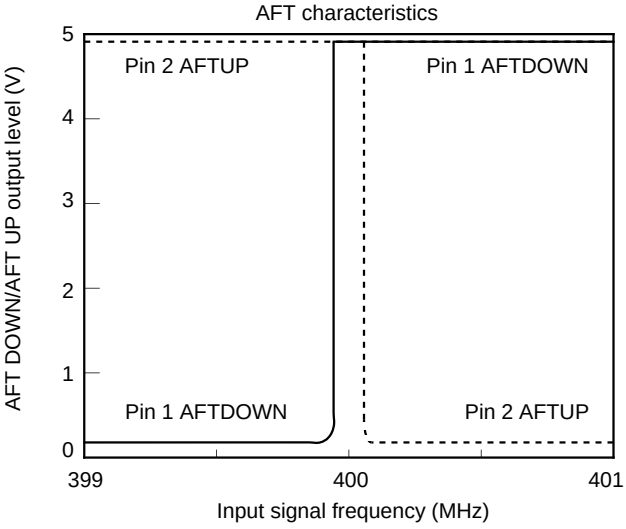
AGC DET Characteristics



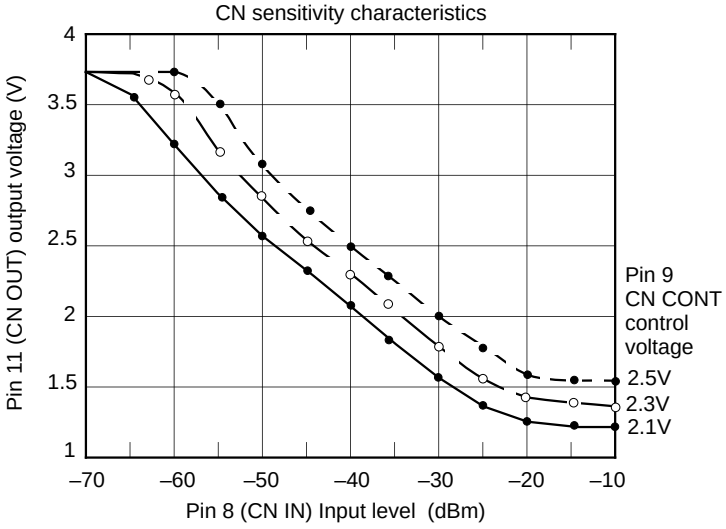
VAMP frequency responce characteristics



AFT characteristics

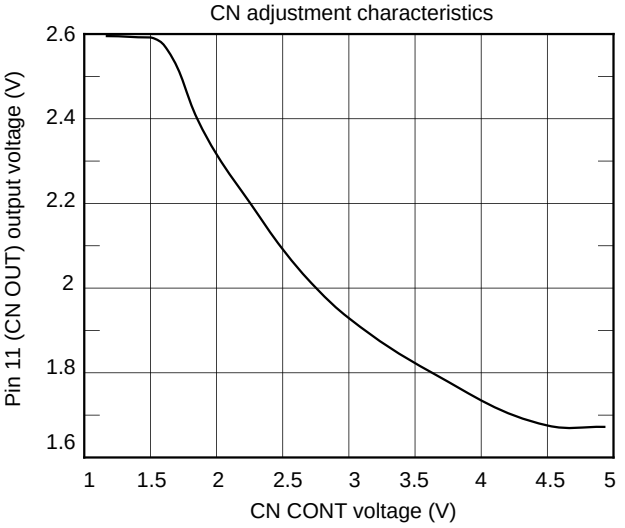


CN sensitivity characteristics



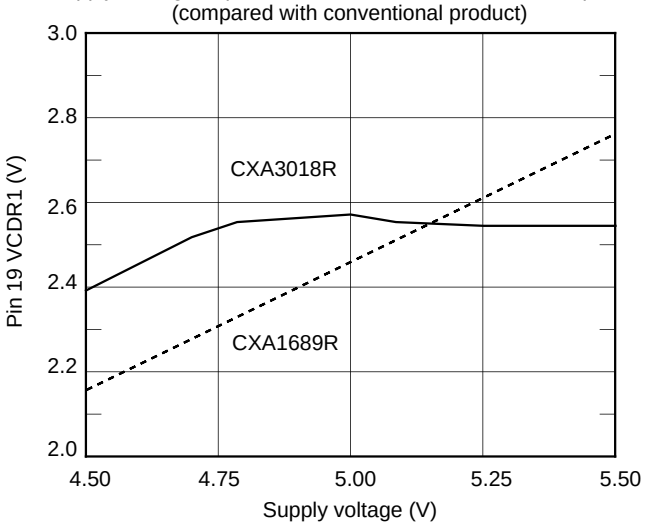
Input level –40 dBm

CN adjustment characteristics



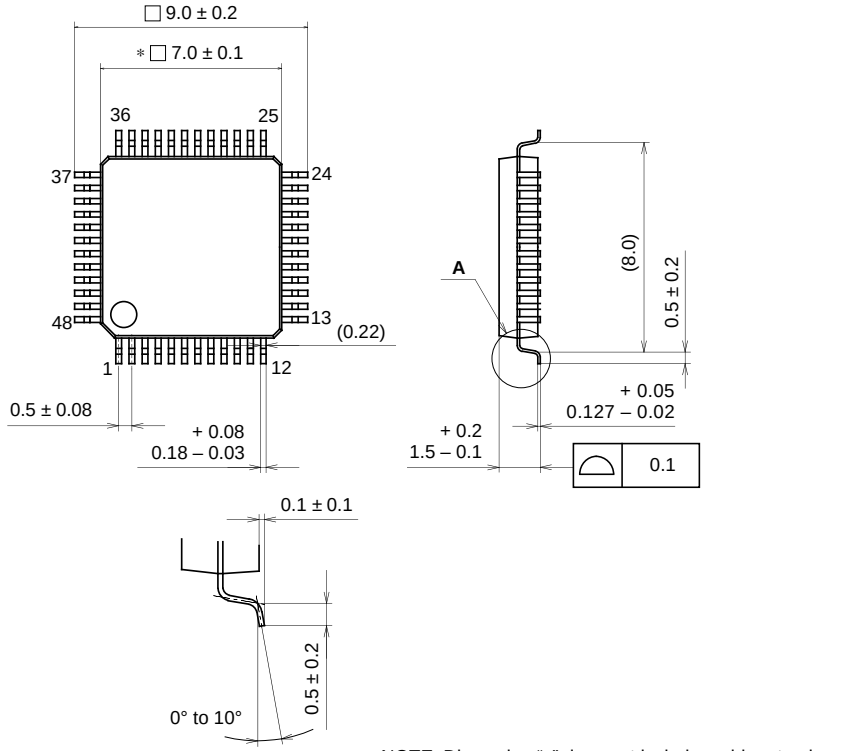
(MIX OUT –pins 28 and 29 are shorted)

Supply voltage dependent characteristics of VCDR1 output DC
(compared with conventional product)



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	∗QFP048-P-0707-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g