SONY

CXA3022R

RF Transmitter IC for PDC

Description

The CXA3022R is a one-chip solution for the RF transmitter function for a 800 MHz or 1.5 GHz PDC handset.

Features

- PLL, quadrature modulation, RF output power control on chip
- Applicable each band of 800 MHz PDC handset or 1.5 GHz PDC handset
- By a three wire serial bus, there are set PLL data and RF output power control data
- VGA Amp can be controled by 8-bit DAC
- Built-in sleep mode

Function

- IQ mixer (quadrature modulation)
- Mixer for up-conversion.
- VGA Amp (Voltage Gain Control Amp)
- 3-bit DAC for PIN ATT.
- 6-bit DAC for PA (Power Amp) control bias.
- 8-bit DAC for VGA power control bias.
- Sample-and-hold function of VGA power control bias.
- PLL for IQ mixer.
- Local output for 2nd IF Mixer (RX).

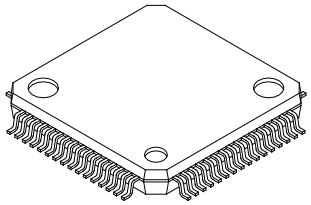
Applications

800 MHz PDC handset and 1.5 GHz PDC handset

Structure

Bipolar silicon monolithic IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

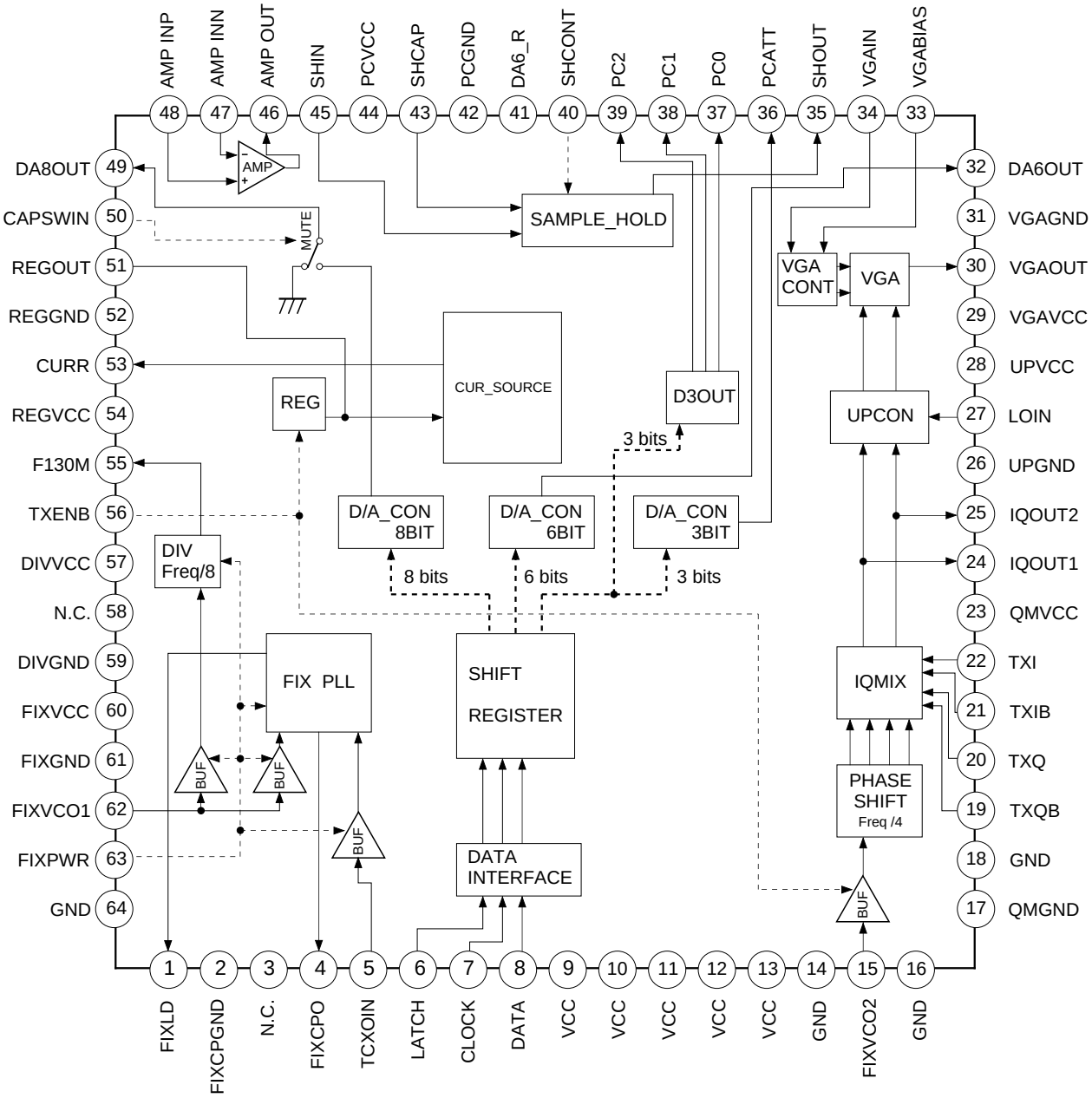
• Supply voltage	V_{CC}	5.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C

Operating Conditions

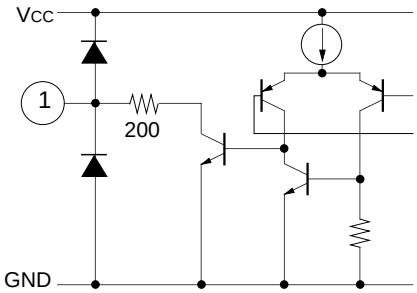
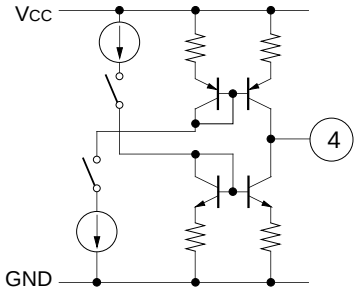
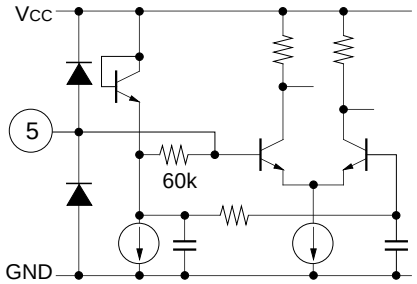
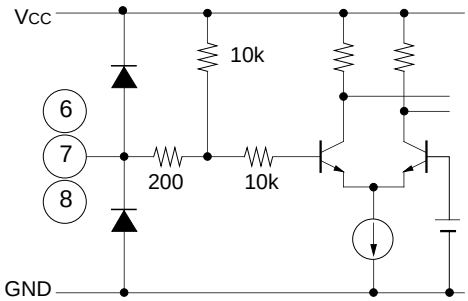
• Operating voltage	V_{CC}	2.7 to 3.3	V

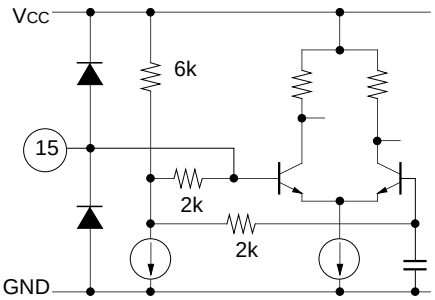
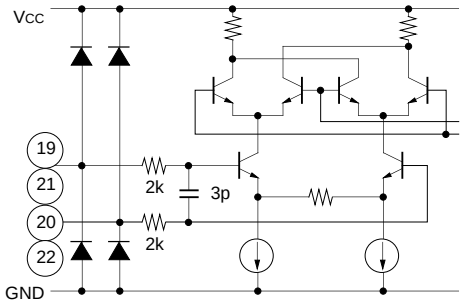
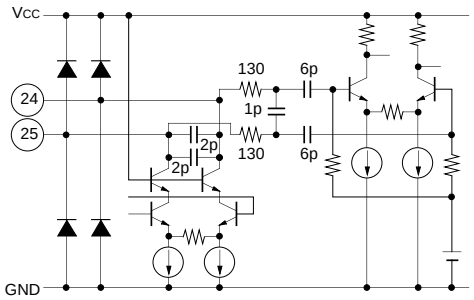
E96645-TE

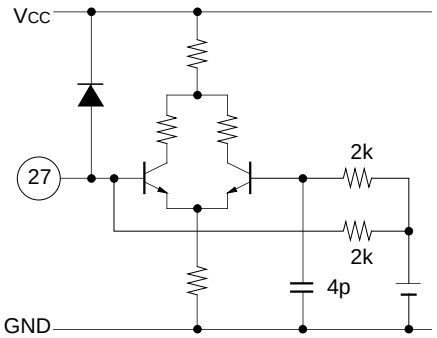
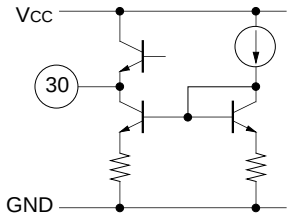
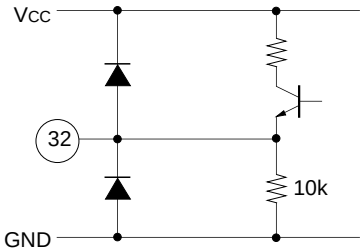
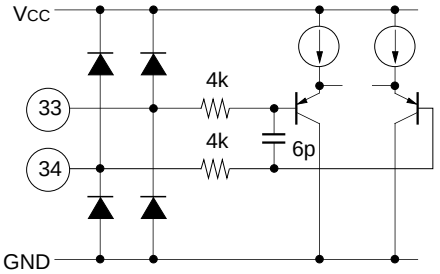
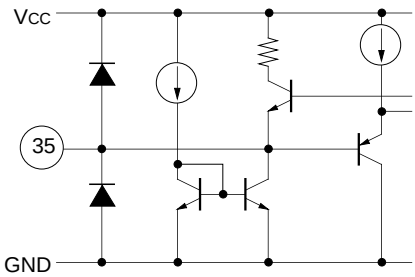
Block Diagram

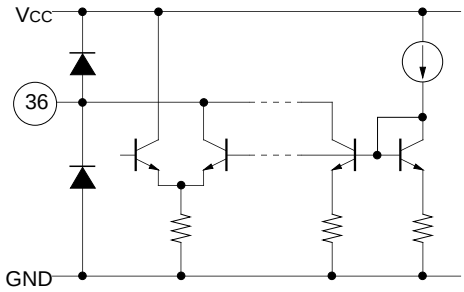
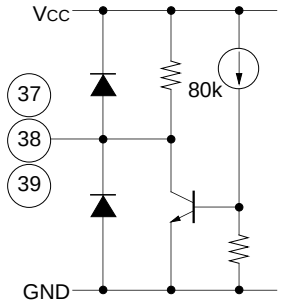
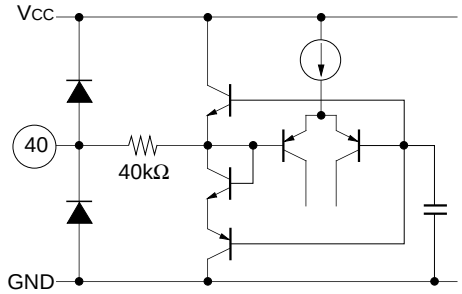
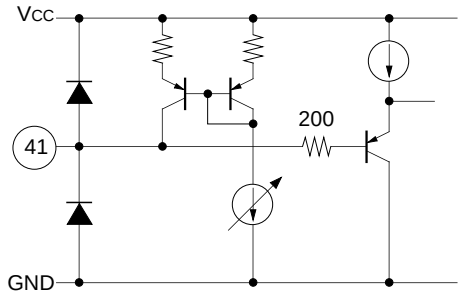
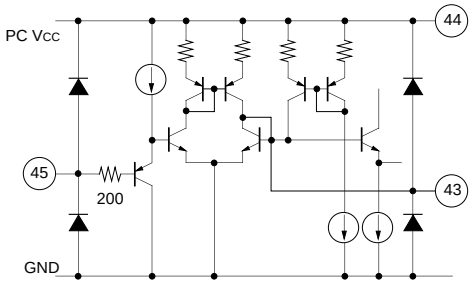


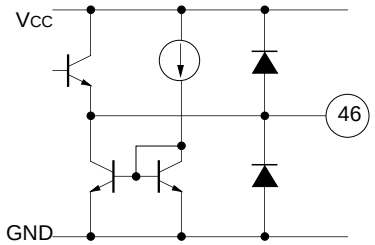
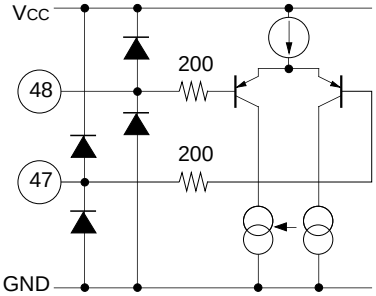
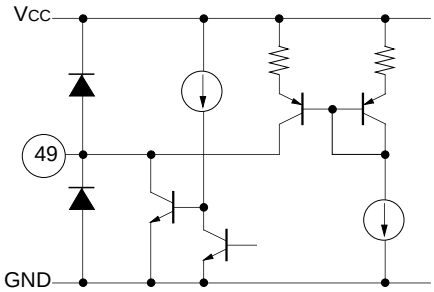
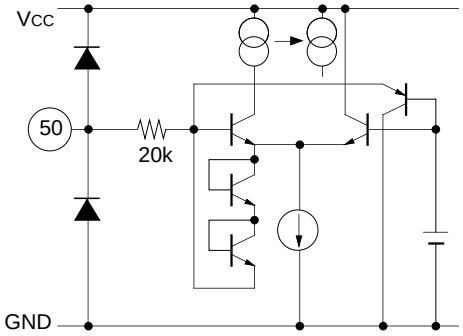
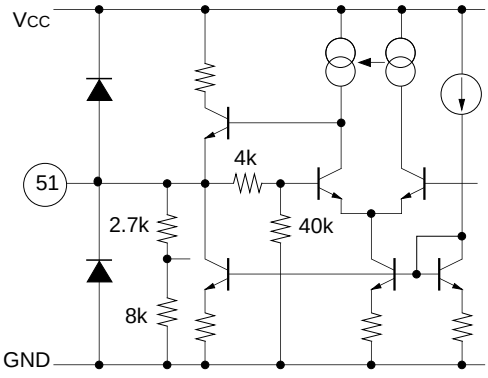
Pin Description

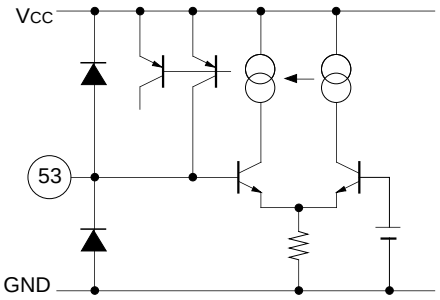
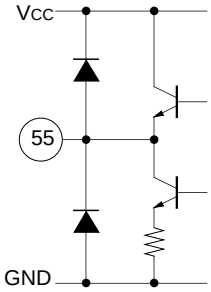
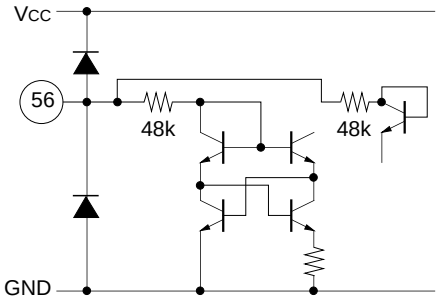
Pin No	Symbol	DC	Equivalent circuit	Description
1	FIXLD			Lock detector signal output of FIXPLL.
2	FIXCPGND	0 V		Ground pin of FIXPLL charge pump.
3 58	N.C			No connect pin.
4	FIXCPO			Charge pump output of FIXPLL.
5	TCXOIN	1.9 V		14.4 MHz reference frequency input to FIXPLL.
6	LATCH	2.74 V		TX control (DAC3, DAC6, DAC8) and FIXPLL programming bus latch input.
7	CLOCK			TX control (DAC3, DAC6, DAC8) and FIXPLL programming bus clock input.
8	DATA			TX control (DAC3, DAC6, DAC8) and FIXPLL programming bus data input.

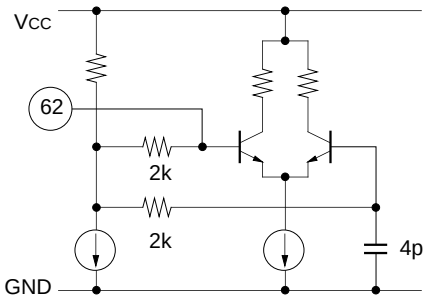
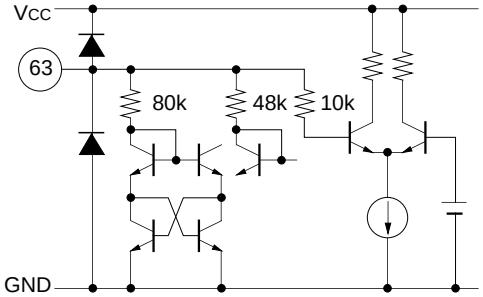
Pin No	Symbol	DC	Equivalent circuit	Description
9 10 11 12 13	VCC	2.75 V		Power supply pin.
14 16 18 64	GND	0 V		Ground pin.
15	FIXVCO2	2.3 V		VCO input to TX.
17	QMGND	0 V		Ground pin of IQMIX.
19	TXQB			Differential transmit inphase and quadrature base-band signal inputs pin. DC coupled inputs, DC level = 1.55 V.
20	TXQ			
21	TXIB			
22	TXI			
23	QMVCC	2.75 V		Power supply pin of IQMIX.
24	IQOUT1			Output pin of IQMIX.
25	IQOUT2			

Pin No	Symbol	DC	Equivalent circuit	Description
26	UPGND	0 V		Ground pin of UPCON.
27	LOIN	1.4 V		Input pin of UPCON(LO).
28	UPVCC	2.75 V		Power supply pin of UPCON.
29	VGAVCC	2.75 V		Power supply pin of VGA.
30	VGAOUT	1.6 V		Transmit RF output pin of VGA.
31	VGAGND	0 V		Ground pin of VGA.
32	DA6OUT			Output pin of DAC6 output voltage.
33	VGABIAS			Input pin of VGA control voltage.
34	VGAIN			Input pin of VGA control voltage.
35	SHOUT			Output pin of SAMPLE_HOLD.

Pin No	Symbol	DC	Equivalent circuit	Description
36	PCATT			Output pin of DAC3 output current. (set to Vcc)
37	PC0			Output pin of DAC3 output voltage.
38	PC1			Output pin of DAC3 output voltage.
39	PC2			Output pin of DAC3 output voltage.
40	SHCONT			Input pin of SAMPLE_HOLD control voltage.
41	DA6_R			External resistor pin (metal film resistor).
42	PCGND	0 V		Ground pin of PC (power control section).
43	SHCAP			External capacitor pin.
44	PCVCC	2.75 V		Power supply pin for PC (power control section).
45	SHIN			Input pin of SAMPLE_HOLD.

Pin No	Symbol	DC	Equivalent circuit	Description
46	AMPOUT			Output pin of AMP.
47	AMPINN			Input pin of AMP (N).
48	AMPINP			Input pin of AMP (P).
49	DA8OUT			Output pin of DAC8 output current.
50	CAPSWIN			Output control pin of DAC8.
51	REGOUT	1.34 V		Output pin of regulator voltage.

Pin No	Symbol	DC	Equivalent circuit	Description
52	REGGND	0 V		Ground pin of REG.
53	CURR	1.0 V		The pin for external resistor (Metal film resister).
54	REGVCC	2.75 V		Power supply pin of REG.
55	F130M	0.95 V		Output pin of frequency /8 of FIXVCO1 input.
56	TXENB			Enable input pin for TX section.
57	DIVVCC	2.75 V		Power supply pin.
59	DIVGND	0 V		Ground pin of DIV.
60	FIXVCC	2.75 V		Power supply pin of FIXVCC.
61	FIXGND	0 V		Ground pin of FIXVCC.

Pin No	Symbol	DC	Equivalent circuit	Description
62	FIXVCO1	2.3 V		VCO input to FIXPLL.
63	FIXPWR			Power save pin for FIXPLL section.

Electrical Characteristics

V_{CC}=2.75 V, Ta=25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply	V_{CC}		2.7	2.75	3.3	V
Supply current (TX mode)	$I_{CC}1$	TXENB=2.75 V (High) FIX (PLL1) PWR=2.75 V (High)	52.0	64.0	77.0	mA
Supply current (PLL active mode)	$I_{CC}2$	TXENB=0 V (Low) FIX (PLL1) PWR=2.75 V (High)	5.6	8.8	12.5	
Supply current (Sleep mode)	$I_{CC}3$	TXENB=0 V (Low) FIX (PLL1) PWR=0 V (Low)	0.34	0.55	0.83	
TXENB						
High level input voltage	VHTX		V_{CC} –0.8	—	V_{CC}	V
Low level input voltage	VLTX		–0.2	—	0.5	V
Rise time	TRTX	Vreg : ON, Cext=2000 pF			5.0	µs
High level input current (TXENBpin)	IHTX	TXENB=V_{CC}=2.75 V	37.0	46.0	70.0	µA
REGOUT						
Output voltage	VOREG	TXENB=V_{CC}=2.75 V	1.24	1.33	1.40	V
DATA, CLOCK, LATCH						
Input voltage level – Low	VinL				1.10	V
Input voltage level – High	VinH		2.40			

TX section V_{CC}=2.75 V, Ta=25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IQMOD (I & Q modulator)						
Input bias current	IQM		1.0	7.0	16.0	µA
Input DC voltage	VinQM			1550		mV
Input AC level	vinQM			–4		dBm
UPCON						
TX local input frequency	finLO		1169.9	—	1215.1	MHz
TX local input level	vinLO			–12		dBm
VGA (Transmit output)						
Output level (1) (CONT:1.8 V)	voVGA1	*1 f=1474.2 MHz VGAIN=1.8 V, VGABIAS=1.2 V	–24	–21	–14	dBm
Output level (2) (CONT:1.3 V)	voVGA2	*1 f=1474.2 MHz VGAIN=1.3 V, VGABIAS=1.2 V	–36	–29	–20.5	
Output level (3) (CONT:0.5 V)	voVGA3	*1 f=1474.2 MHz VGAIN=0.5 V, VGABIAS=1.2 V		–63.5		
Gain range	GraVGA	*1 f=1474.2 MHz	41	42.5		dB
Image suppression	Sima	*1		–54	–40	dBc
Carrier suppression	Scar	*1		–39	–30	
IM3	IM3	*1		–58	–50	dB
Output level difference (Frequency)	vodif	*1 Output level (1474.2 MHz)– Output level (956 MHz)	–4.5	–3.5		
TX local leak level	voLole	*1		–14		

*1. IF input (FIXVCO=–10 dBm, 1036.4 MHz), LO input (–12 dBm 1215.1 MHz)

TX power control section V_{CC}=2.75 V, Ta=25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VGACONT						
Input current (VGABIAS pin)	Iin VBIA	VGABIAS=VGAIN=1.2 V	–1	0.0	1	µA
Input current (VGAIN pin)	Iin VIN	VGABIAS=VGAIN=1.2 V	–1	0.0	1	
OPAMP						
High level output voltage	VoHOA	AMPINN=0.8 V, AMPINP=1.0 V (NFB)	1880	2000		mV
Low level output voltage	VoLOA	AMPINN=0.6 V, AMPINP=0.4 V (NFB)		40	100	
S/H (SAMPLE_HOLD)						
High level control voltage (hold)	VinHSH		V_{CC}–0.8	—	V_{CC}	V
Low level control voltage (sampling)	VinLSH		–0.2	—	0.8	
High level input current (SHCONT pin)	IinHSH	SHCONT=V_{CC}=2.75 V	1.0	9.0	15.0	µA
Low level input current (SHCONT pin)	IinLSH	SHCONT=–0.3 V	–35.0	–24.0	–15.0	
Input voltage range (SHIN pin)	VinRSH		500	—	1700	mV
Droop (6.7 mS)	dro	SHIN=1.0, SHCAP (Cext 0.033 µ),	–1	—	1	
Precision of hold voltage	pho	SHIN=1.0	–1	—	1	
DAC3						
Output current (1)	IoD31	DAC3_DATA : 0	95	100	108	µA
Output current (2)	IoD32	DAC3_DATA : 1	172	182	197	
Output current (3)	IoD33	DAC3_DATA : 2	313	332	354	
Output current (4)	IoD34	DAC3_DATA : 3	570	604	640	
Output current (5)	IoD35	DAC3_DATA : 4	1038	1100	1169	
Output current (6)	IoD36	DAC3_DATA : 5	1888	2000	2119	
Output current (7)	IoD37	DAC3_DATA : 6, 7	–1	0	1	

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PC0, PC1, PC2 output voltage High level	VoHD3		2.55	2.74		V
PC0, PC1, PC2 output voltage Low level	VoLd3			65	120	mV
DAC6						
MAX output voltage	VomaxD6	V_{CC}= 2.75 V DAC6_DATA 63, DA6_R=15 kΩ	1.67	1.83	2.00	V
MIN output voltage	VominD6	V_{CC}= 2.75 V DAC6_DATA 0, DA6_R=15 kΩ	169	315	400	mV
Source current	IsD6			200	500	µA
DAC8						
MAX output voltage	VomaxD8	V_{CC}= 2.75 V DAC8_DATA 255, RL=13 kΩ	1080	1160	1236	mV
MIN output voltage	VominD8	V_{CC}= 2.75 V DAC8_DATA 0, RL=13 kΩ	–1	0	1	
Output voltage (CAPSW OFF)	Vocapoff	CAPSWIN=0.0 V		40	90	
CAPSW						
High level control voltage	V_{HCAP}	RL=10 kΩ	V_{CC}–0.8	—	V_{CC}	V
Low level control voltage	V_{LCAP}	RL=10 kΩ	–0.2	—	0.7	
High level input current	I_{HCAP}	CAPSWIN=V_{CC}=2.75 V	30	43	60	µA
Low level input current	I_{LCAP}	CAPSWIN=0 V	–2	0	2	

PLL section V_{CC}=2.75 V, Ta=25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level control voltage	V_{HFP}		V_{CC}–0.8	—	V_{CC}	V
Low level control voltage	V_{LFP}		–0.2	—	0.5	
High level input current (FIXPLL)	I_{HFP}	FIXPWR=V_{CC}=2.75 V	36	49	65	µA
Low level input current (FIXPLL)	I_{LFP}	FIXPWR=0 V	–1	0	1	
FIXPLL input frequency	finFP	TCXO : 14.4 MHz		1036.4		MHz
FIXPLL input level	vinFP	TCXO : 14.4 MHz		–10		dBm
Charge pump current	I_{CP}	Each charge pump		1.20		mA
LD output voltage level–Low	V_{LLD}	PLL : Unlock		30	100	mV
LD output voltage level–High	V_{HLD}	PLL : Lock RL=100 K	2550	2750		
PLL (FIXPLL) /8						
Output level	foFP/8	RL=50 Ω, FIXVCO1 pin : 1036.4 MHz	–24.5	–20.0	–16.5	dBm
Output frequency	voFP/8	RL=50 Ω, FIXVCO1 pin : 1036.4 MHz		129.55		MHz

Function Mode 1

Function mode	TXENB	FIXPWR
1. TX mode	high	high
2. PLL active mode	low	high
3. Sleep mode	low	low

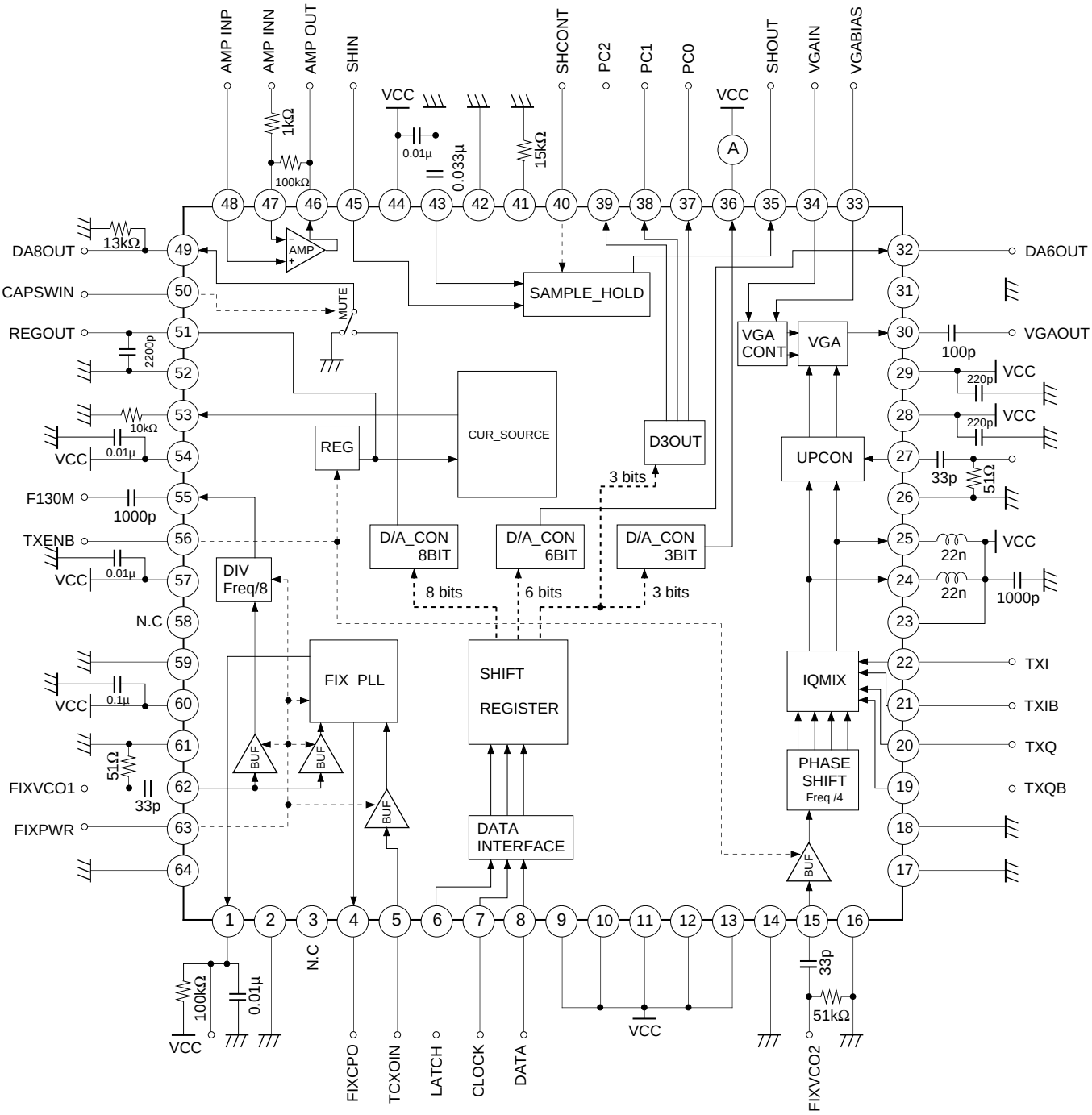
Mode functions explain:

1. TX mode:
   This mode requires everything circuits to be operating.
2. PLL active mode :
   This mode powers down everything except the PLL circuit and the not sleep circuit.
3. Sleep mode :
   This mode powers down everything except the not sleep circuits.

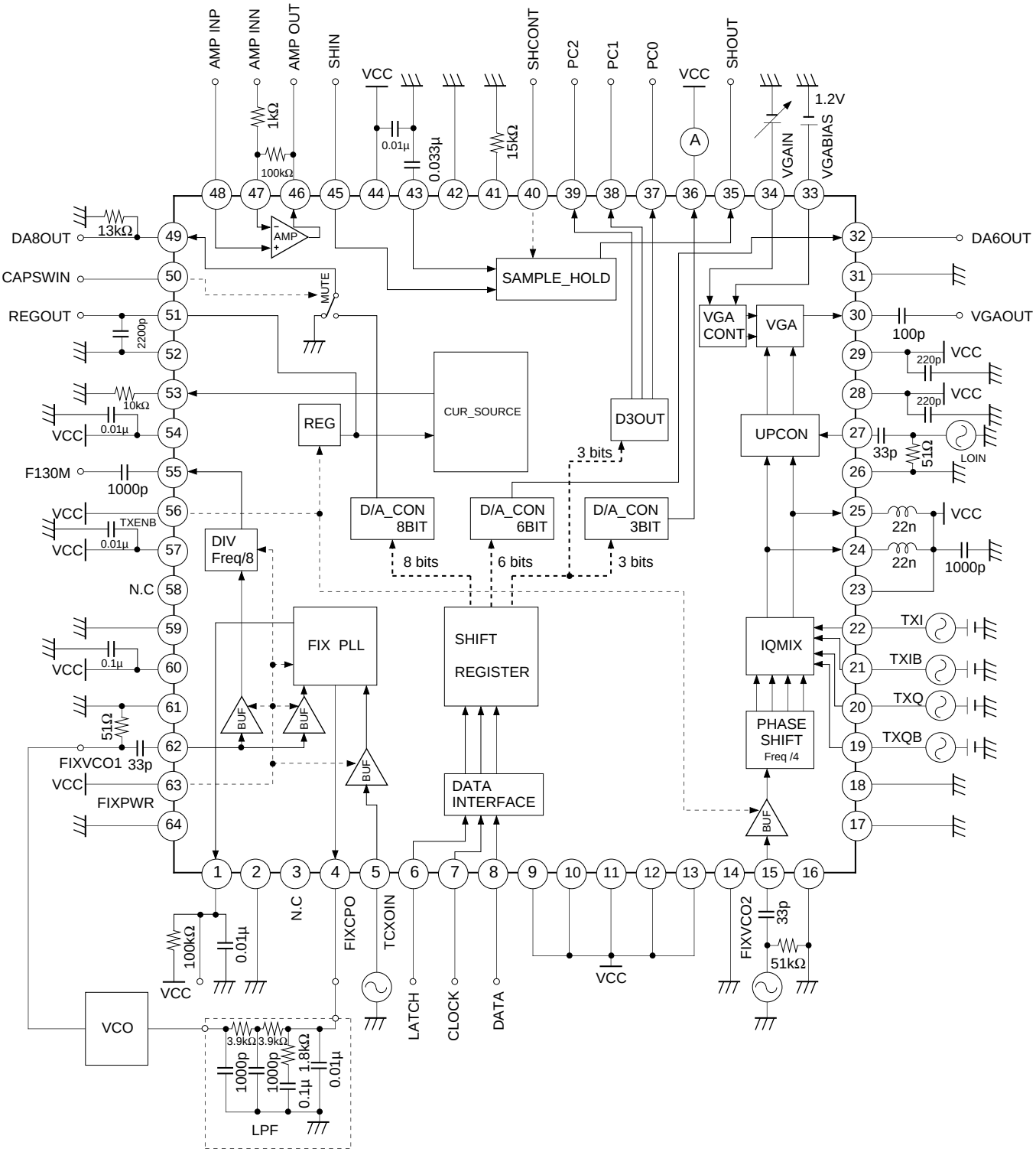
Function Mode 2

Control pin	Input	Function mode
SHCONT	L	Sampling
	H	Hold
CAPSWIN (DAC8SW)	L	DAC8 OFF (mute)
	H	DAC8 ON (active)

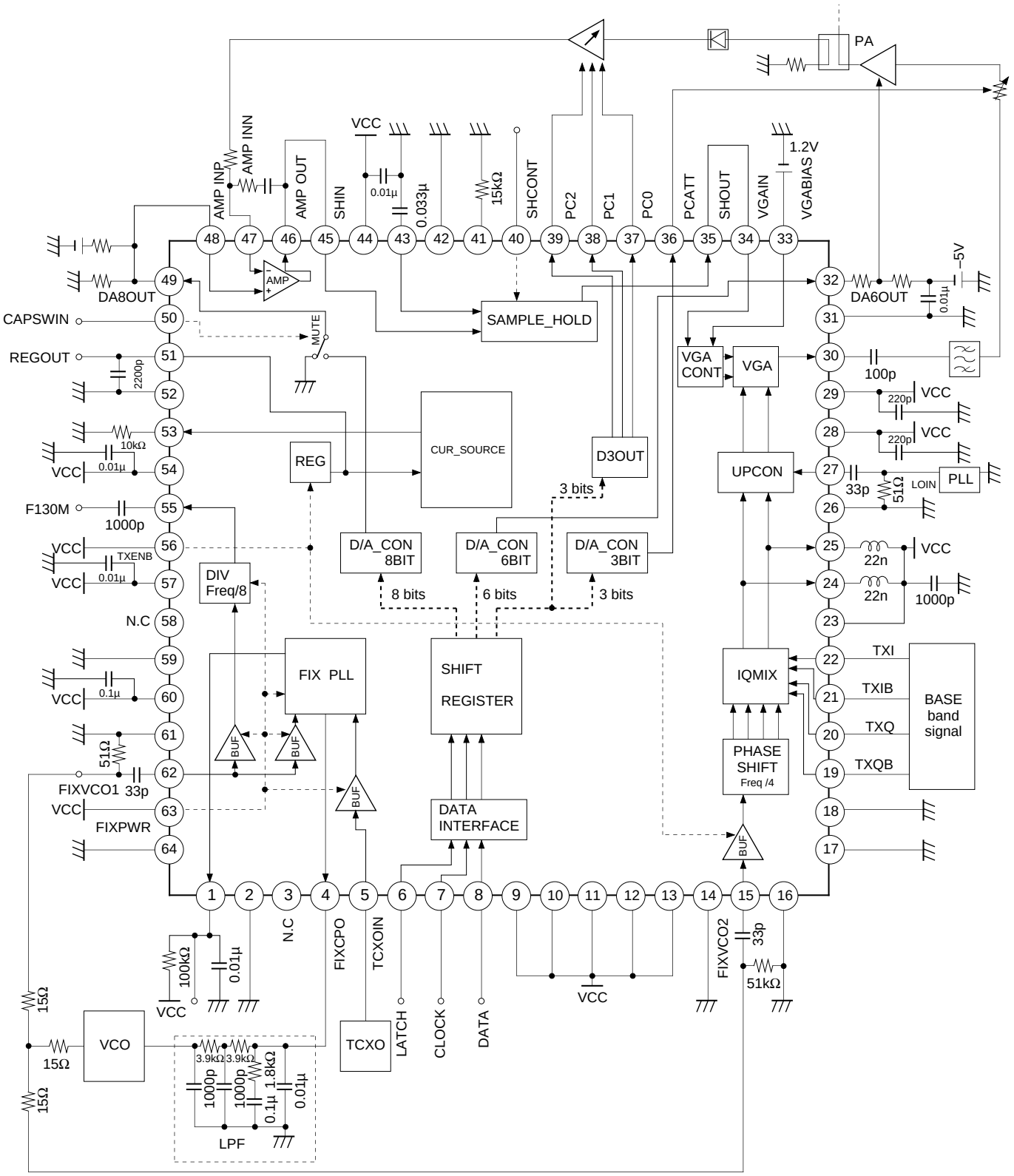
DC Electrical Characteristics Measurement Circuit



Electrical Characteristics Measurement Circuit



Application Circuit



Description of operation

The CXA3022R is a one-chip solution for the RF transmitter section for a 800 MHz or 1.5 GHz PDC (personal digital cellar) handset. It has three sections: Transmit, Transmit control, and PLL. There are two pins (TXENB/FIXPWR) allowing power save.

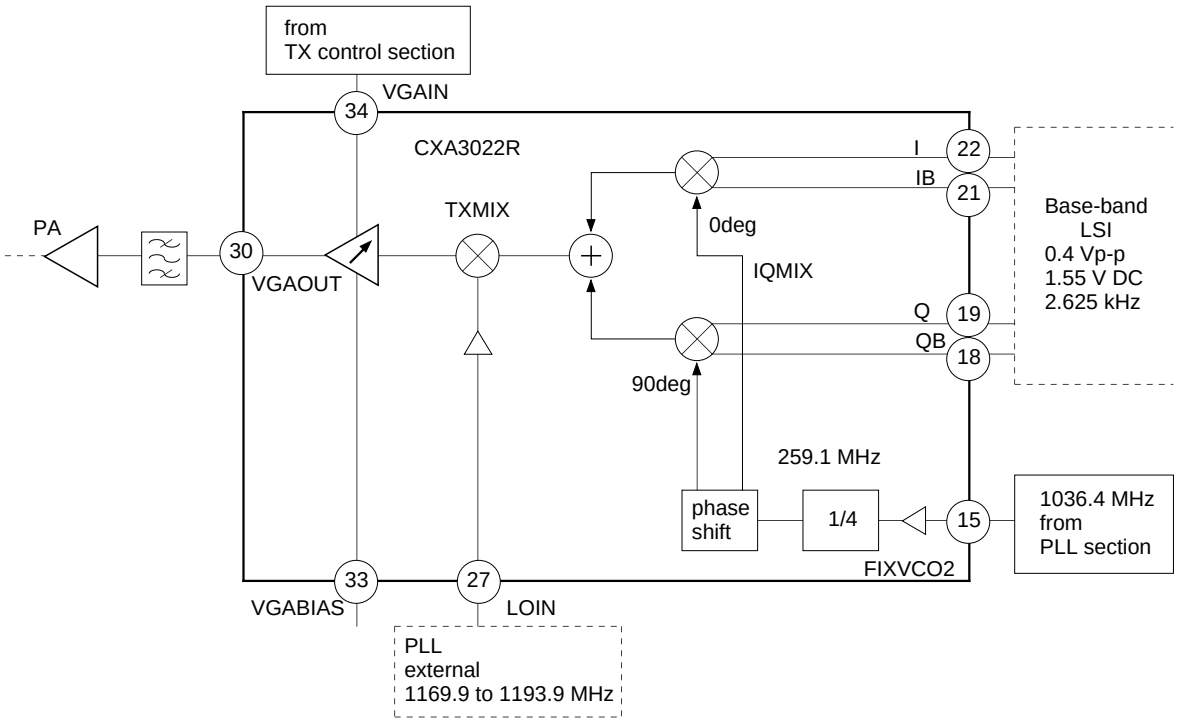
Transmit Section

The transmit section converts signals from base-band I and Q to RF using a double conversion approach. The device accepts differential I and Q base-band signals (TXI, TXIB, TXQ and TXQB pins) which are converted to IF using a quadrature modulator. Shows the transmit section detail.

The I and Q signals should be DC coupled. The CXA3022R expects these signals to be at about 1.55 V DC and 0.4 Vp-p differential.

The output power is typically –29 dBm (1.5 GHz) if the base-band input signals are 0.4 Vp-p.
This IC has gain control pin. When the VGAIN pin is 1.8 V (VGABIAS=1.2 V), output level is maximum. When the VGAIN pin is 0.5 V (VGABIAS=1.2 V), output level is minimum.

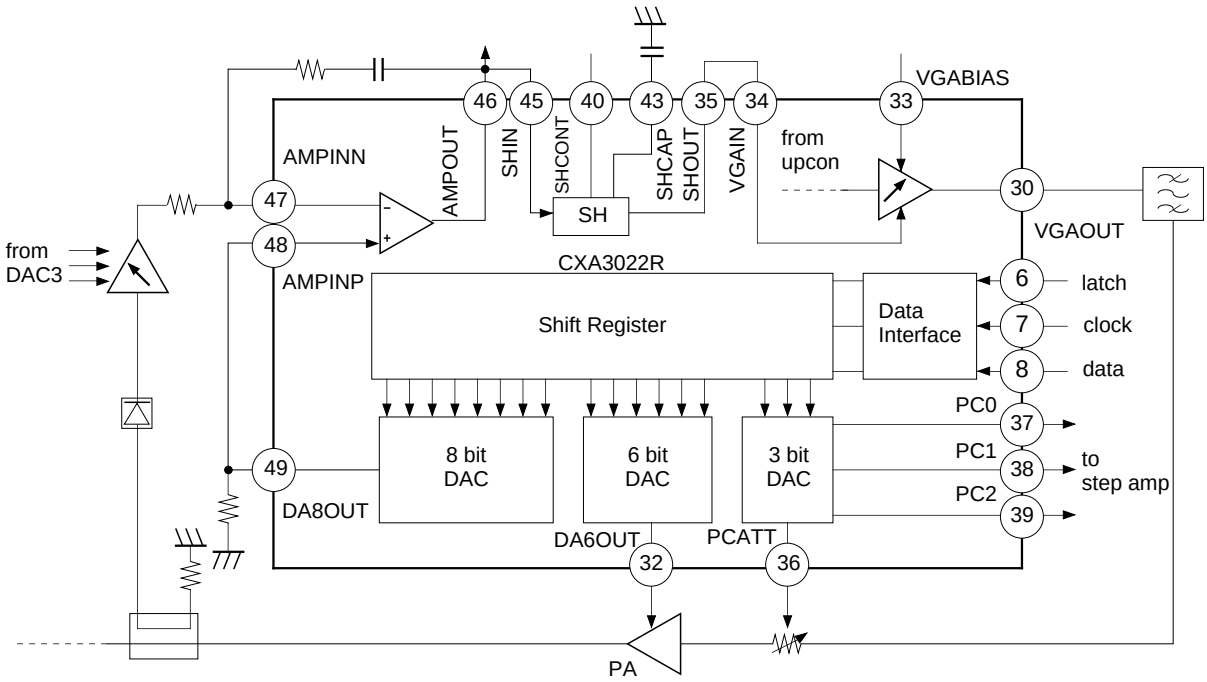
Transmit Section Detail



TX Control Section

TX control has five blocks : 3-bit DAC, 6-bit DAC, 8-bit DAC, SAMPLE_HOLD, and VGACONT.
Shows the Transmit Control detail.

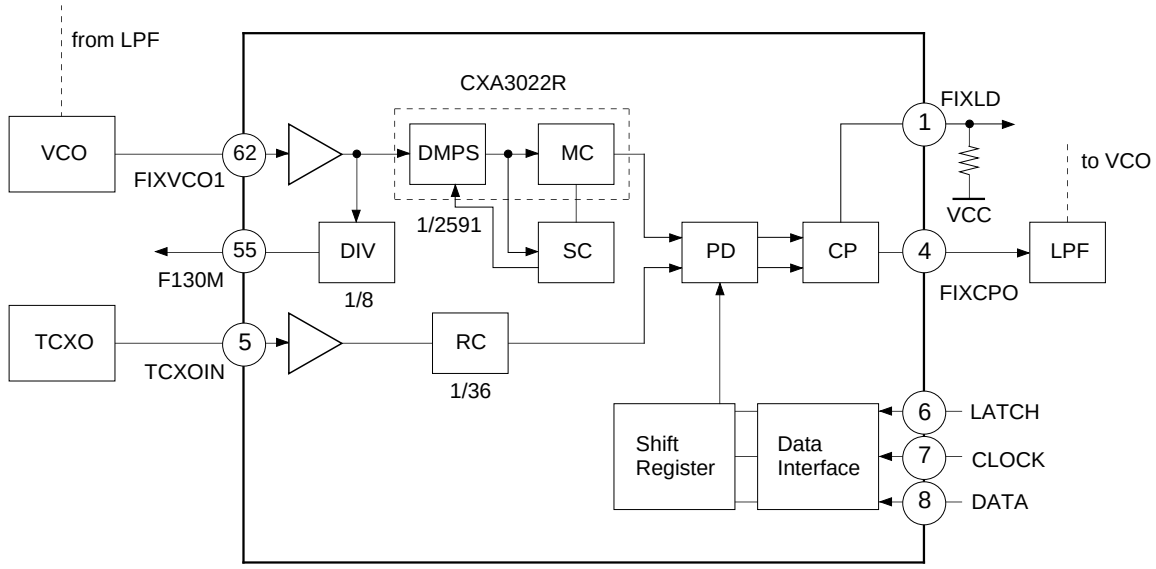
Transmit Control Section Detail



FIXPLL

The CXA3022R has FIX PLL : except VCO and LPF.
The FIXPLL works from a 14.4 MHz reference clock.
Shows the FIXPLL detail.

PLL Detail

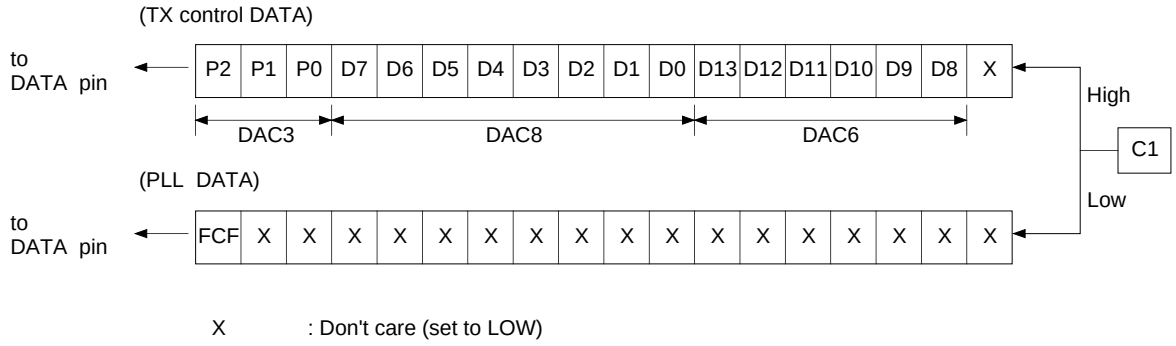


TX Control and PLL Programming

The TX control and PLL are programmed via a three wire bus : DATA, CLOCK, and LATCH.
These data are loaded into a 19-bit shift register. The data on the DATA input is loaded into the shift resister at the rising edge of the CLOCK signal.

Data Structure

The control data structure is given below :
P2 or FCF is the first bit loaded, and C1 is the last. When the signal on the LATCH pin rises, the CXA3022R will assume that the last bit is C1. These tell the CXA3022R the destination of the control data : the TX control (DAC3, DAC6, DAC8) or the PLL.



C1 : Latch Address Bits

C1	Data latch address
Low	PLL data
High	TX control (DAC3, DAC6, DAC8) data

P0 to P2 : Output voltage and output current control for DAC3

P0 to P2 : DAC3 output voltage control

	Data	Output voltage		
		PC0	PC1	PC2
P0	L	Low	—	—
	H	High	—	—
P1	L	—	Low	—
	H	—	High	—
P2	L	—	—	Low
	H	—	—	High

P0 to P2 : DAC3 output current control (Binary value with P0 as LSB)

Data			Output current
P2	P1	P0	Typ.
L	L	L	–26 dB
L	L	H	–20.8 dB
L	H	L	–15.6 dB
L	H	H	–10.4 dB
H	L	L	–5.2 dB
H	L	H	0 dB
H	H	L	∗
H	H	H	∗

0 dB=2 mA, ∗=0 µA

D8 to D13 : Output voltage control for DAC6 (Binary value with D8 as LSB)

	Data						Output voltage
	D13	D12	D11	D10	D9	D8	
0	L	L	L	L	L	L	MIN
1	L	L	L	L	L	H	:
2	L	L	L	L	H	L	:
3	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
62	H	H	H	H	H	L	:
63	H	H	H	H	H	H	MAX

L : Low, H : High

D0 to D7 : Output current control for DAC8 (Binary value with D0 as LSB)

	Data								Output current
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	MIN
1	L	L	L	L	L	L	L	H	:
2	L	L	L	L	L	L	H	L	:
3	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
254	H	H	H	H	H	H	H	L	:
255	H	H	H	H	H	H	H	H	MAX

L : Low, H : High

FCF : Polarity control bit of PLL charge pump

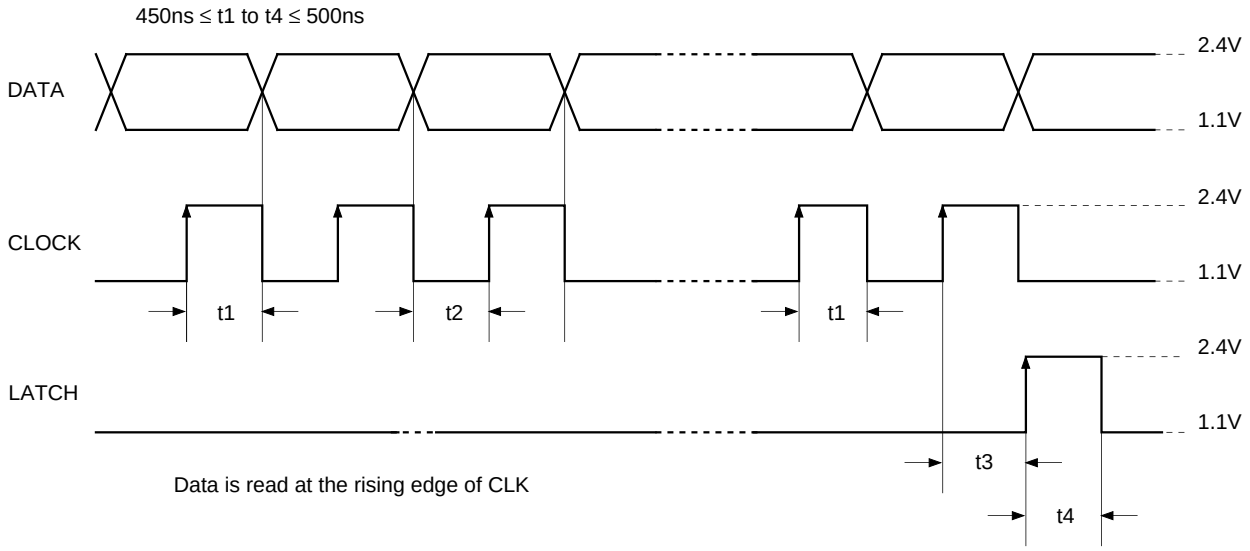
	FCF : Low	FCF : High
Signal	FIXCPO	FIXCPO
fri>fpi	H	L
fri=fpi	Z	Z
fri<fpi	L	H

fri : Output frequency of PLL reference counter

fpi : Output frequency of PLL programmable counter

Z : High impedance (PLL lock)

Data input timing



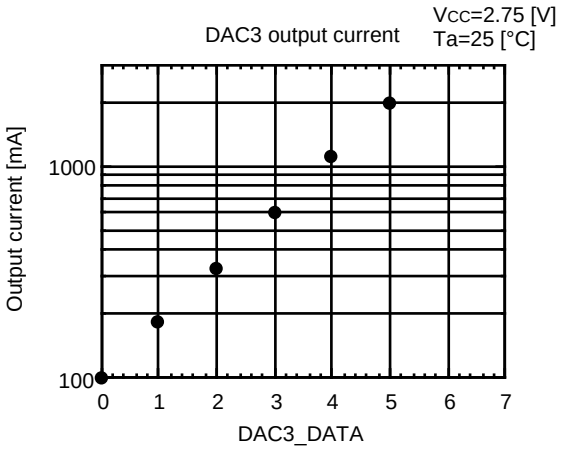
Notes on Operation

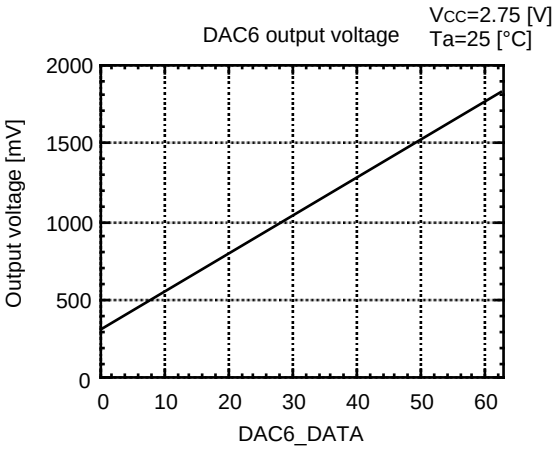
1. Pay attention to handling this IC because its electrostatic discharge strength is weak.

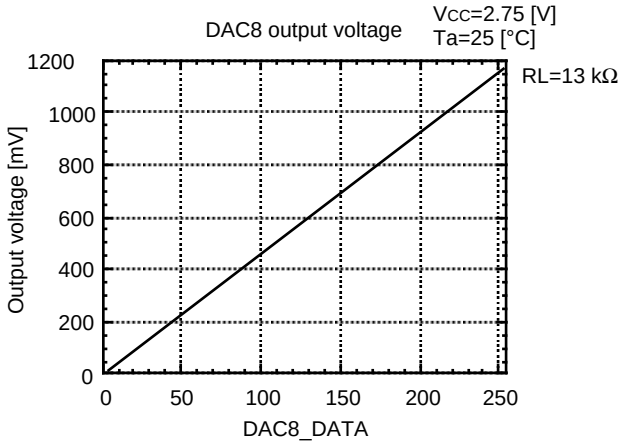
2. The outputs (PCATT, IQOUT1, IQOUT2, FIXLD) of this IC are the open collector type. When these pins are not used, connect to V_{CC}.

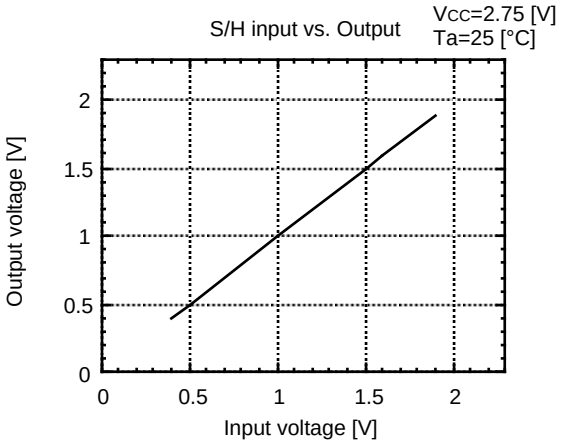
3. The 10 kΩ metal film resistor should be connected between Pin 53 and GND.

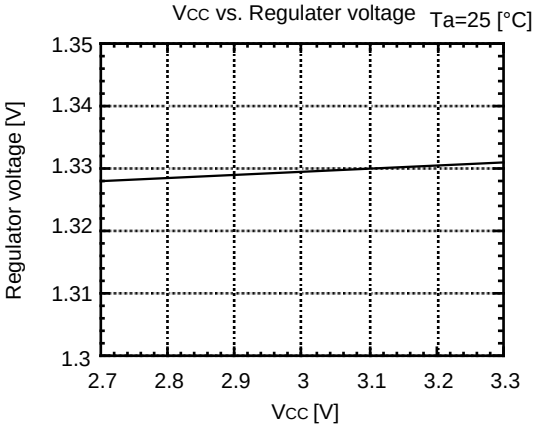
Example of Representative Characteristics



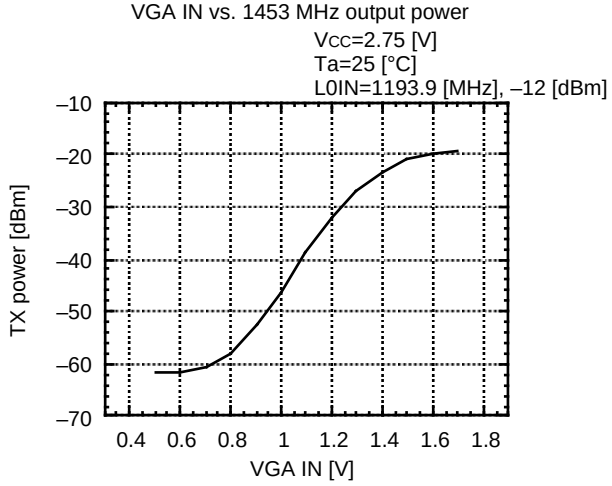




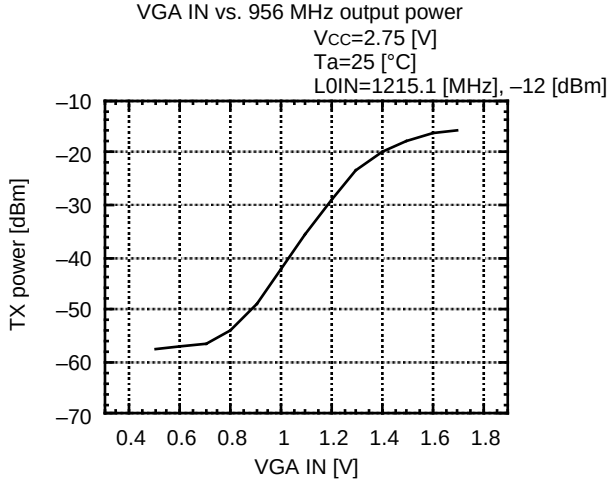




VGA IN vs. 1453 MHz output power



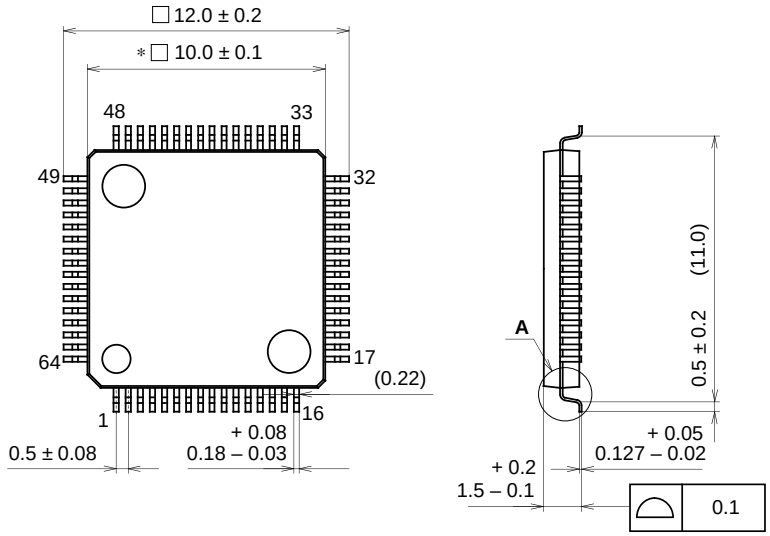
VGA IN vs. 956 MHz output power

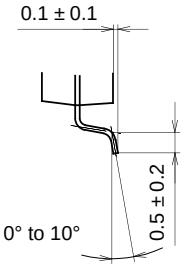


Common Conditions
I, Q (IB, QB) signal input : 2.625 [kHz], 0.4 Vp-p
I, Q (IB, QB) bias : 1.55 [V]
FIX VCO2 input : 1036.4 [MHz], –10 [dBm]

Package Outline Unit : mm

64PIN LQFP (PLASTIC)





DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g