SONY

CXA3185/3186N

All Band TV Tuner IC with On-chip PLL

Description

The CXA3185/3186N is a monolithic TV tuner IC which integrates local oscillator and mixer circuits for VHF band, local oscillator and mixer circuits for UHF band, an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner.

Features

- Low noise figure
- Low power consumption (5 V, 54 mA typ.)
- On-chip tuning PLL (3-wire bus format)
- Selection of frequency steps 31.25 kHz, 50 kHz and 62.5 kHz
- On-chip 4-output band switch

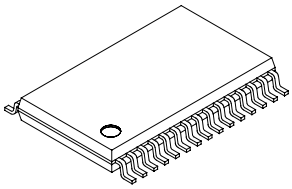
Applications

- TV tuners
- VCR tuners
- CATV tuners

Structure

Bipolar silicon monolithic IC

30 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta = 25 °C)

• Supply voltage	$V_{CC}1, V_{CC}2$	–0.3 to +5.5	V
	$V_{CC}3$	–0.3 to +10.0	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	880	mW
	(when mounted on a substrate)		

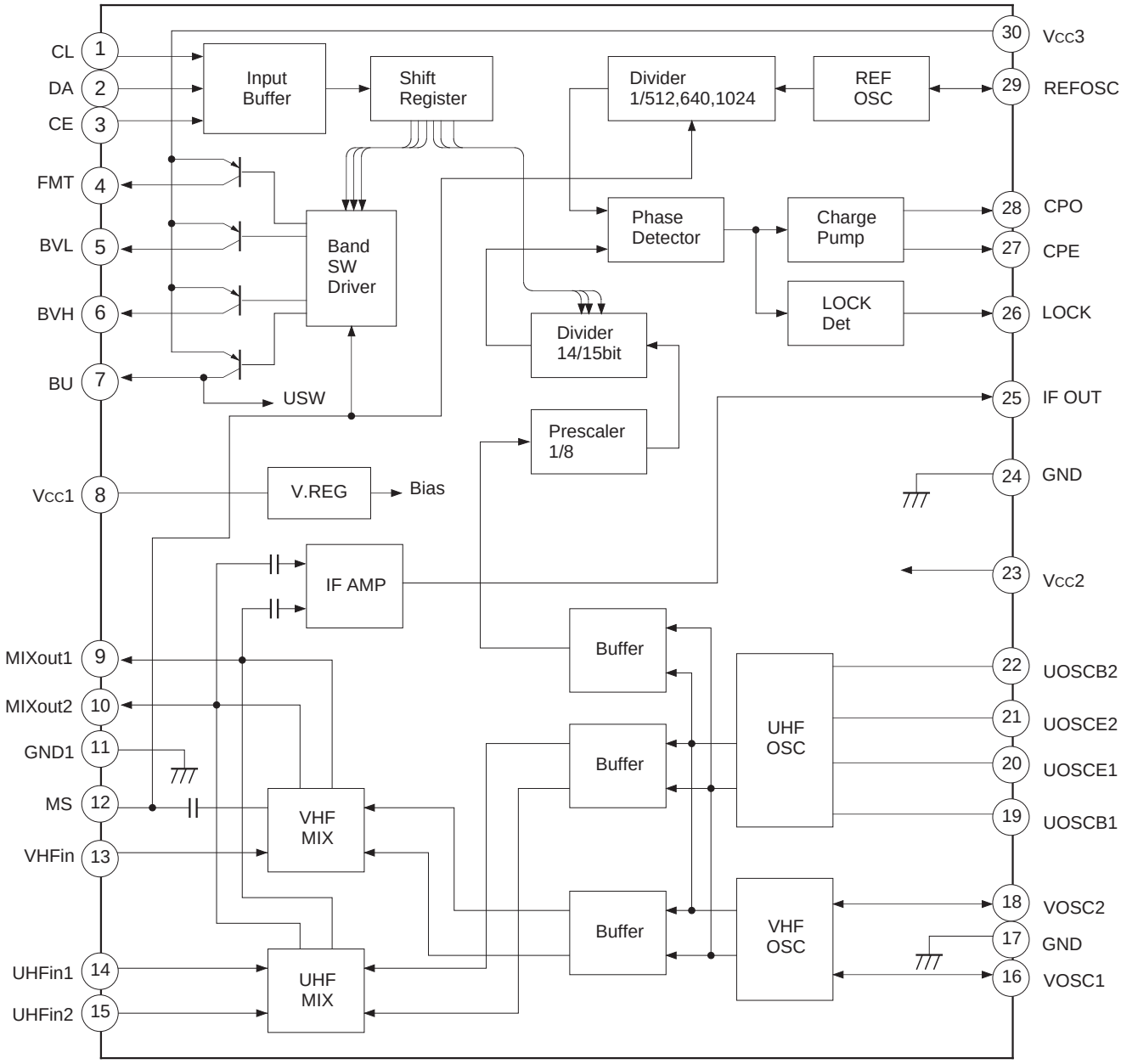
Operating Conditions

• Supply voltage	$V_{CC}1, V_{CC}2$	4.75 to 5.3	V
	$V_{CC}3$	4.75 to 9.45	V
• Operating temperature	Topr	–20 to +75	°C

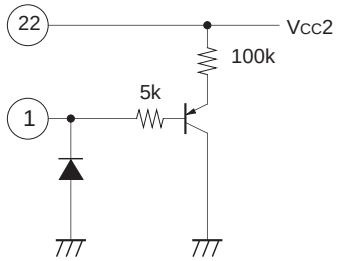
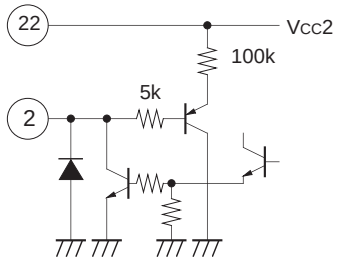
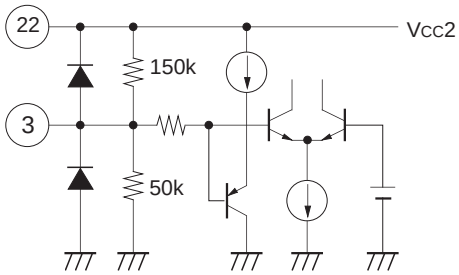
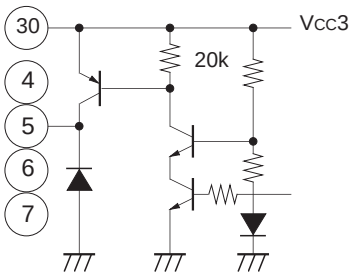
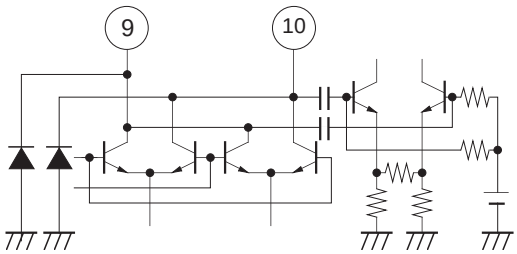
Note) Electrostatic discharge strength is weak, and care should be taken in handling this IC.

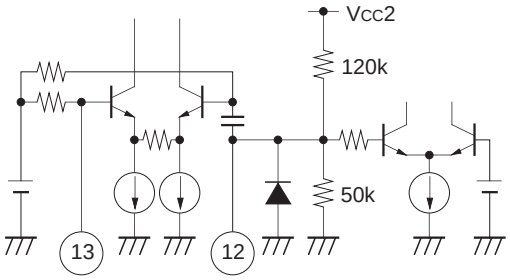
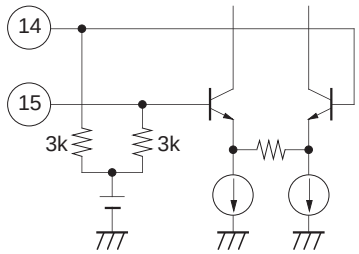
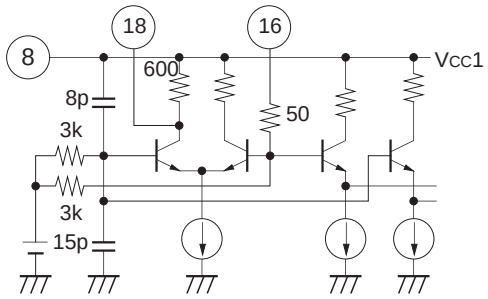
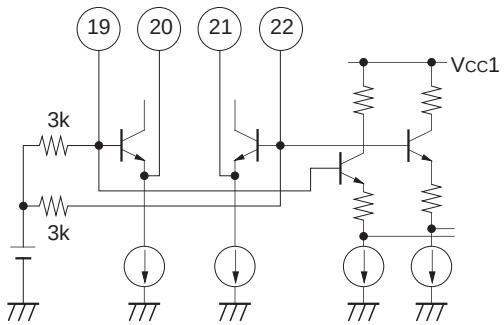
E97944-TE

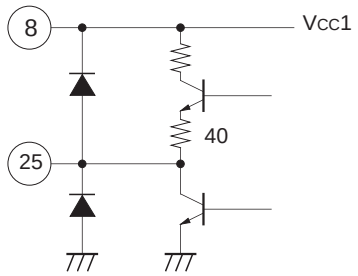
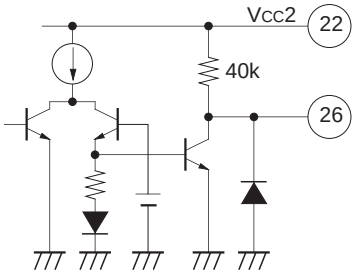
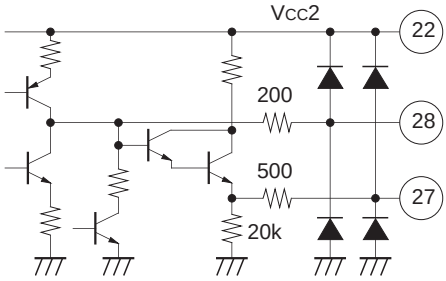
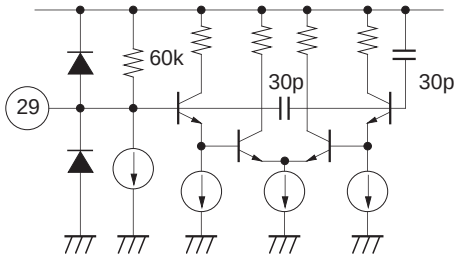
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
1	CL		—	Clock input.
2	DA		—	Data input.
3	CE		1.25 (when open)	Enable pin.
4	FMT		ON : Vcc3 OFF : 0	4 : Output for FM TRAP. 5 : Power supply output for VL band. 6 : Power supply output for VH band. 7 : Power supply output for UHF band. The selected band pin goes High.
5	BVL			
6	BVH			
7	BU			
8	Vcc1			Analog circuit power supply.
9	MIXout1			Mixer outputs.
10	MIXout2			
11	GND1	—	—	Analog circuit GND.

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
12	MS		1.5 (when open)	Frequency step mode selection. Five modes can be selected according to the applied voltage.
13	VHFin		2.3 (VHF) 0 (UHF)	VHF input. The input format is unbalanced input.
14	UHFin1		0 (VHF) 2.3 (UHF)	UHF input. The input method can be selected from balanced input or unbalanced input.
15	UHFin2		0 (VHF) 2.3 (UHF)	
16	VOSC1		3.0 (VHF) 3.1 (UHF)	External resonance circuit connection for VHF oscillator.
18	VOSC2		3.5 (VHF) 5.0 (UHF)	
17	GND		—	GND
19	UOSCB1		3.2 (VHF) 2.9 (UHF)	External resonance circuit connection for UHF oscillator.
20	UOSCE1		— (VHF) 2.4 (UHF)	
21	UOSCE2		— (VHF) 2.4 (UHF)	
22	UOSCB2		3.2 (VHF) 2.9 (UHF)	

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
23	Vcc2	—	—	PLL circuit power supply.
24	GND2	—	—	PLL circuit GND.
25	IFOUT		2.3	IF output.
26	LOCK		5.0 (Lock) 0.2 (UNLock)	LOCK detection. High when locked, Low when unlocked.
27	CPE		0.6	NPN transistor connection for varicap diode drive.
28	CPO		2.0	Charge pump output. Connect a loop filter.
29	REFOSC		4.3	Crystal connection for reference oscillator.
30	Vcc3		—	Power supply for external supply.

Electrical Characteristics See the Electrical Characteristics Measurement Circuit.

Circuit Current (V_{CC}=5 V, Ta=25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current A	AI$_{CCV}$	V_{CC}1 current, Band switch output open during VHF operation	30	41	55	mA
	AI$_{CCU}$	V_{CC}1 current, Band switch output open during UHF operation	31	42	56	mA
Circuit current D	DI$_{CC}$	V_{CC}2 current	7	11	15	mA

OSC/MIX/IF Amplifier Block

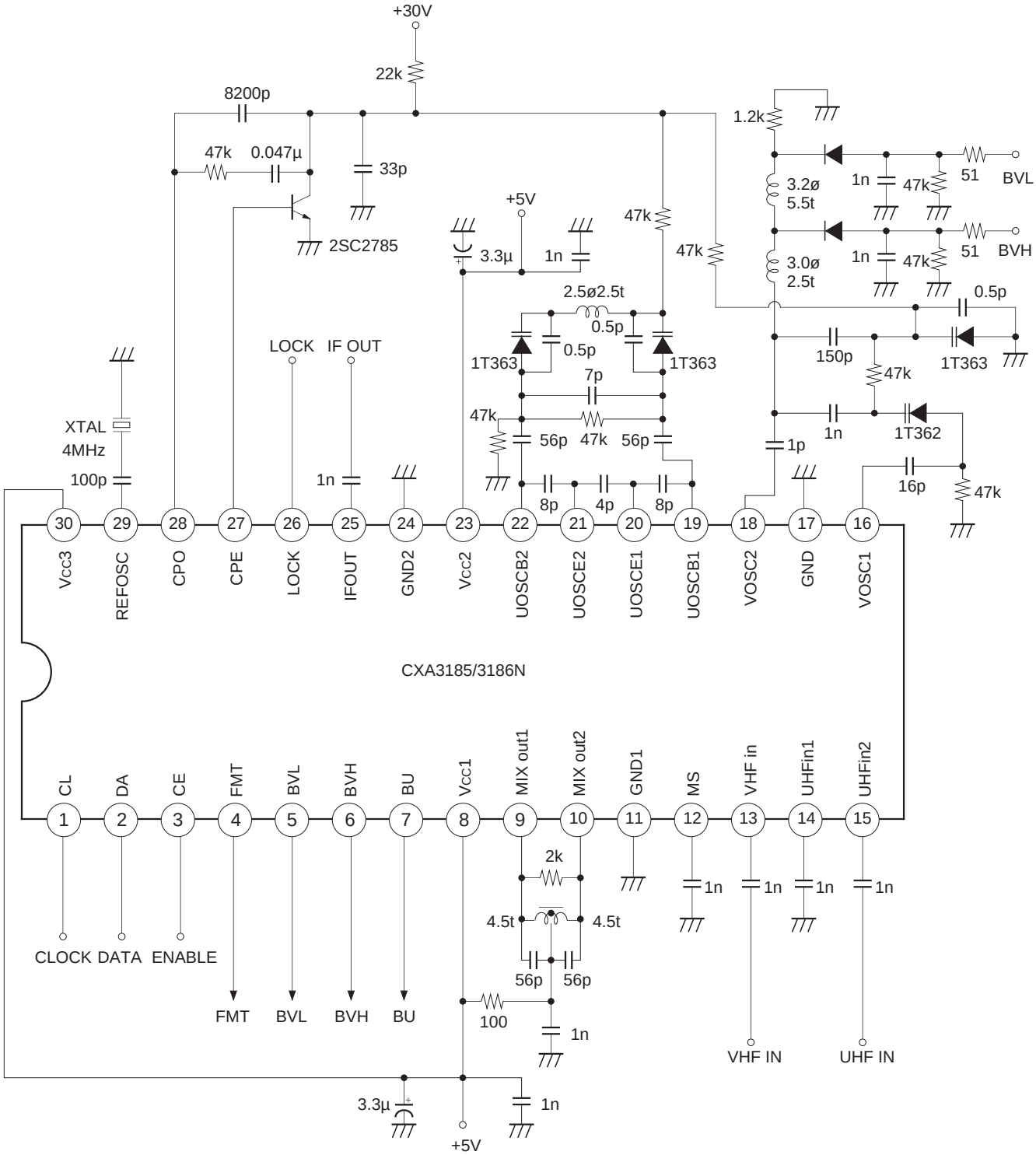
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain *1	CG1	VHF operation f_{RF} = 55 MHz	21	24	27	dB
	CG2	VHF operation f_{RF} = 360 MHz	22	25	28	dB
	CG3	UHF operation f_{RF} = 360 MHz	26	29	32	dB
	CG4	UHF operation f_{RF} = 800 MHz	27	30	33	dB
Noise figure *1, *2	NF1	VHF operation f_{RF} = 55 MHz		12	15	dB
	NF2	VHF operation f_{RF} = 360 MHz		11	14	dB
	NF3	UHF operation f_{RF} = 360 MHz		8.5	12.5	dB
	NF4	UHF operation f_{RF} = 800 MHz		9.5	13.5	dB
1 % cross modulation *1, *3	CM1	VHF operation f_D = 55 MHz, f_{UD} = ±12 MHz	97	101		dBµ
	CM2	VHF operation f_D = 360 MHz, f_{UD} = ±12 MHz	96	100		dBµ
	CM3	UHF operation f_D = 360 MHz, f_{UD} = ±12 MHz	92	96		dBµ
	CM4	UHF operation f_D = 800 MHz, f_{UD} = ±12 MHz	88	92		dBµ
Maximum output power	Pomax	50 Ω load saturation output	+5	+10		dBm
Switch ON drift *4	Δfsw1	VHF operation f_{OSC} = 100 MHz Δf from 3 s to 3 min after switch ON			±300	kHz
	Δfsw2	VHF operation f_{OSC} = 405 MHz Δf from 3 s to 3 min after switch ON			±400	kHz
	Δfsw3	UHF operation f_{OSC} = 405 MHz Δf from 3 s to 3 min after switch ON			±400	kHz
	Δfsw4	UHF operation f_{OSC} = 845 MHz Δf from 3 s to 3 min after switch ON			±500	kHz
Supply voltage drift *4	Δfst1	VHF operation f_{OSC} = 100 MHz Δf when V_{CC} 5 V changes ±5 %			±150	kHz
	Δfst2	VHF operation f_{OSC} = 405 MHz Δf when V_{CC} 5 V changes ±5 %			±250	kHz
	Δfst3	UHF operation f_{OSC} = 405 MHz Δf when V_{CC} 5 V changes ±5 %			±200	kHz
	Δfst4	UHF operation f_{OSC} = 845 MHz Δf when V_{CC} 5 V changes ±5 %			±250	kHz

*1 Measured value for untuned inputs.
*2 Noise figure is the direct-reading value of NF meter in DSB.
*3 Desired signal (f_D) input level is –30 dBm. Undesired signal (f_{UD}) is 100 kHz, 30 % AM.
The measurement value is undesired signal level, it measured with a spectrum analyzer at S/I=46 dBm.
*4 Value when the PLL is not operating.

PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
CL and DA pins						
"H" level input voltage	V_{IH}		3		V_{CC}	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	$V_{IH} = V_{CC}$		0	–0.1	µA
"L" level input current	I_{IL}	V_{IL} = GND		–1	–2	µA
CE pins						
"H" level input voltage	V_{IHE}		3		V_{CC}	V
"L" level input voltage	V_{ILE}		GND		1.5	V
"H" level input current	I_{IHE}	$V_{IHE}=V_{CC}$		100	130	µA
"L" level input current	I_{ILE}	V_{ILE}=GND		–30	–45	µA
CPO (charge pump)						
Output current	I_{CPO}		±35	±50	±75	µA
Leak current	LeakCP				30	nA
LOCK						
"H" output voltage	V_{LOCKH}	When locked	V_{CC}–0.5		V_{CC}	V
"L" output voltage	V_{LOCKL}	When unlocked	0		0.5	V
REFOSC						
Oscillator frequency range	F_{XTOSC}		3		12	MHz
Input capacitance	C_{XTOSC}		17.5	19	20.5	pF
Drive level	V_{XTOSC}		200	400		mVp-p
BVL, BVH, BU (Band SW)						
Output current	$I_{BS}1$	When ON			–25	mA
Saturation voltage	$V_{SAT}1$	When ON Sink current = 20 mA		100	200	mV
Leak current	LeakBS1	When OFF		0.5	3	µA
FMT (Band SW)						
Output current	$I_{BS}2$	When ON			–7	mA
Saturation voltage	$V_{SAT}2$	When ON Sink current = 5 mA		75	150	mV
Leak current	LeakBS2	When OFF		0.03	0.1	µA
Bus timing						
Data setup time	t_{SD}	See Timing Chart on Page 15	300			ns
Data hold time	t_{HD}	See Timing Chart on Page 15	600			ns
Enable waiting time	t_{WE}	See Timing Chart on Page 15	300			ns
Enable setup time	t_{SE}	See Timing Chart on Page 15	300			ns
Enable hold time	t_{HE}	See Timing Chart on Page 15	600			ns

Electrical Characteristics Measurement Circuit



Description of Functions

The CXA3185/3186N is a terrestrial wave broadcast tuner IC which converts frequencies to IF in order to tune and detect only the desired reception frequency of VHF, CATV and UHF band signals.

In addition to the mixer, local oscillator and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillator frequency control onto a single chip.

The functions of the various circuits are described below.

1. Mixer circuit

This circuit outputs the frequency difference between the signal input to VHFIN or UHFIN and the local oscillation signal.

2. Local oscillator circuit

A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.

3. IF amplifier circuit

This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.

4. PLL circuit

This PLL circuit fixes the local oscillator frequency to the desired frequency. It consists of a prescaler, main divider, reference divider, phase comparator, charge pump and reference oscillator. The control format supports the 3-wire bus format. The following four modes can be selected according to the combination of the frequency division values of the main and reference dividers.

Mode	Main divider	Reference divider
A-0	15 bit	1024 fixed
A-1	14 bit	512 fixed
A-2	15 bit	640 fixed
A-3/4	15 bit	512 fixed

Description of Analog Block Operation

(See the Electrical Characteristics Measurement Circuit.)

VHF oscillator circuit

- This circuit is a differential amplifier type oscillator circuit. Pin 18 is the output and Pin 16 is the input. Oscillation is performed by connecting an LC resonance circuit including a varicap to Pin 18 via coupled capacitance, inputting to Pin 16 with feedback capacitance, and applying positive feedback.
- The amplifier between Pins 16 and 18 has an extremely high gain. Therefore, care should be taken to avoid creating parasitic capacitance, resistance or other feedback loops as this may produce abnormal oscillation.

VHF mixer circuit

- The mixer circuit employs a double balance mixer with little local oscillation signal leakage. The input format is base input type, with Pin 12 grounded and the RF signal input to Pin 13.
- The RF signal is inserted from the oscillator, converted to IF frequency and output from Pins 9 and 10.
- Pins 9 and 10 are open collectors, so power must be supplied externally. The electric potential of Pins 9 and 10 at this time must be DC 4.0 V or more.

UHF oscillator circuit

- This oscillator circuit is designed so that two collector ground type Colpitts oscillators perform differential oscillation operation via an LC resonance circuit including a varicap. Connect resonance capacitance which consists of colpitts oscillator between Pins 19 and 20, Pins 20 and 21, and Pins 21 and 22. Then an LC resonance circuit including a varicap diode is connected between Pins 19 and 22.

UHF mixer circuit

- This circuit employs a double balance mixer like the VHF mixer circuit. The input format is base input type, with Pins 14 and 15 as the RF input pins. The input method can be selected from balanced input consisting of differential input to Pins 14 and 15 or unbalanced input consisting of grounding Pin 14 via a capacitor and input to Pin 15.
- Pins 9 and 10 are the mixer outputs.
- Pins 9 and 10 are open collectors, so power must be supplied externally. The electric potential of Pins 9 and 10 at this time must be DC 4.0 V or more.

IF amplifier circuit

- The signals frequency converted by the mixer are output from Pins 9 and 10, and at the same time are AC coupled inside the IC and input to the IF amplifier.
- Single-tuned filters are connected to Pins 9 and 10 in order to improve the interference characteristics of the IF amplifier.
- The signal amplified by the IF amplifier is output from Pin 25. The output impedance is approximately 75 Ω.

Description of PLL Block

The PLL on this IC supports the 3-wire bus control format.

The serial data is input to the DA, CL and CE pins. The data is loaded to the shift register at the clock rise, and latched at the enable fall.

Symbol	3-wire bus control
CE	Enable input
CL	Clock input
DA	Data input
LOCK	Lock signal output

1) Mode Setting Method

The modes for each frequency step are set according to the MS pin voltage.

Mode	MS pin voltage	Main divider	Reference divider	Reference frequency*	Frequency step*	Control word length
A-0	0 to 0.15Vcc	15 bit	1024	3.90625 kHz	31.25 kHz	Total 19 bits
A-1	OPEN	14 bit	512	7.8125 kHz	62.5 kHz	Total 18 bits
A-2	0.45Vcc to 0.55Vcc	15 bit	640	6.25 kHz	50 kHz	Total 19 bits
A-3	0.65Vcc to 0.75Vcc	15 bit	512	7.8125 kHz	62.5 kHz	Total 19 bits
A-4	0.85Vcc to Vcc	15 bit	512	7.8125 kHz	62.5 kHz	Total 27 bits

∗ Frequency step is for when X'tal OSC = 4 MHz.

2) Programming

- The VCO lock frequency is obtained according to the following formula.

  $fosc = fref \times 8 \times (32\ M + S)$

  fosc : local oscillator frequency
  fref : reference frequency
  8 : prescaler fixed frequency division ratio
  M : main divider frequency division ratio
  S : swallow counter frequency division ratio

  The variable frequency division ranges of M and S are as follows, and are set as binary.

  $32 \leq M \leq 1023$ ($32 \leq M \leq 511$ for A-1 mode)

  $0 \leq S \leq 31$

- The PLL control data is comprised of the above frequency data and the band switch control data.

2-1) The CXA3185N control format is as follows.

2-1-1 : A-0/A-2/A-3 Modes (19-bit data format)

Front bit ←MSB LSB→

BU	FMT	BVH	BVL	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0

2-1-2 : A-1 Mode (18-bit data format)

Front bit ←MSB LSB→

BU	FMT	BVH	BVL	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0

2-1-3 : A-4 Mode (27-bit data format)

Front bit ←MSB LSB→

BU	FMT	BVH	BVL	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0
X	CP	T1	CD	X	R1	R0	X											

∗) X: Don’t care

S0 to : swallow counter frequency division ratio setting
M0 to : main divider frequency division ratio setting
BVL : VL band switch control (output PNP Tr ON when “1”)
BVH : VH band switch control (output PNP Tr ON when “1”)
FMT : FM trap switch control (output PNP Tr ON when “1”)
BU : UHF band switch control (output PNP Tr ON when “1”)
CP : charge pump current switching (200 µA when “1”, 50 µA when “0”)
T1 : test mode selection (when “1”)
CD : charge pump OFF (when “1”)
R0, R1: reference divider frequency division ratio setting (See the table below.)

Reference Divider Frequency Division Ratio Table

R1	R0	Reference divider
0	1	1024
1	1	512
X	0	640

∗) X: Don’t care

2-2) The CXA3186N control format is as follows.
The BU and FMT data order is switched for the CXA3185N.

In this case the control format is as follows.

2-2-1 : A-0/A-2/A-3 Modes (19-bit data format)

Front bit ←MSB LSB→

FMT	BU	BVH	BVL	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0

2-2-2 : A-1 Mode (18-bit data format)

Front bit ←MSB LSB→

FMT	BU	BVH	BVL	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0

2-2-3 : A-4 Mode (27-bit data format)

Front bit ←MSB LSB→

FMT	BU	BVH	BVL	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S4	S3	S2	S1	S0
X	CP	T1	CD	X	R1	R0	X											

∗) X: Don’t care

S0 to : swallow counter frequency division ratio setting
M0 to : main divider frequency division ratio setting
BVL : VL band switch control (output PNP Tr ON when “1”)
BVH : VH band switch control (output PNP Tr ON when “1”)
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BU : UHF band switch control (output PNP Tr ON when “1”)
CP : charge pump current switching (200 µA when “1”, 50 µA when “0”)
T1 : test mode selection (when “1”)
CD : charge pump OFF (when “1”)
R0, R1: reference divider frequency division ratio setting (See the table below.)

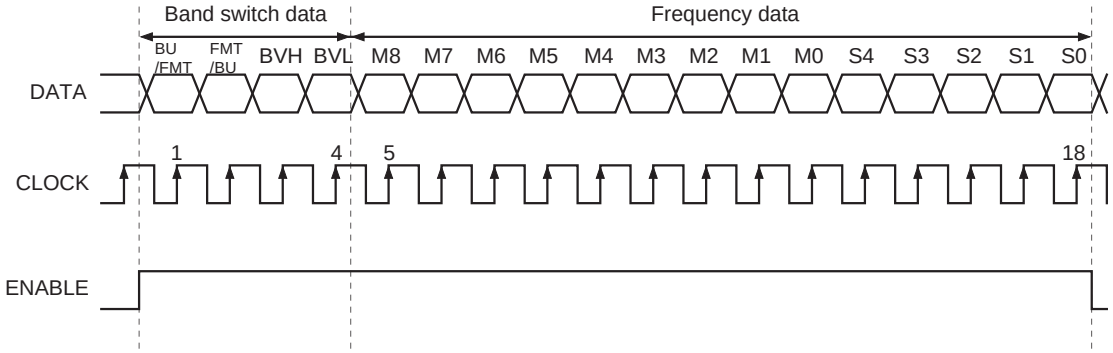
Reference Divider Frequency Division Ratio Table

R1	R0	Reference divider
0	1	1024
1	1	512
X	0	640

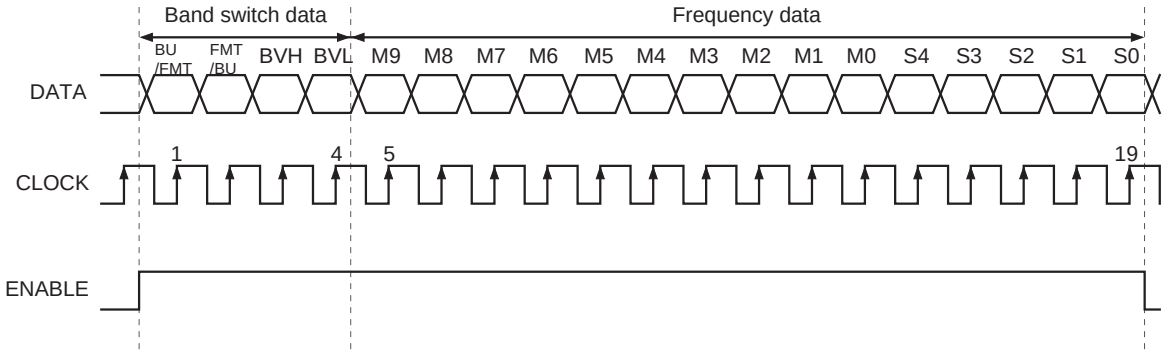
∗) X: Don't care

3) 3-wire Bus Data Format

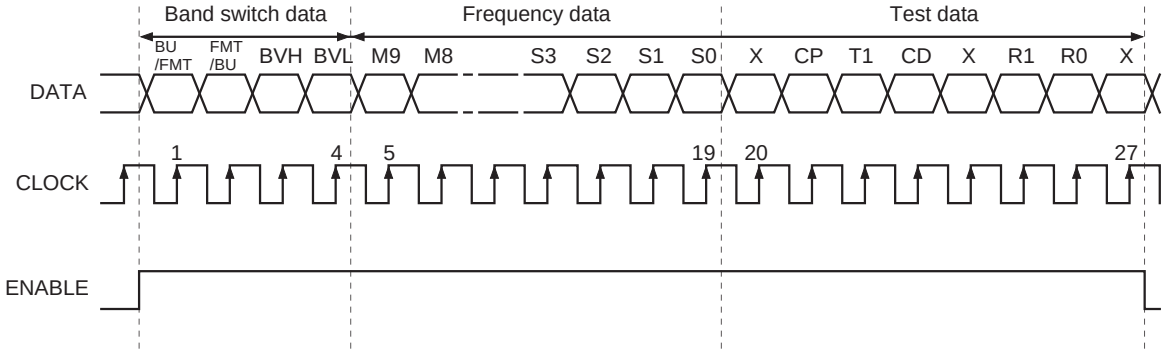
A-1 Mode (18-bit data format)



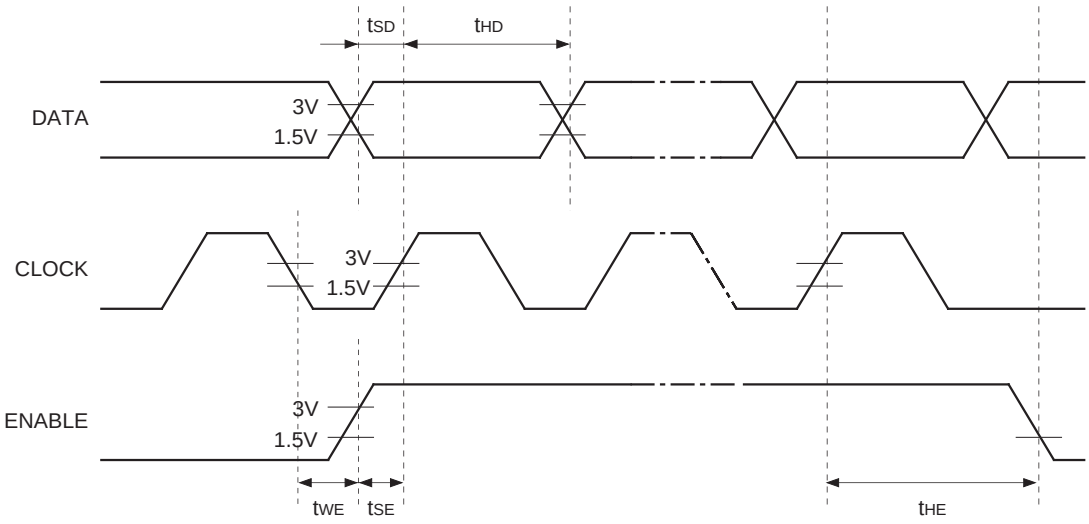
A-0/A-2/A-3 Modes (19-bit data format)



A-4 Mode (27-bit data format)

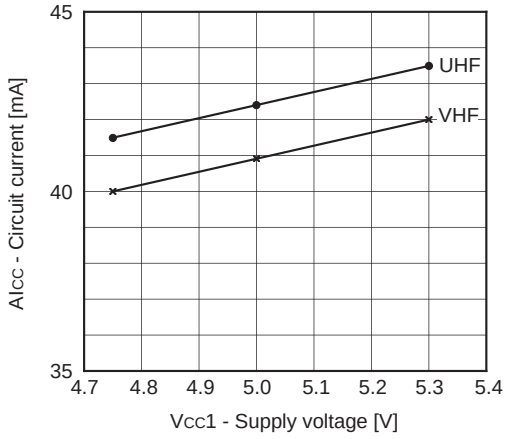


4) Bus Timing Chart

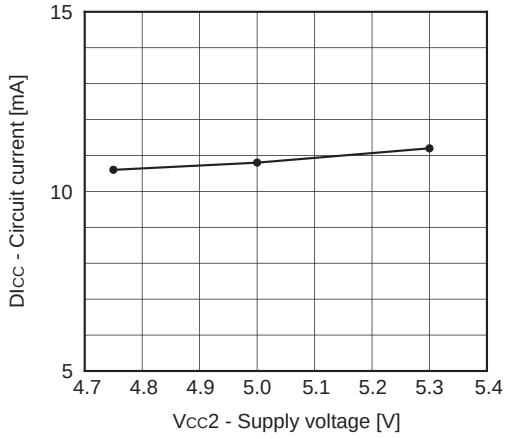


tSD = Data setup time
tHD = Data hold time
tSE = Enable setup time
tHE = Enable hold time
tWE = Enable waiting time

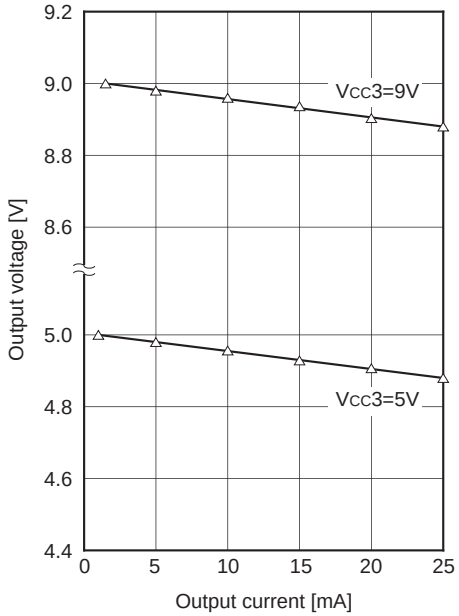
Circuit current vs. Supply voltage 1



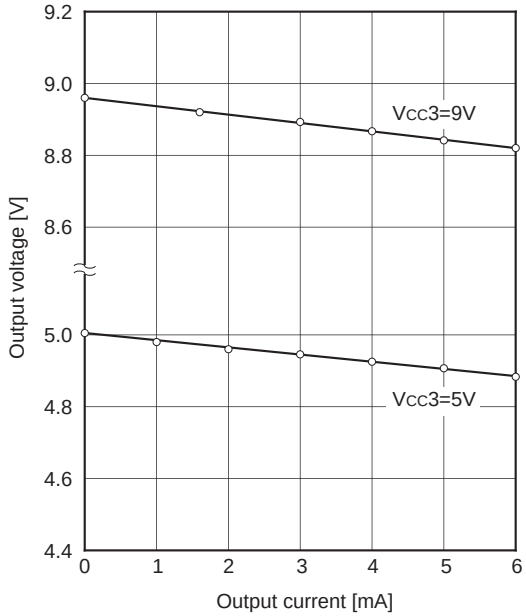
Circuit current vs. Supply voltage 2



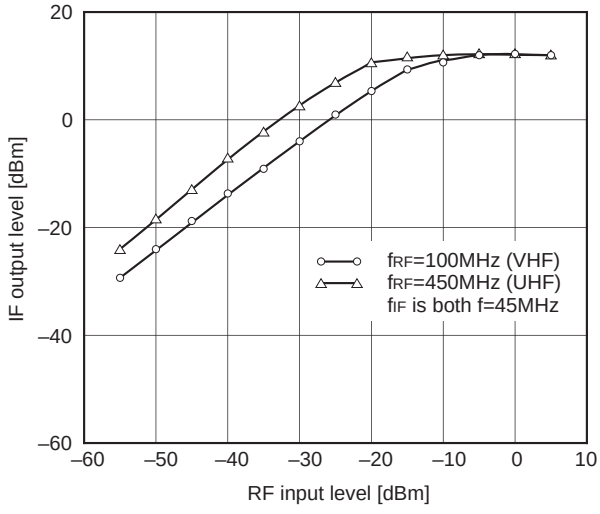
Band SW output voltage vs. Output current (BU, BVH, BVL)



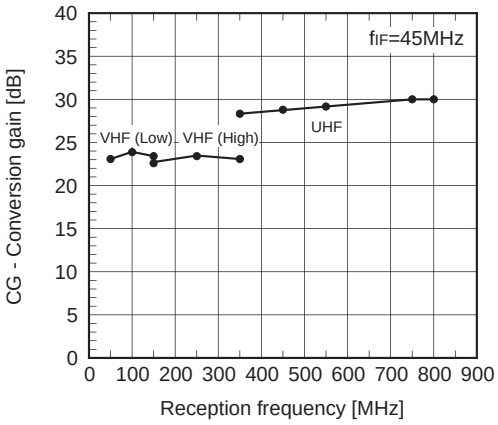
Band SW output voltage vs. Output current (FMT)



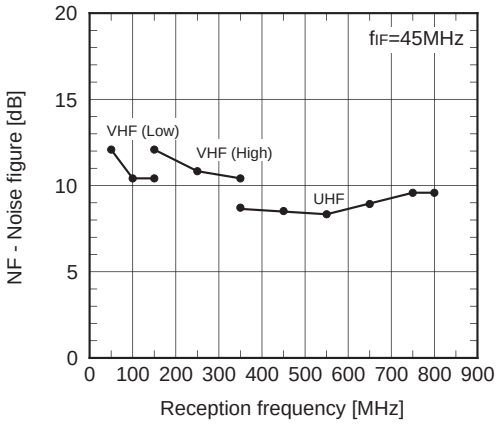
I/O characteristics (Untuned input)



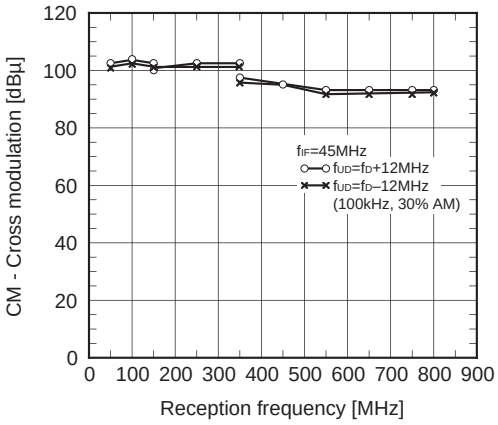
Conversion gain vs. Reception frequency (Untuned input)



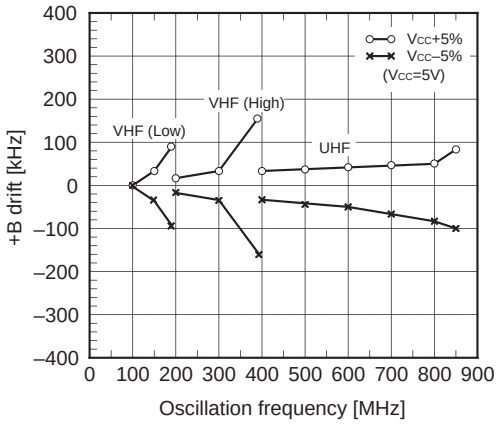
Noise figure vs. Reception frequency (Untuned input, in DSB)



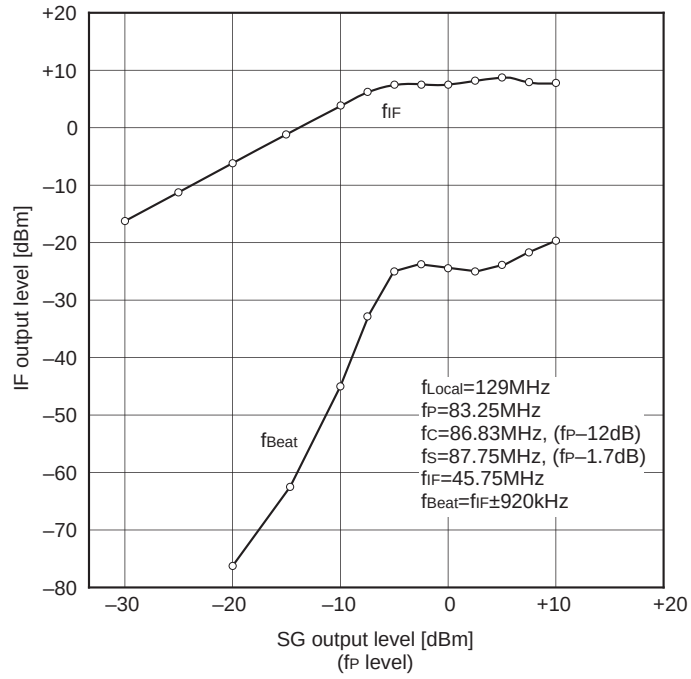
Next adjacent cross modulation vs. Reception frequency (Untuned input)



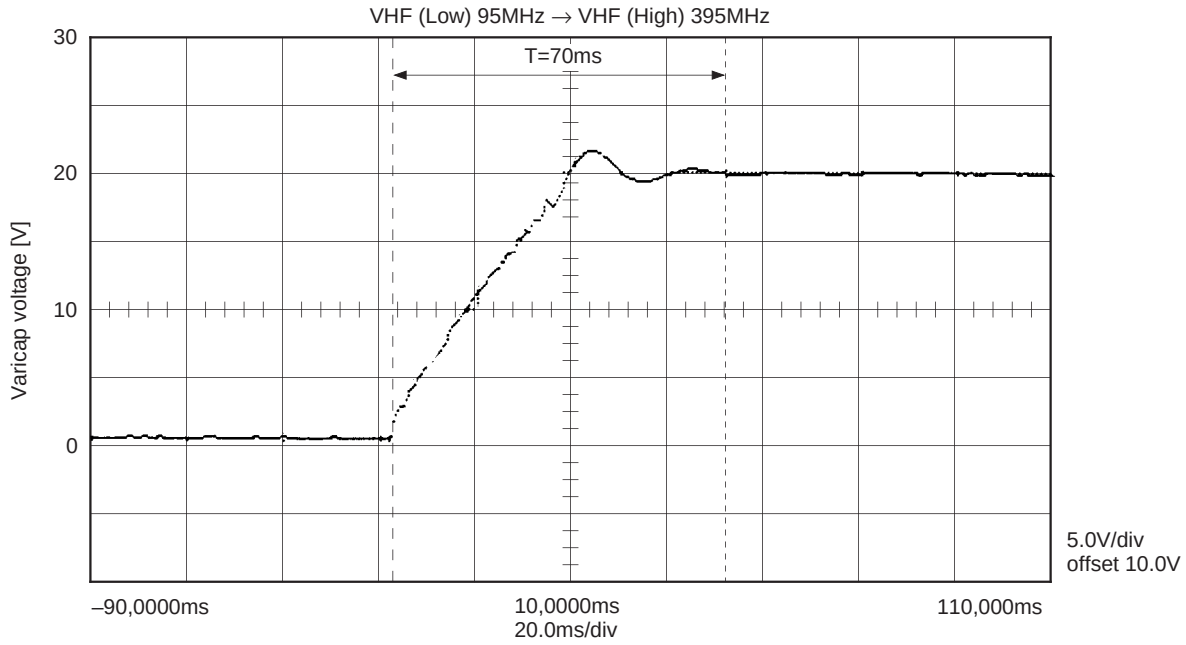
Oscillation frequency power supply fluctuation (PLL off)

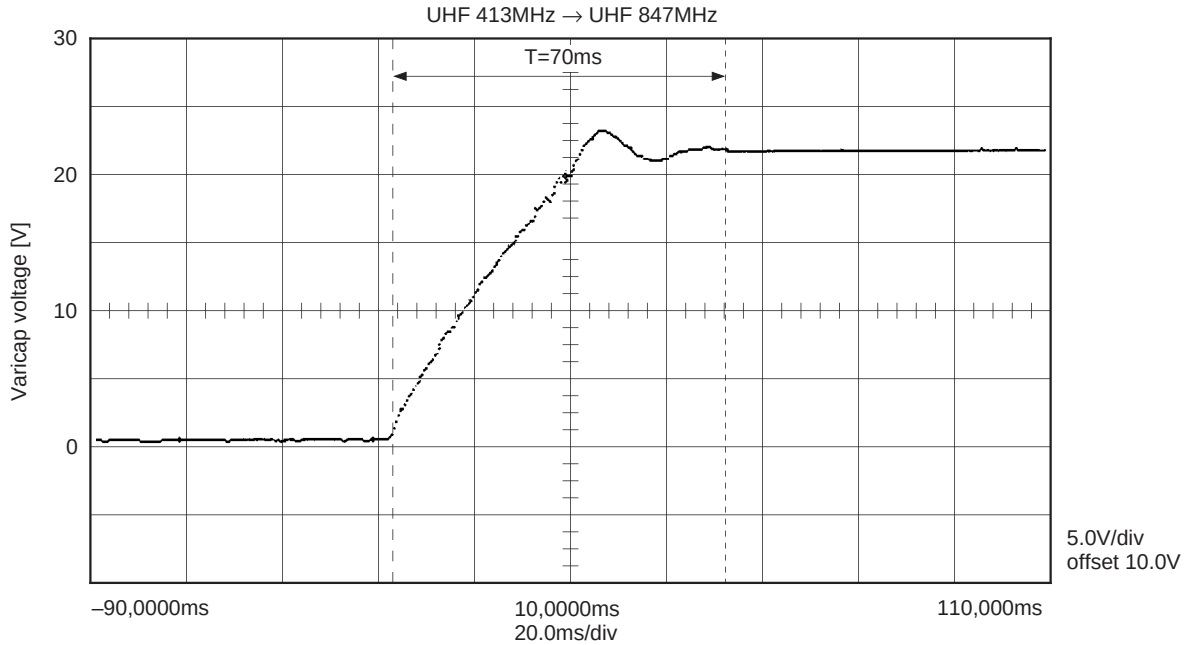


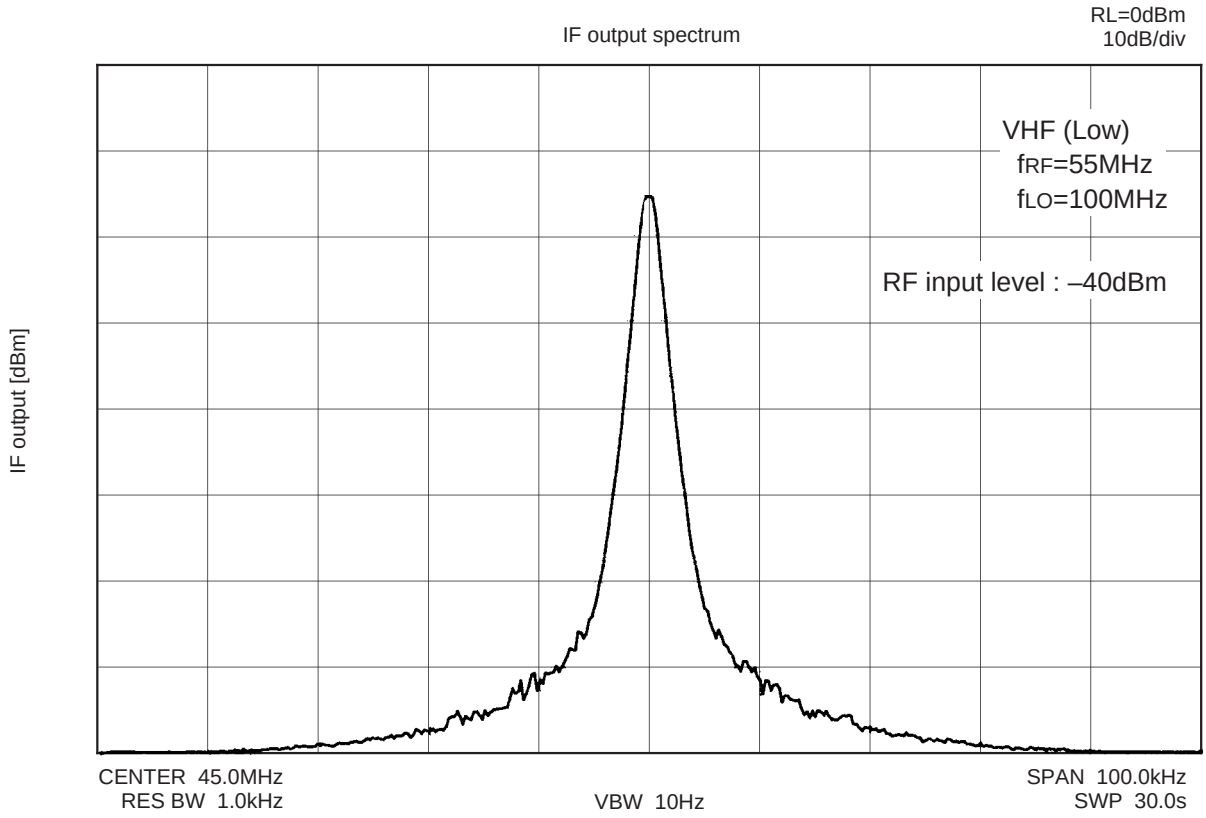
PCS beat characteristics

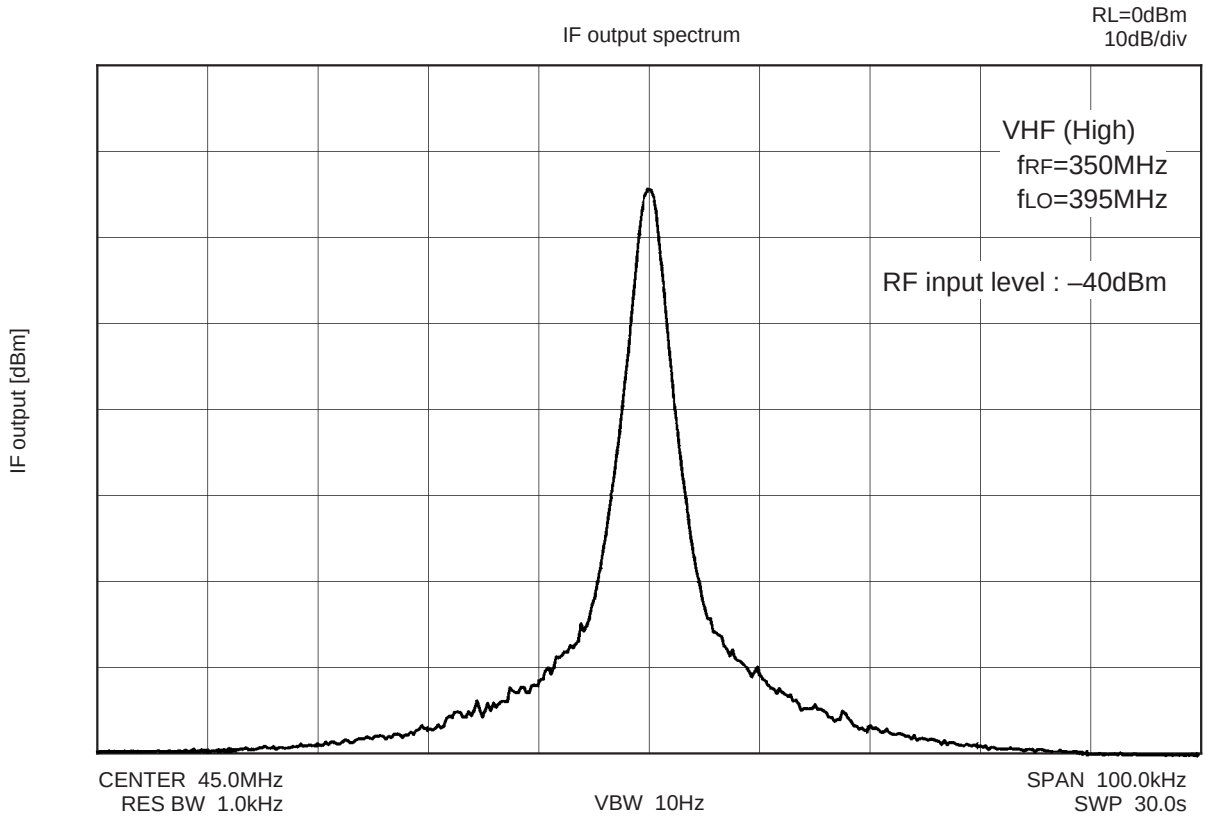


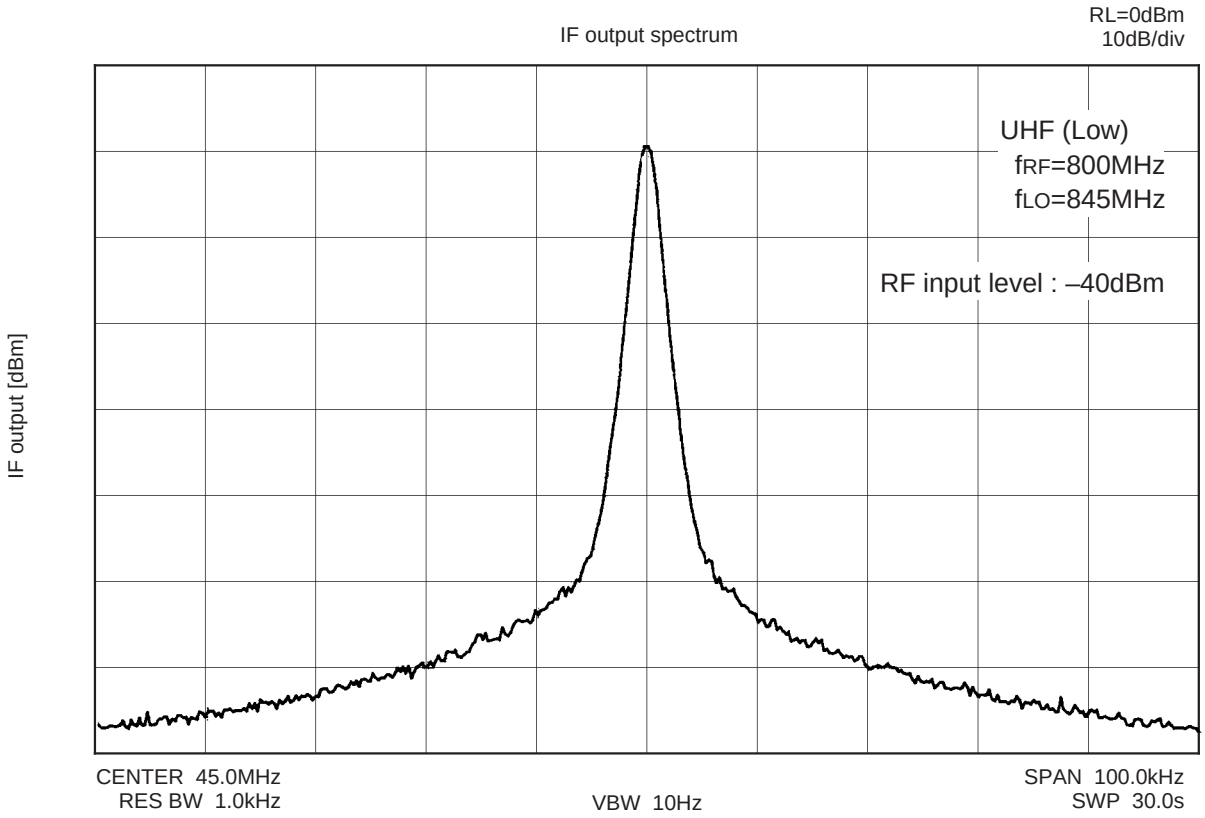
Tuning Response Time



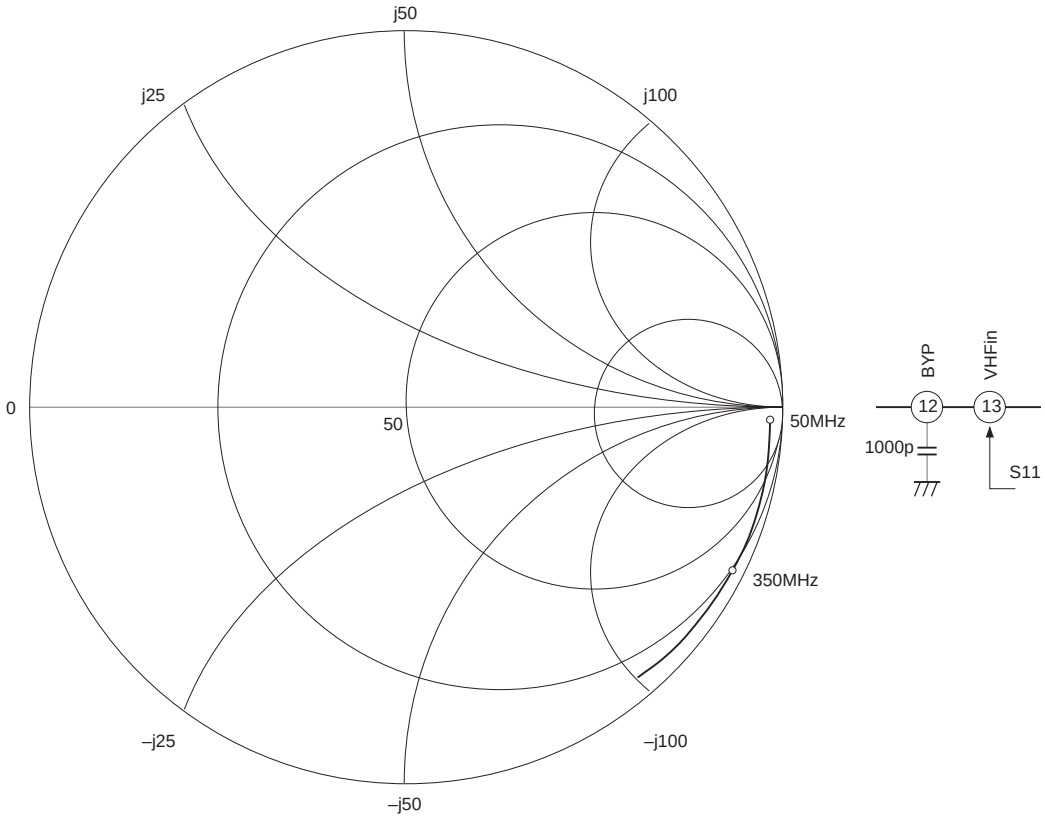



IF output spectrum
RL=0dBm
10dB/div
VHF (Low)
fRF=55MHz
fLO=100MHz
RF input level : –40dBm
IF output [dBm]
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s

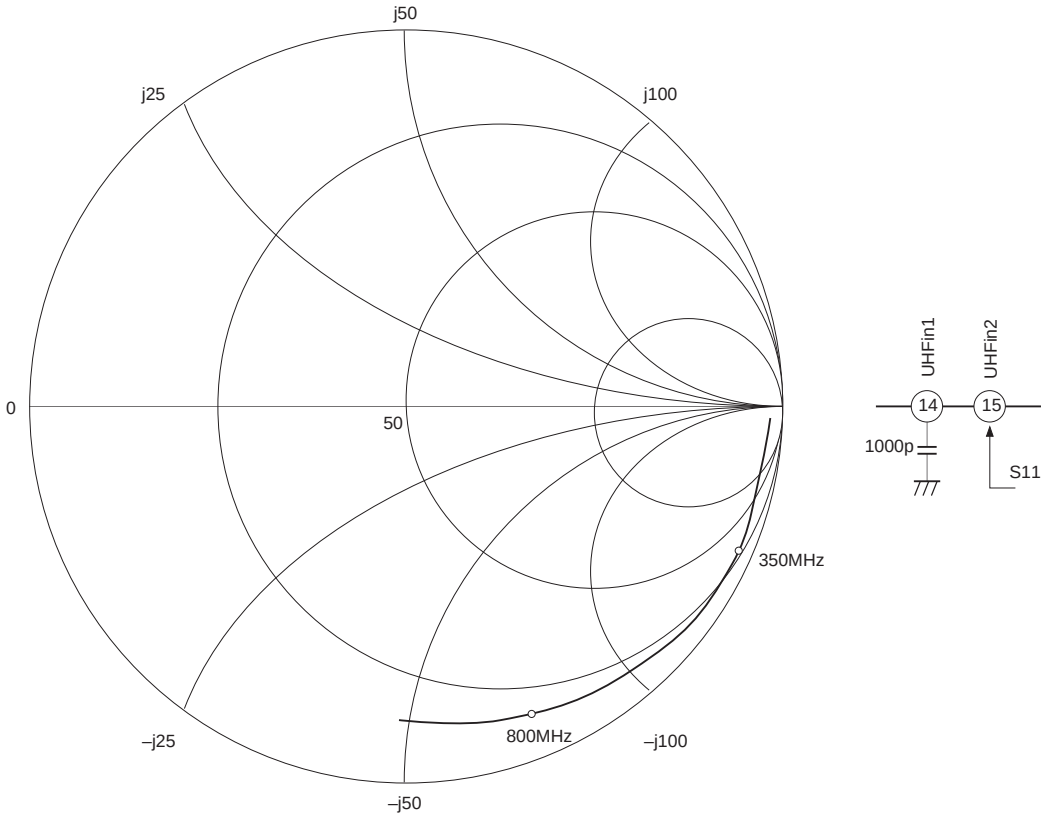

IF output spectrum
RL=0dBm
10dB/div
VHF (High)
fRF=350MHz
fLO=395MHz
RF input level : –40dBm
IF output [dBm]
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s


IF output spectrum
RL=0dBm
10dB/div
UHF (Low)
fRF=800MHz
fLO=845MHz
RF input level : –40dBm
IF output [dBm]
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s

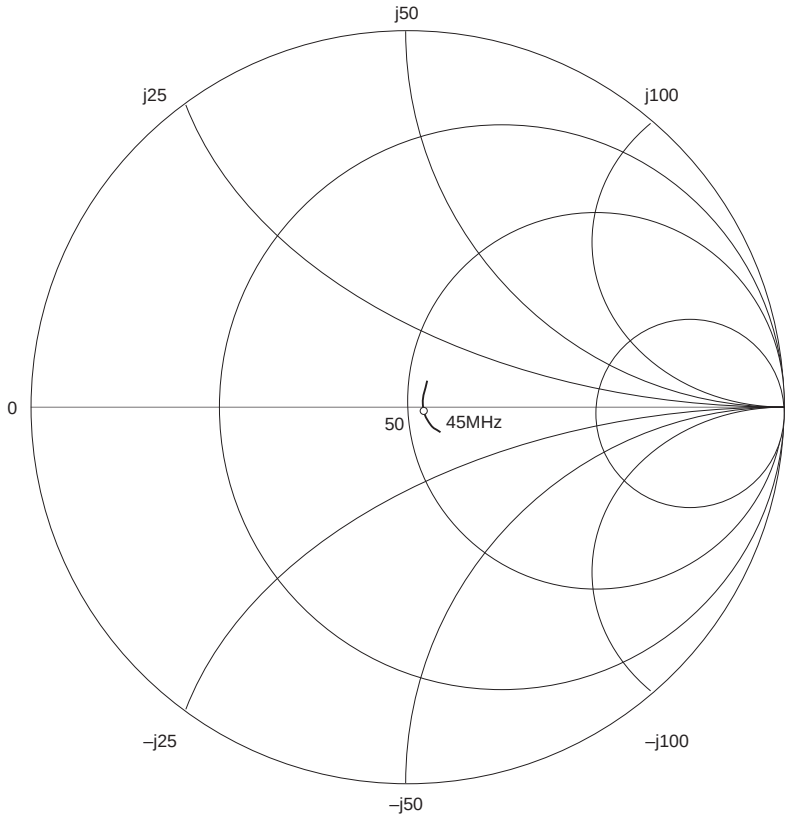
VHF Input Impedance



UHF Input Impedance

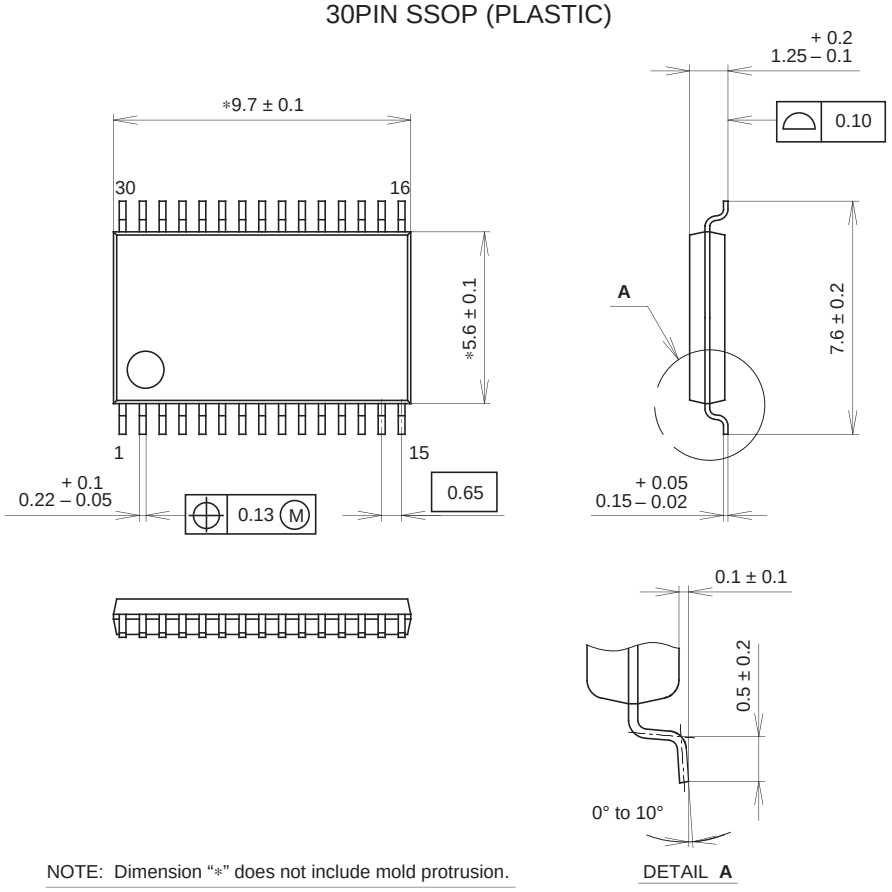


IF Output Impedance



Package Outline Unit : mm

30PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).