

RX Gain Control Amplifier

Description

CXA3201N is an RX gain control amplifier suitable for CDMA cellular/PCS phone.

Features

- Wide gain control range
- Linear gain slope
- Wideband operation (50MHz to 300MHz)
- Very small package (16 Pin SSOP)
- Low voltage operation
- Two input ports
- Power save function included

Absolute Maximum Ratings

- | | | | |
|-------------------------------------|-----------|------------------------|----|
| • Supply voltage | V_{CC} | 6 | V |
| • Operating temperature | T_{opr} | -55 to +125 | °C |
| • Storage temperature | T_{stg} | -65 to +150 | °C |
| • Allowable Power dissipation | P_D | 330 | mW |
| • Supply voltage range | | -0.3 to 6 | V |
| • Logic input voltage | | -0.3 to $V_{CC} + 0.3$ | V |
| • Signal input voltage | | -0.3 to $V_{CC} + 0.3$ | V |
| • Differential signal input voltage | | 0 to 2.5 | V |

Operating Condition

- | | | | |
|----------------|----------|------------|---|
| Supply voltage | V_{CC} | 2.7 to 3.8 | V |
|----------------|----------|------------|---|

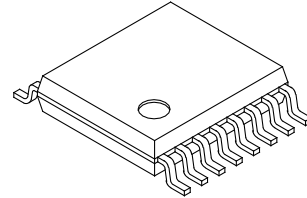
Applications

CDMA cellular/PCS phone

Structure

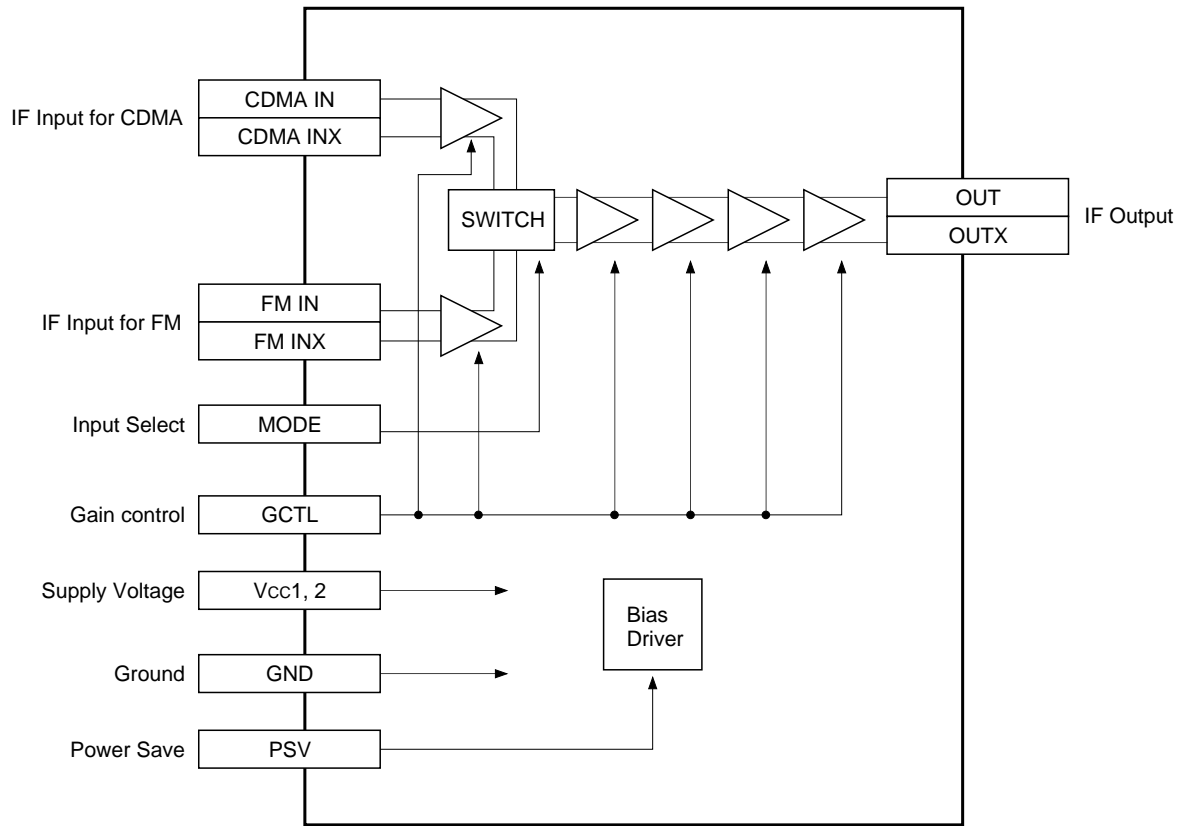
Bipolar silicon monolithic IC

16 pin SSOP (Plastic)

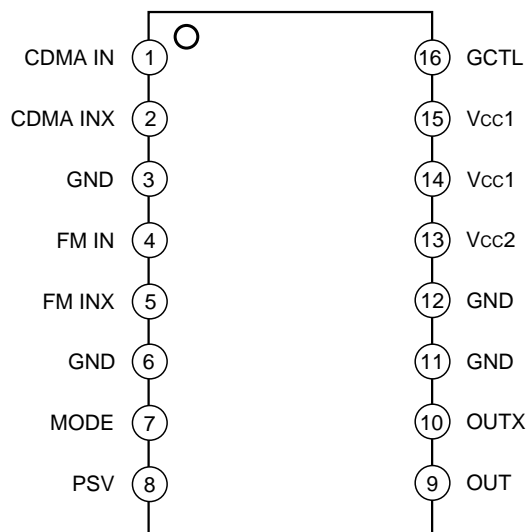


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Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage TYP (V)	Equivalent circuit	Description
1	CDMA IN	1.15		Differential input pins for received CDMA IF signal.
2	CDMA INX	1.15		
3 6 11 12	GND	0		Ground.
4	FM IN	1.15		Differential input pins for received FM IF signal.
5	FM INX	1.15		
7	MODE	—		Input select pin. CDMA IN for High FM IN for Low.
8	PSV	—		Power save function pin. High: Active Low: Power save

Pin No.	Symbol	Pin voltage TYP (V)	Equivalent circuit	Description
9	OUT	—		Differential output pins for received CDMA IF signal. Open collector output.
10	OUTX	—		
13	Vcc2	3.0		Positive power supply for output stage.
14 15	Vcc1	3.0		Positive power supply.
16	GCTL	—		Gain control pin.

Electrical Characteristics

DC Characteristics

(V_{CC} = 3.0V, T_a = 27°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I _{cc1}	V _{psv} = 3.0V, V _{gctl} = 1.5V, Pin 13, 14	7	10.2	15	mA
Current consumption 2	I _{cc2}	V _{psv} = 0 V, V _{gctl} = 1.5V, Pin 13, 14	10	27	50	μA
Input current pin 7H	I _{modeH}	V _{mode} = 3.0V			1	
Input current pin 7L	I _{modeL}	V _{mode} = 0.5V	-1			
Input current pin 8H	I _{psvH}	V _{psv} = 3.0V			1	
Input current pin 8L	I _{psvL}	V _{psv} = 0 V	-15			
Input current pin 16H	I _{gctlH}	V _{gctl} = 3.0V			1	
Input current pin 16L	I _{gctlL}	V _{gctl} = 0.5V	-1			
MODE high voltage	V _{mH}	Pin 7	2.5			V
MODE low voltage	V _{mL}	Pin 7			0.5	
PSV high voltage	V _{psH}	Pin 8	2.5			
PSV low voltage	V _{psL}	Pin 8			0.5	

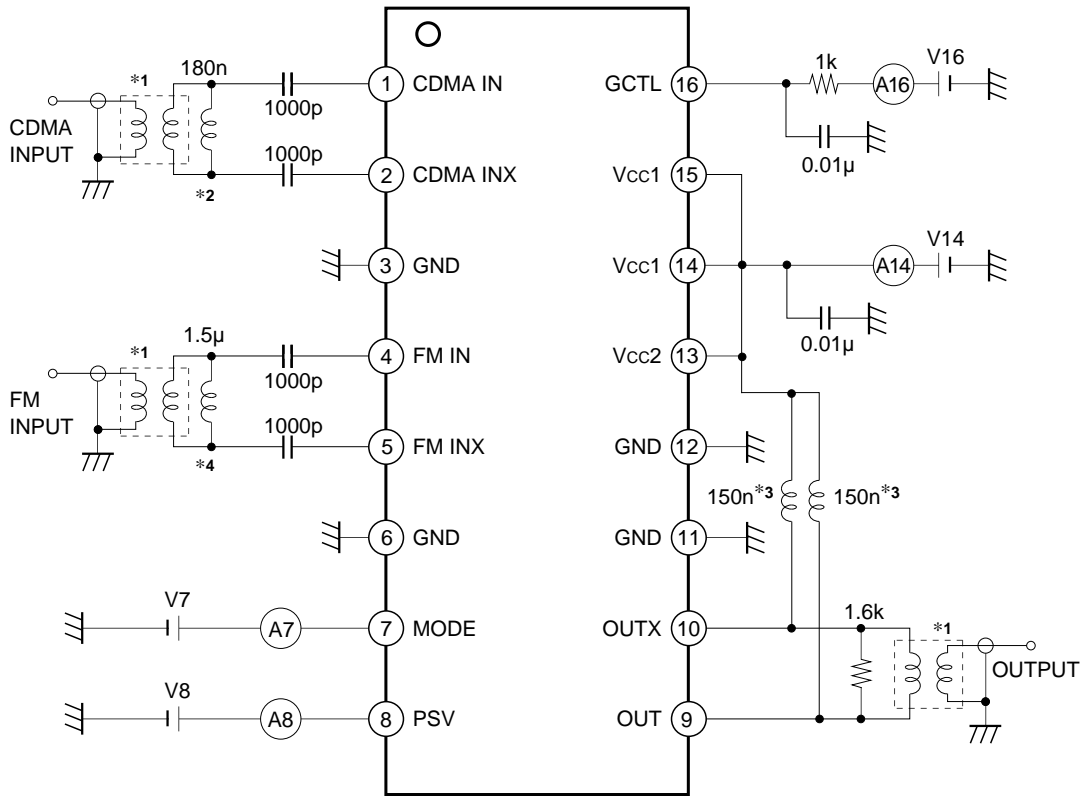
AC Characteristics

(V_{CC} = 3.0V, T_a = 27°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency range	F _r		50		300	MHz
Gain CDMA2.4	G _{CDMA2.4}	V _{mode} = "H", f = 210.38MHz, V _{gctl} = 2.4V	42	46	50	dB
Gain CDMA1.5	G _{CDMA1.5}	V _{mode} = "H", V _{gctl} = 1.5V	-7	-3	1	
Gain CDMA0.6	G _{CDMA0.6}	V _{mode} = "H", V _{gctl} = 0.6V	-59	-55	-51	
CDMA Gain slope	G _{CLIN}	V _{mode} = "H", Gain CDMA at V _{gctl} = 2.0V – Gain CDMA at V _{gctl} = 1.0V	58	61	64	dB/V
Gain FM2.4	G _{FM2.4}	V _{mode} = "L", f = 85.38MHz, V _{gctl} = 2.4V	42	46	50	dB
Gain FM1.5	G _{FM1.5}	V _{mode} = "L", V _{gctl} = 1.5V	-7	-3	1	
Gain FM0.6	G _{FM0.6}	V _{mode} = "L", V _{gctl} = 0.6V	-59	-55	-51	
FM Gain slope	G _{FMLIN}	V _{mode} = "L", Gain FM at V _{gctl} = 2.0V – Gain FM at V _{gctl} = 1.0V	58	61	64	dB/V
Input level 3rd order intercept point	IIP3	V _{mode} = "H", G _{CDMA} = 40dB* ¹ f ₁ = 209.38MHz, f ₂ = 211.38MHz Measure of 210.38MHz	-42	-38		dBm
Noise Figure	NF	V _{mode} = "H", G _{CDMA} = 40dB* ¹ Measure of 210.38MHz		5	8	dB

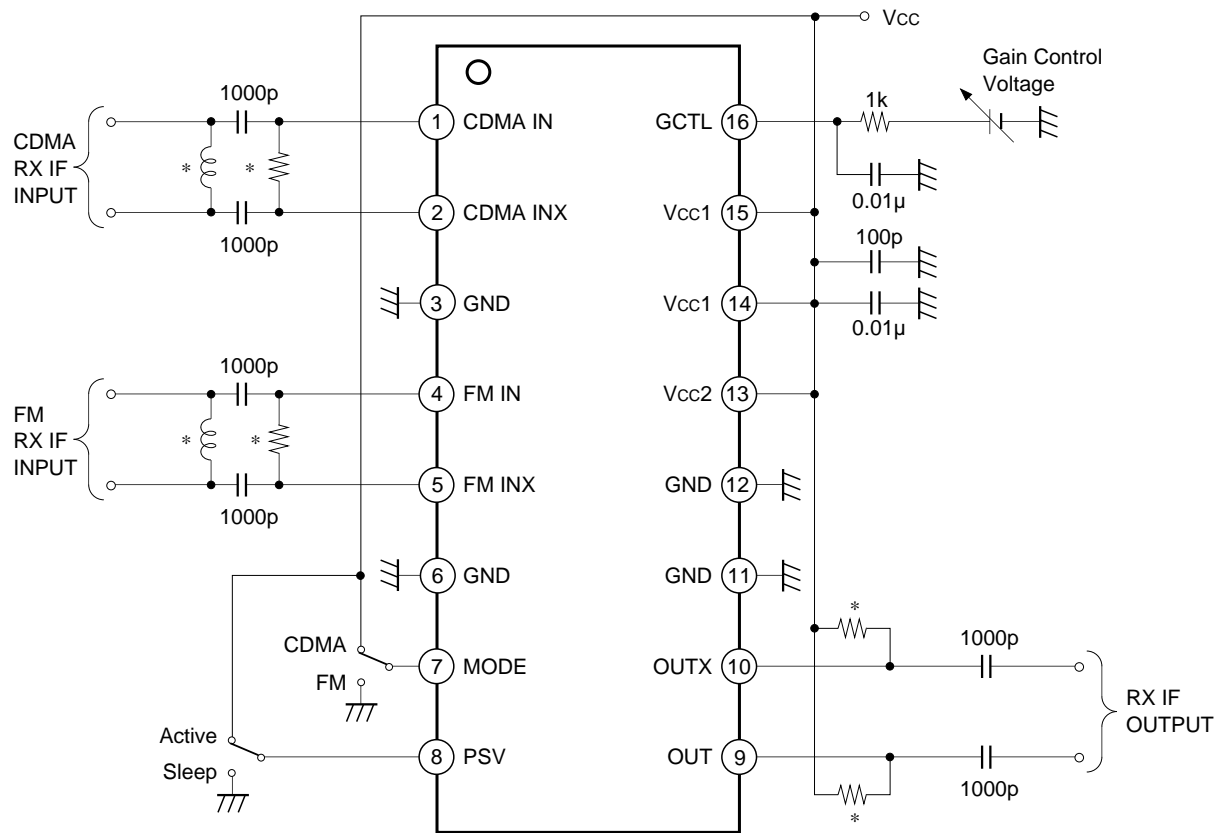
*1 Adjust GCTL voltage, and set the overall gain to 40dB.

Measurement Circuit



- *1 TOKO, Inc. B5FL 616DS-1135
- *2 Coilcraft, Inc. 0805HS-181TKBC
- *3 Coilcraft, Inc. 0805HS-151TKBC
- *4 Coilcraft, Inc. 1008CS-152XKBC

Application Circuit



* Must be adjusting values to result a best impedance matching between BPF filter and this IC.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Design Reference Values

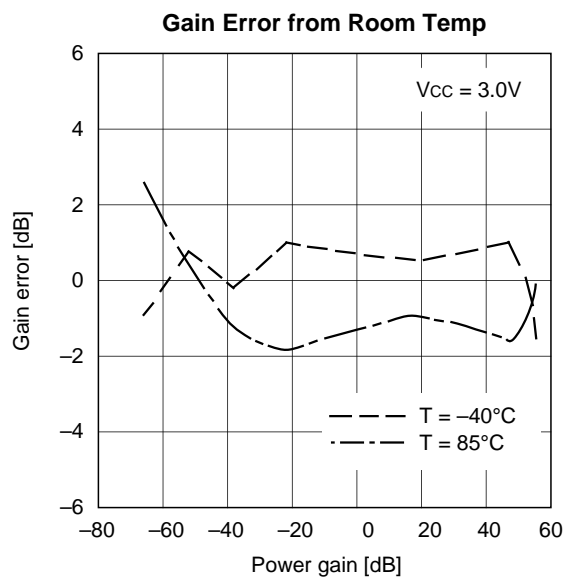
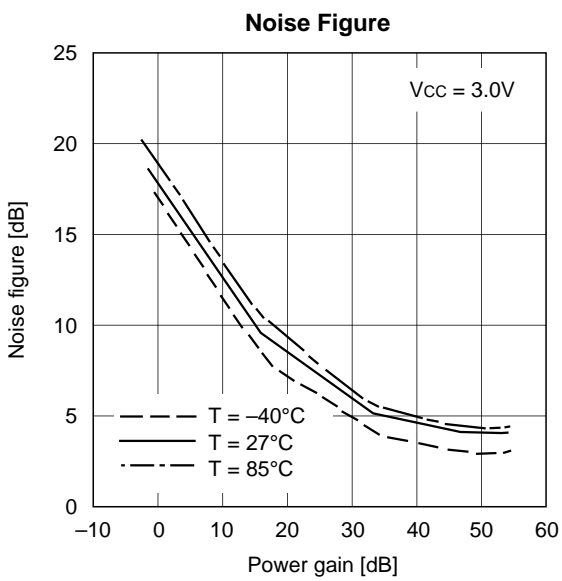
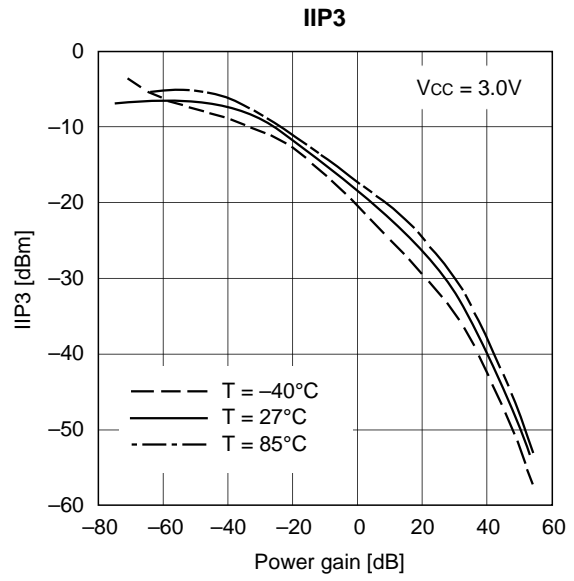
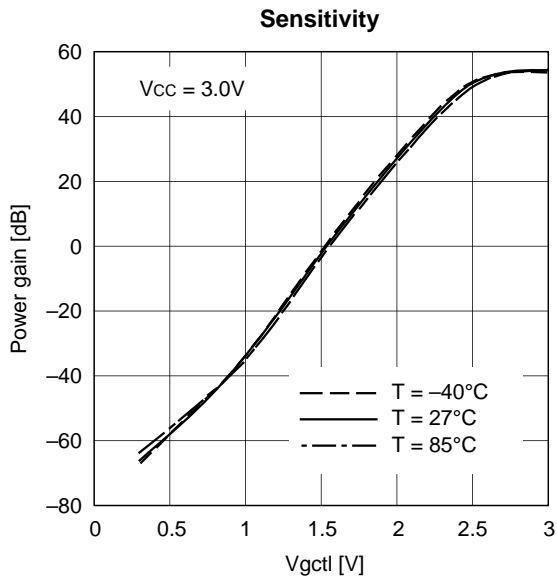
Single ended measurement

(V_{CC} = 3.0V, T_a = 27°C)

Item	Symbol	Conditions	Typ.	Unit
Input resistance	R _{in}	f = 210.38MHz, V _{gctl} = 1.5V	2.7	kΩ
Input capacitance	C _{in}		1.4	pF
Output resistance	R _{out}		5.9	kΩ
Output capacitance	C _{out}		0.85	pF

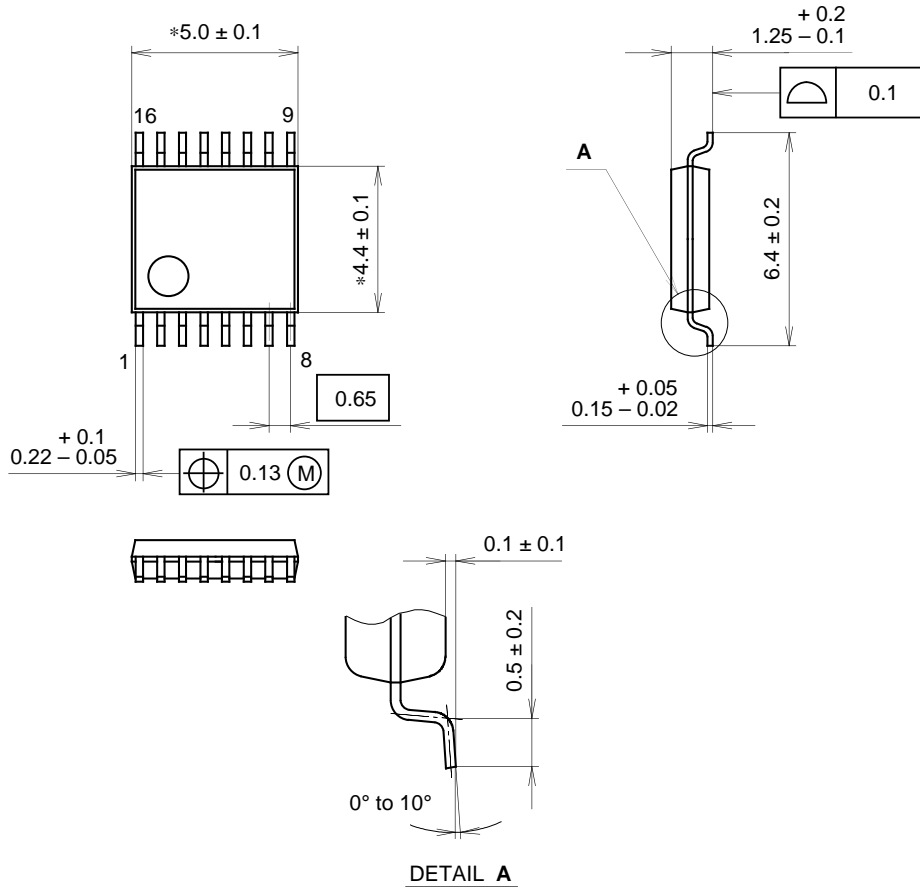
Notes on Operation

- 1) This IC is a wideband amplifier with wide gain control range. The decoupling capacitors between GND Pin and V_{CC} Pin should be as close to the IC as possible.
- 2) The resistors connected to Pins 9 and 10 should be as close to the IC as possible.
- 3) This IC assumes the excellent characteristics when the differential input impedance between Pins 1 and 2, Pins 4 and 5 is 500Ω. Refer to the Measurement Circuit for the external element settings, etc.
- 4) Pay attention to handling this IC because its electrostatic discharge strength is weak.



Package Outline Unit: mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
 This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).