

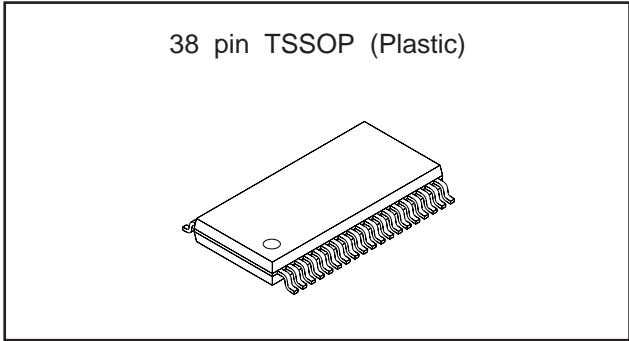
6/4-channel Read/Write Amplifier for GMR-Ind Head Hard Disk Drive

Description

The CXA3238TN/CXA3239TN is a Read/Write amplifier for GMR-Ind (Giant Magneto Resistive-Inductive) heads used in hard disk drives, and is capable of supporting up to six channels.

Features

- +5 V and -3 V power supply.
- Current bias voltage sense type.
- Drives up to six heads (CXA3238TN)
- Drives up to four heads (CXA3239TN)
- Low power 180 mW at Read
- Differential read amplifier gain ; $\times 140/190$
($R_{MR}=50 \Omega$)
- Input noise of $0.77 \text{ nV} / \sqrt{\text{Hz}}$ (typ.),
 $R_{MR}=50 \Omega, I_B=6.0 \text{ mA}$.
- Recovery time write to read ; 300 nsec. (typ.)
- Write data is triggered by differential P-ECL signal.
- Servo bank write. (All channels)
- Write unsafe detection circuit.
- Serial port ...
 - Head selection
 - MR bias
 - Write current



Absolute Maximum Ratings ($T_a=25 \text{ }^\circ\text{C}$)

• Supply voltage	V_{CC}	-0.3 to +6	V
• Supply voltage	V_{EE}	-4.5 to +0.3	V
• Digital input voltage	V_{di}	-0.3 to $V_{CC}+0.3$	V
• Operating temperature	T_{opr}	-20 to +70	$^\circ\text{C}$
• Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
• Allowable power dissipation			
	TSSOP38	P_D	1000 mW

Operating Conditions

• Supply voltage	V_{CC}	+4.4 to +5.5	V
	V_{EE}	-4.0 to -2.6	V
• MR bias voltage	V_{MR}	-300 to +300	mV
• Bias current	I_B	3 to 8	mA
• Write current	I_W	15 to 45	mA

Applications

Hard disk drives with GMR-Ind heads.

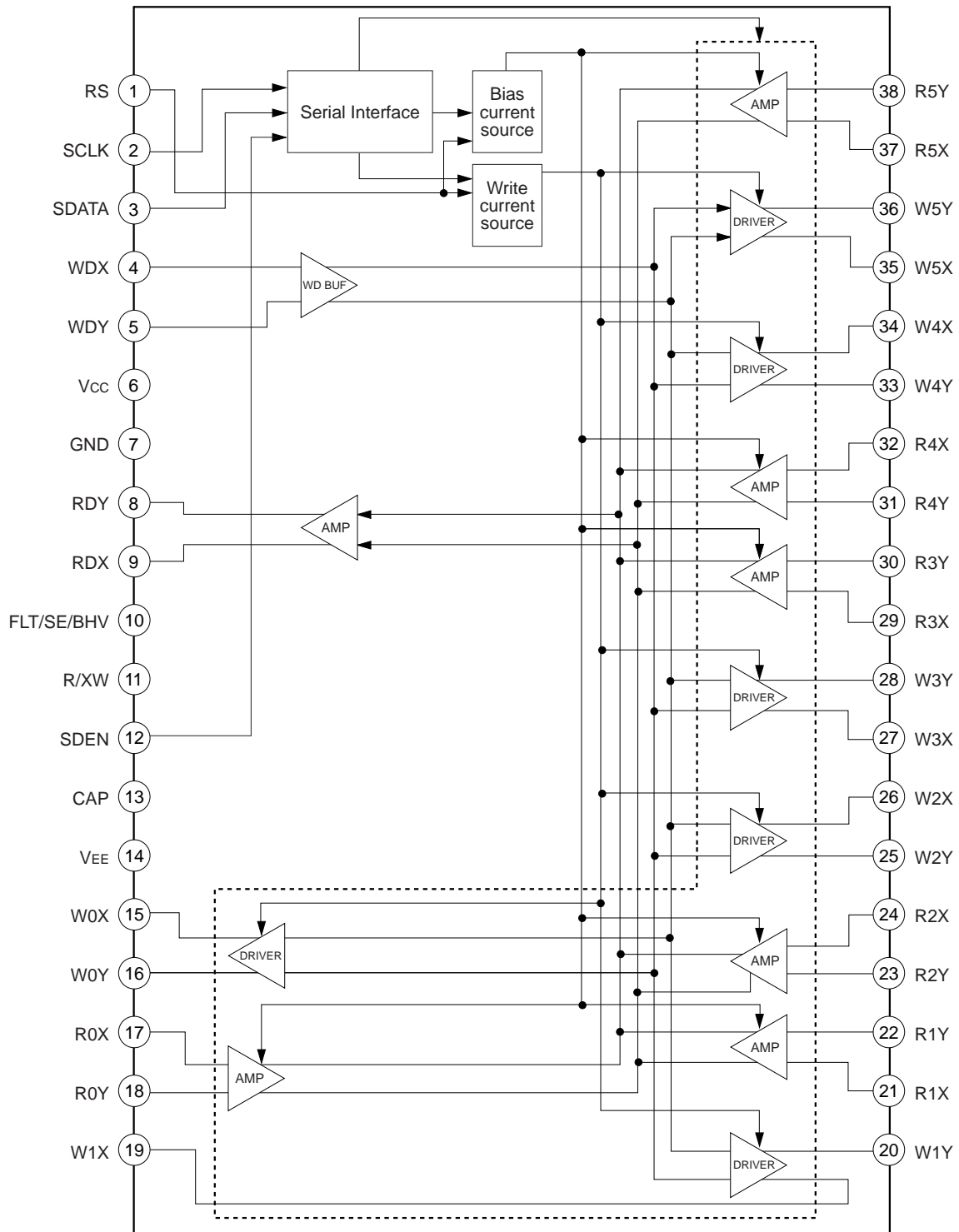
Structure

Bipolar silicon monolithic IC

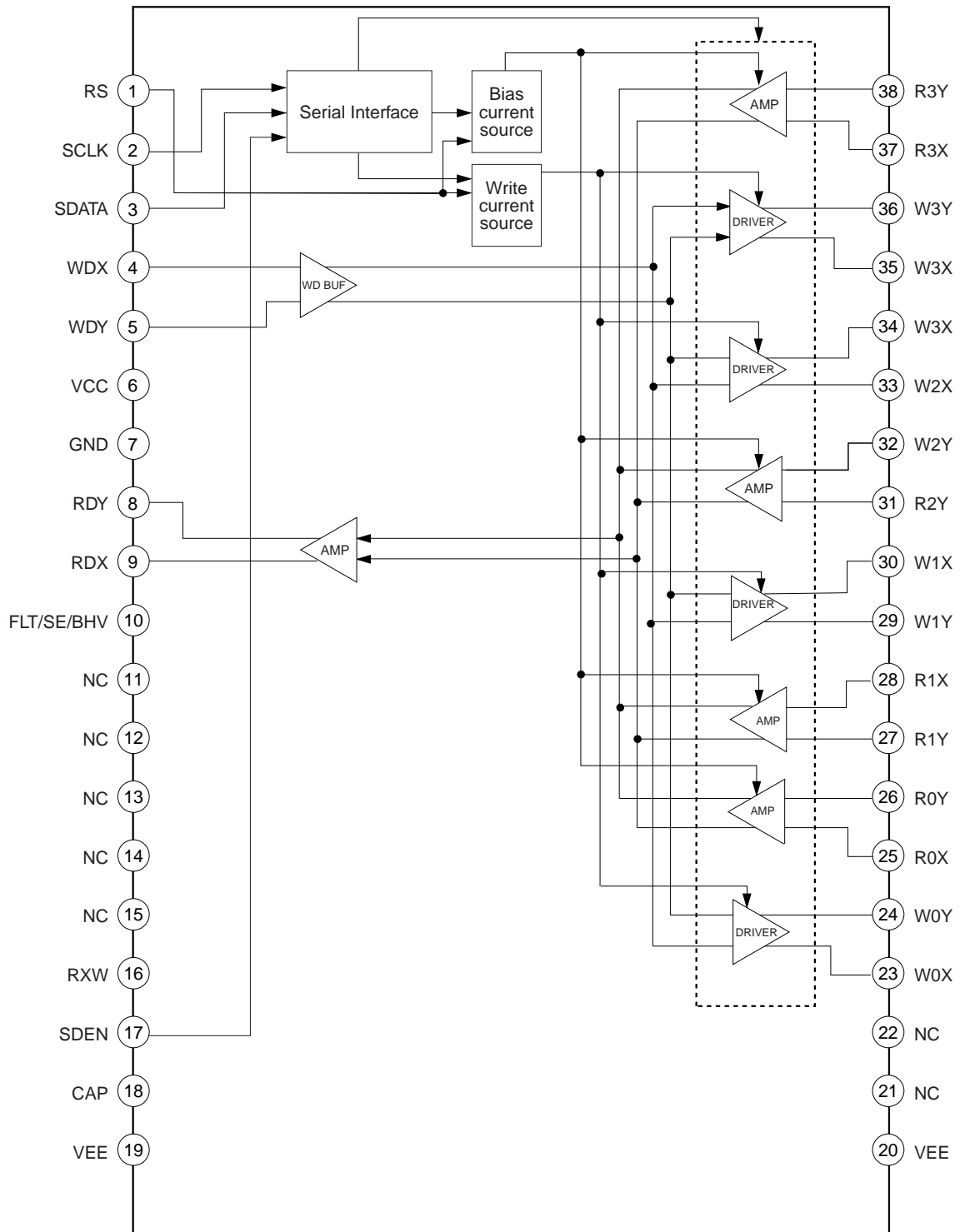
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Block Diagram and Pin Configuration

CXA3238TN



CXA3239TN



Pin Description CXA3238TN

Pin No.	Symbol	Equivalent circuit	Description
1	RS		Bias current setting register is connected between this pin and GND.
2 3 12	SCLK SDATA SDEN		Serial control signal input.
4 5	WDX WDY		Differential P-ECL write data input.
6	Vcc		5 V power supply.
7	GND		Ground
9 8	RDX RDY		Read amplifier output with coupling capacitors. High impedance in the write mode.

Pin No.	Symbol	Equivalent circuit	Description
10	FLT/SE/BHV		Head unsafe detection output. Servo Bank Write Enable input. Buffered Head Voltage output.
11	R/XW		Read / Write control signal input. Read when high, Write when low.
13	CAP		Connect an external capacitor of Read amplifier between this pin and VEE.
14	V _{EE}		-3 V power supply.
15 16 19 20 26 25 27 28 34 33 35 36	W0X W0Y W1X W1Y W2X W2Y W3X W3Y W4X W4Y W5X W5Y		Inductive heads for Write. Six channels are provided.

Pin No.	Symbol	Equivalent circuit	Description
17 18 21 22 24 23 29 30 32 31 37 38	R0X R0Y R1X R1Y R2X R2Y R3X R3Y R4X R4Y R5X R5Y	<p>The diagram shows an equivalent circuit for six channels. It consists of two horizontal lines representing power rails: Vcc at the top and VEE at the bottom. Six diodes are connected between these rails. The cathodes of all diodes are connected to the Vcc rail. The anodes are connected to the VEE rail and are grouped into three pairs: the top pair (pins 17, 21, 24), the middle pair (pins 29, 32, 37), and the bottom pair (pins 30, 31, 38). Each pair of pins is enclosed in a circle.</p>	MR heads for Read. Six channels are provided.

Pin Description CXA3239TN

Pin No.	Symbol	Equivalent circuit	Description
1	RS		Bias current setting register is connected between this pin and GND.
2 3 17	SCLK SDATA SDEN		Serial control signal input.
4 5	WDX WDY		Differential P-ECL write data input.
6	Vcc		5 V power supply.
7	GND		Ground
9 8	RDX RDY		Read amplifier output with coupling capacitors. High impedance in the write mode.

Pin No.	Symbol	Equivalent circuit	Description
10	FLT/SE/BHV		<p>Head unsafe detection output. Servo Bank Write Enable input. Buffered Head Voltage output.</p>
11 12 13 14 15 21 22	NC		Non Connection
16	R/XW		<p>Read / Write control signal input. Read when high, Write when low.</p>
18	CAP		<p>Connect an external capacitor of Read amplifier between this pin and VEE.</p>

Pin No.	Symbol	Equivalent circuit	Description
23 24 29 30 33 34 35 36	W0X W0Y W1Y W1X W2Y W2X W3X W3Y		Inductive heads for Write. Six channels are provided.
25 26 27 28 31 32 37 38			MR heads for Read. Six channels are provided.

Electrical Characteristics

(Unless otherwise specified; $V_{CC}=5\text{ V}$, $V_{EE}=-3\text{ V}$, $T_a=25\text{ }^\circ\text{C}$, $CAP=0.1\text{ }\mu\text{F}$, $R_S=7.5\text{ k}\Omega$)

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Power Dissipation $I_W=31\text{ mA}$, $I_B=6.0\text{ mA}$							
1-1	V_{CC} power supply current	I_{SP1}	SLEEP mode		2.1	2.8	mA
1-2		I_{ID1}	IDLE mode		22	29	mA
1-3		I_{RE1}	Read mode		36	47	mA
1-4		I_{WR1}	Write mode		80	100	mA
1-6	V_{EE} power supply current	I_{ID2}	IDLE mode		10	13	mA
1-7		I_{RE2}	Read mode		10	13	mA
1-8		I_{WR2}	Write mode		10	13	mA
1-9	Bank write mode	I_{CCBW}	$I_{CCBW}=17+17\times N+I_W\times N$, $I_W=31\text{ mA}$		300		mA
Digital Inputs							
2-1	TTL input low input voltage	V_{IL}	TTL input; R/XW Pull-up register : 100 k Ω	0		0.8	V
2-2	TTL input high input voltage	V_{IH}		2.0		$V_{CC}+0.3$	V
2-3	TTL input input current	I_{TTL}	High voltage : 5 V Low voltage : 0 V	-100		100	μA
2-4	Serial interface input low input voltage	V_{SIL}	Serial input; SDATA, SCLK, SDEN			1	V
2-5	Serial interface input high input voltage	V_{SIH}		4			V
2-6	Serial interface input input current	I_{ST}	High voltage : 5 V, Low voltage : 0 V Pull-down register : 14 k Ω	-1000		1000	μA
3-1	P ECL input Voltage range	V_{WDV}	Write data input	V_{CC} -2.5		$V_{CC}+0.3$	V
3-2	P ECL input Input amplitude	V_{WDA}		0.3		1.5	V
3-3	P ECL input current	I_{WD}	Input voltage : 4 V	-20		20	μA
4-1	Bank Write Enable voltage	V_{SEH}		$V_{CC}+1.2$		$V_{CC}+1.4$	V
4-2	Bank Write Enable current	I_{SEH}		6		14	mA

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
5-1	FLT output low voltage	V _{FLTL}	External resistance=2.4 k Ω			0.8	V
5-2	FLT output high voltage	V _{FLTH}	External resistance=2.4 k Ω	4.5			V
6	BHV accuracy	E _{BHV}	$V_{BHV}=V_{CC}-4\times I_B\times(R_{MR}+5.5\ \Omega)$ $I_B="1,1,1"$ $R_{MR}=50\ \Omega$	-8		8	%
Read Characteristics $R_{MR}=50\ \Omega$, $I_B=6.0\ \text{mA}$							
R1	Low Gain	A _{VL}	[GAIN]=0 $R_{MR}=50\ \Omega$, $I_B=6.0\ \text{mA}$	115	140	165	V/V
R2	High Gain	A _{VH}	[GAIN]=1 $R_{MR}=50\ \Omega$, $I_B=6.0\ \text{mA}$	155	190	225	V/V
R3	Low frequency cut-off (-3 dB)	F _{CL}			350	550	kHz
R4	High frequency cut-off (-3 dB)	F _{CH}		140	200		MHz
R5	Input reflected noise	E _{NI}	Exclusive of Head noise $R_{MR}=50\ \Omega$, $I_B=6.0\ \text{mA}$		0.77	0.95	nV/ $\sqrt{\text{Hz}}$
R6	MR bias current range 1	I _{BR1}		3		8	mA
R7	MR bias accuracy	E _{IB}		-7		+7	%
R8	MR bias resolution	R _{IB}	3 bit DAC		0.714		mA
R9-1	V _{CC} power supply rejection ratio	PSRR1	Ripple voltage : 100 mVp-p 100 kHz to 50 MHz	38			dB
R9-2	V _{EE} power supply rejection ratio	PSRR2	Ripple voltage : 100 mVp-p 100 kHz to 10 MHz	45			dB
R10-1	Common mode rejection ratio 1	CMRR1	Ripple voltage : 100 mVp-p 100 kHz to 50 MHz	37			dB
R10-2	Common mode rejection ratio 2	CMRR2	Ripple voltage : 100 mVp-p 51 MHz to 80 MHz	27			dB
R11	Control line input noise rejection	CLRR	Ripple voltage : 100 mVp-p 4 MHz to 80 MHz	40			dB
R12	RDX/RDY offset difference magnitude	V _{OFF1}	Write to Read			50	mV
R13	RDX/RDY output impedance	R _{Dro}	Differential, read mode	30		100	Ω

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Read Safety Characteristics							
P1	MR head open threshold	MROp	Head X - Head Y	600	750	900	mV
P2	MR head short threshold	MRsh	Head X - Head Y IB= '000' to '011'	15	50	90	mV
Write Characteristics							
W1	Write current range	IWR	DAC code= \times '0000' to \times '1111'	15		45	mA
W2	Write current accuracy	EIW		-7		+7	%
W3	Write current resolution	RIW	4 bit DAC		2		mA
W4	Leakage current	ILEAK	Unselected head			200	μ A
W6	Damping register	RD		320	420	520	Ω
W7	Write current propagation delay time	Tpd	LH=0, RH=0 Write DATA to 50 % of Write current			10	ns
W8	Write current rise/fall time	TR/TF	RH=15 Ω , LH=150 nH, Iw=31 mA		2.5		ns
W9	Erase current accuracy	EIE	VCC=3.5 V DAC code= \times '0101'	-18	-9	0	%
Write Safety Characteristics							
U1	Write head open threshold	ROp	Detect open head		1.2	1.4	V
U2	Head voltage when short to GND	VG	Detect short to GND			0.1	V
U3	WD frequency too low	fWDL		0.5		1.8	MHz
U4	Write safety detect time	Tws	T1 : 2 transitions on WDX/WDY			300 +T1	ns
U5	Low Vcc threshold	VWthL	Fault detected	3.7	3.9	4.1	V
U6	Low Vcc threshold	VWthH	Fault removed	3.9	4.1	4.3	V
U7	Low Vcc threshold hysteresis	Vhys			200		mV

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Switching Characteristics $I_W=31\text{ mA}$, $I_B=6\text{ mA}$							
S1	Write to Read	T_{WR}	Signal on WDX/WDY 90 % RD signal or 10 % I_W		300	500	ns
S2	Read to Write	T_{RW}	90 % I^W		50	70	ns
S3	Idle to Read	T_{IR}	90 % RD signal			1.0	μs
S4-1	Sleep to Read(A3238)	T_{SR1}	90 % RD signal ,90 % $I_B^{(*1)}$ $I_B="0,1,1"$		600	1000	μs
S4-2	Sleep to Read(A3239)	T_{SR2}	90 % RD signal ,90 % $I_B^{(*1)}$ $I_B="0,1,1"$		600	2000	μs
Bank Write Characteristics $I_W=31\text{ mA}$, $I_B=6\text{ mA}$							
S5	Read to Bank Write	T_{RB}	90 % I_W			100	ns
S6	Bank Write to Read	T_{BR}	10 % I_W			100	ns
S7	Idle to Bank Write Idle to Write	T_{IW}	90 % I_W			300	us
Serial port timing							
B1	Set up time	T_{su} (sden)	SDEN to first SCLK	10			ns
B2	Hold time	T_h (sden)	Last SCLK to deassert SDEN	10			ns
B4	SCLK frequency	f (sclk)				30	MHz
B5	SCLK pulse width	T_w (sclk)		10			ns
B6	SCLK-SDATA set up time	T_{su} (d)		10			ns
B7	SCLK-SDATA hold time	T_h (d)		10			ns
B8	SDEN low time	T_{SL}		100			ns

(*1) TSR is proportional to I_B and external CAP value

Serial port characteristics

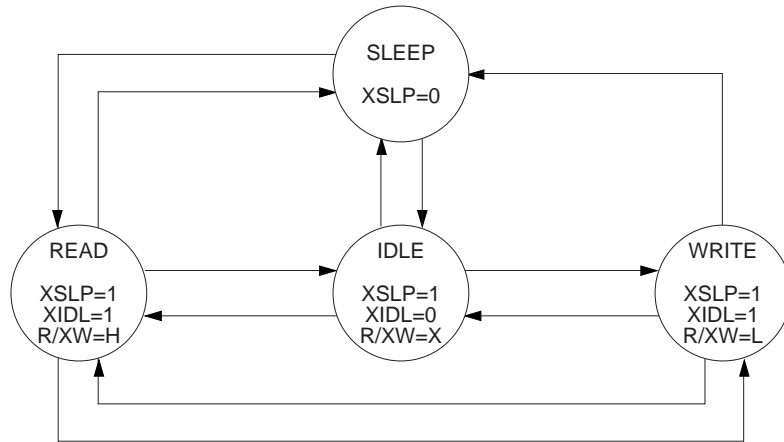
ADR1	ADR0	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0	0	XSLP	XIDL	N/A	HS2	HS1	HS0
0	1	GAIN	BHV	N/A	IB2	IB1	IB0
1	0	MROPN	MRSHT	IW3	IW2	IW1	IW0

*IB<2-0> bits are initialized by '0' at power on

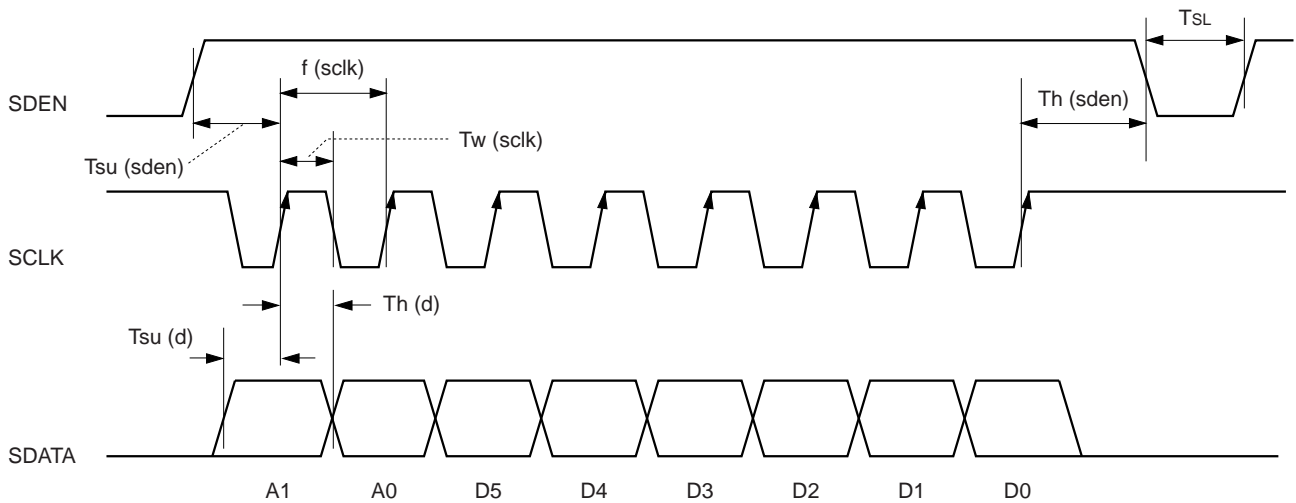
Code Description

Bit	Function
XSLP	"0" = Set the pre-amp into low power "sleep" mode
XIDL	"0" = Set preamplifier to idle mode
HS<2-0>	Head select bit
GAIN	Set the per-amp to high or low gain mode. "1" = Set preamplifier to high gain mode
BHV	Activate the BHV test point pin. "1" active.
IB<2-0>	MR bias current set
MROPN	"1" = Set MR head open detector active.
MRSHT	"1" = Set MR head short detector active.
IW<3-0>	Set write current

Mode Control



Serial Port Timing Detail



Serial Port Timing

After the SDEN goes high, the last eight bits are transferred into the register. The SCLK will shift the data presented at the SDATA into an internal shift register on the rising edge of each clock. As SCLK initial condition, both of Low and High signal is acceptable.

◆ Unsafe condition

1. Write fault condition

When write fault condition, FLT is a high level.

- Open write head leads. $f_{WD} < 15 \text{ MHz}$
- Write head leads shorted to ground.
- WD frequency too low.
- Power supplies out of tolerance.

2. Read fault condition

When read fault condition, FLT is a low level.

- Open and short MR head. (This function set by serial resister)

◆ Bank write control

1. Set to the Read mode.
2. Force FLT/SE positive (Put 820Ω between V_{CC} and SE terminal).
#This disables all Fault detection.
3. Set V_{CC} at 3.5 V (needed in only Erase mode)
4. Initiate the write operation by setting R/XW = "L".
5. Terminate the write operation by setting R/XW = "H".

- i) Usage less than 50 % write duty.
- ii) Low voltage detector is disabled in Bank Write mode and Erase mode.
- iii) Don't change the serial register data bits in following conditions :
 - *) $V_{CC}=3.5 \text{ V}$
 - ***) On entering Write data

◆ BHV condition

1. Usage within $V_{CC}=5 \text{ V} \pm 5 \%$
2. Turn off BHV bit on MROPN or MRSHT valid
3. V_{BHV} is defined by basis of V_{CC} . $V_{BHV} = V_{CC} - 4 \times I_B \times (R_{MR} + 5.5 \Omega)$

◆ Head select table

6ch

HS2	HS1	HS0	Head select, Normal operation
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	none
1	1	1	none

◆ Head select table

4ch

HS2	HS1	HS0	Head select, Normal operation
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	none
1	0	1	none
1	1	0	none
1	1	1	none

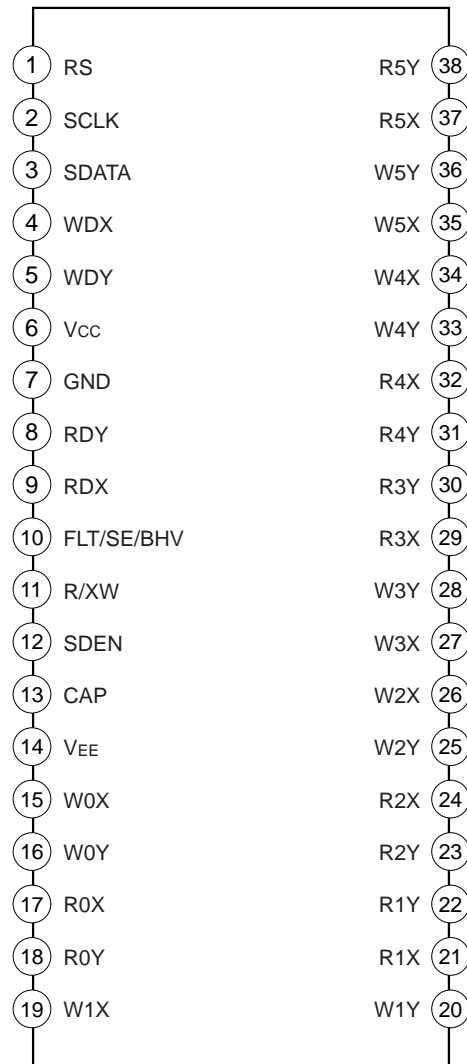
◆ MR Bias

IB2	IB1	IB0	I _B (mA)
0	0	0	3.0
0	0	1	3.714
0	1	0	4.429
0	1	1	5.143
1	0	0	5.857
1	0	1	6.571
1	1	0	7.286
1	1	1	8.0

◆ Write current

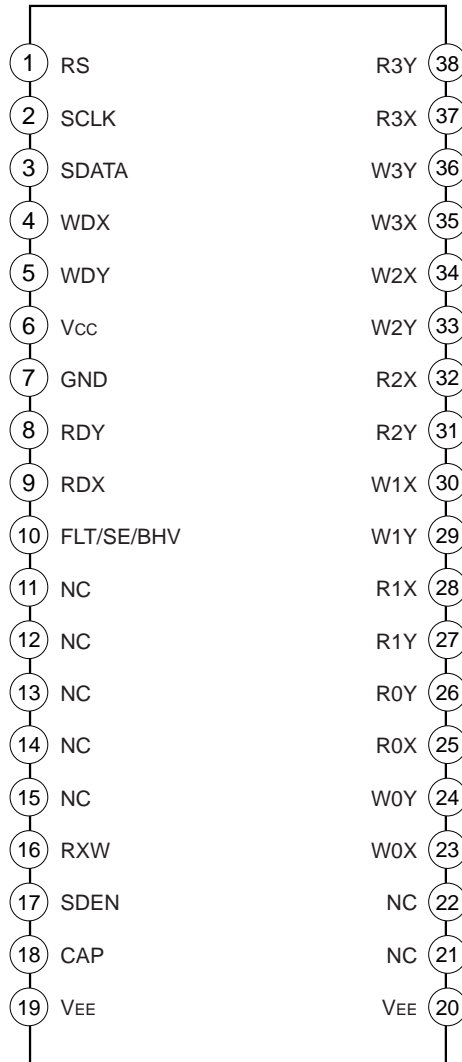
IW3	IW2	IW1	IW0	Write current (mA 0-P)
0	0	0	0	15
0	0	0	1	17
0	0	1	0	19
0	0	1	1	21
0	1	0	0	23
0	1	0	1	25
0	1	1	0	27
0	1	1	1	29
1	0	0	0	31
1	0	0	1	33
1	0	1	0	35
1	0	1	1	37
1	1	0	0	39
1	1	0	1	41
1	1	1	0	43
1	1	1	1	45

◆ 6ch CXA3238TN



TSSOP 38Pin 0.5 mm pitch
 Package dimension including leads 6.4 × 9.7 mm

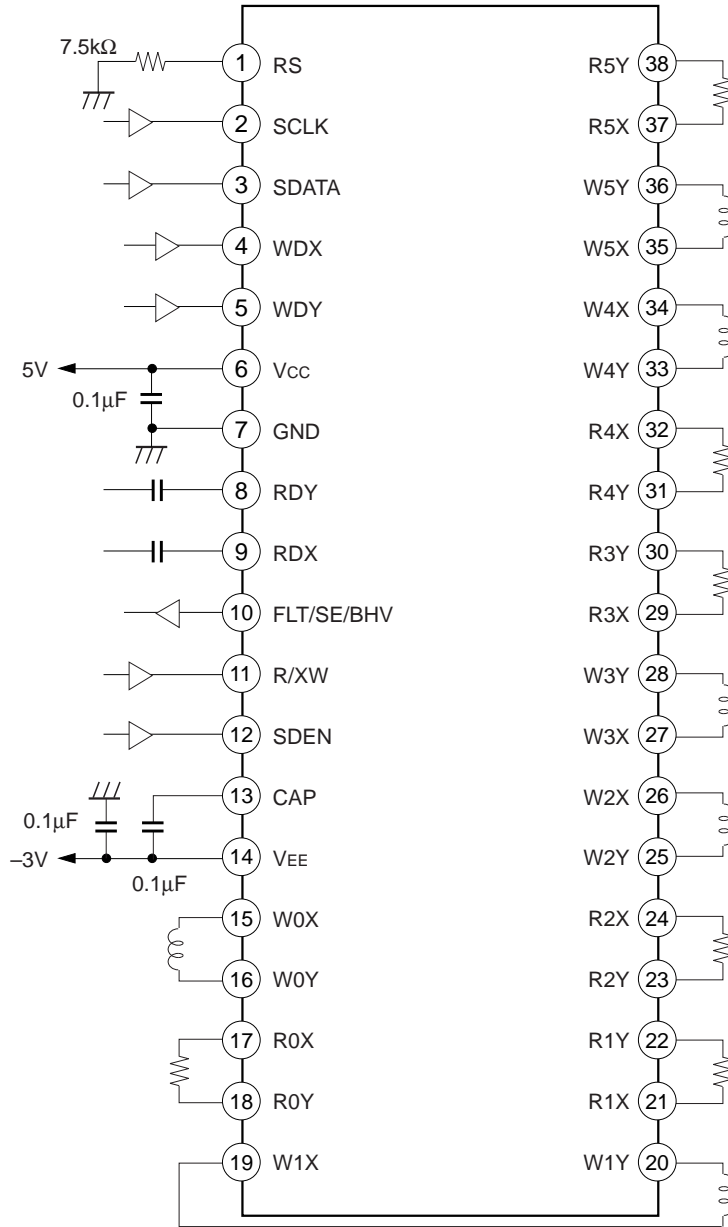
◆ 4ch CXA3239TN



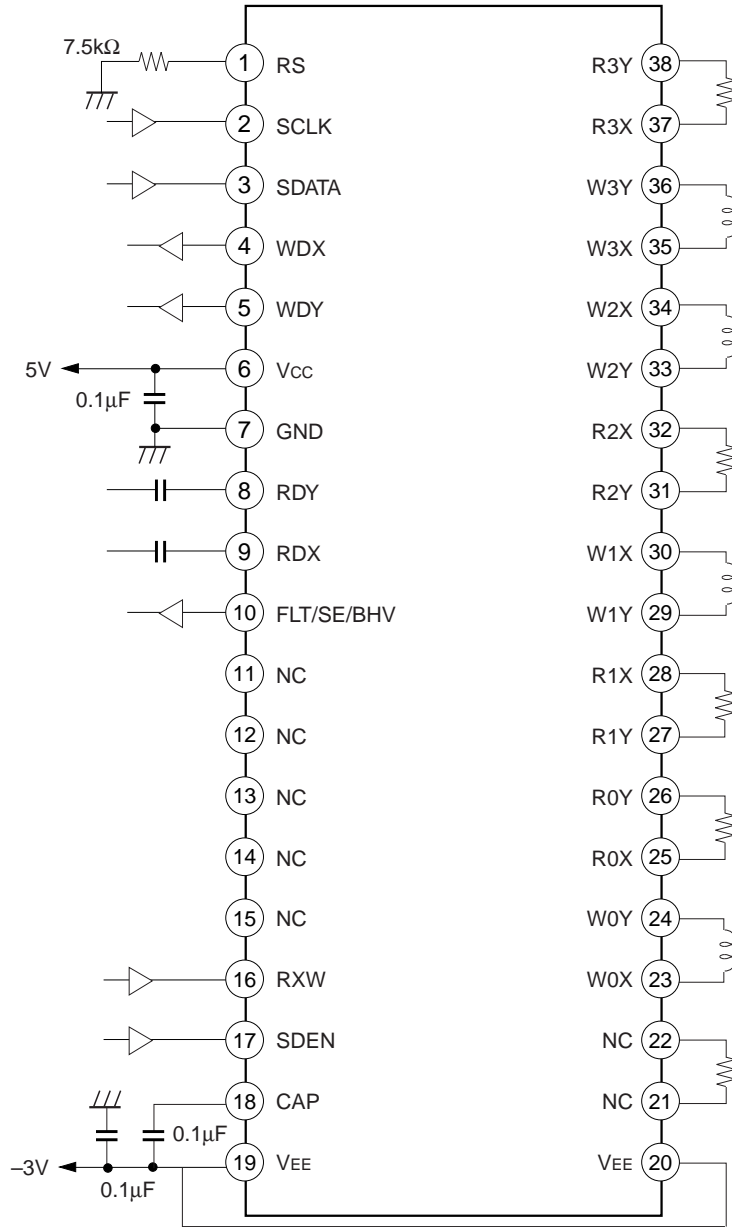
TSSOP 38Pin 0.5 mm pitch
 Package dimension including leads 6.4 × 9.7 mm

Application Circuit

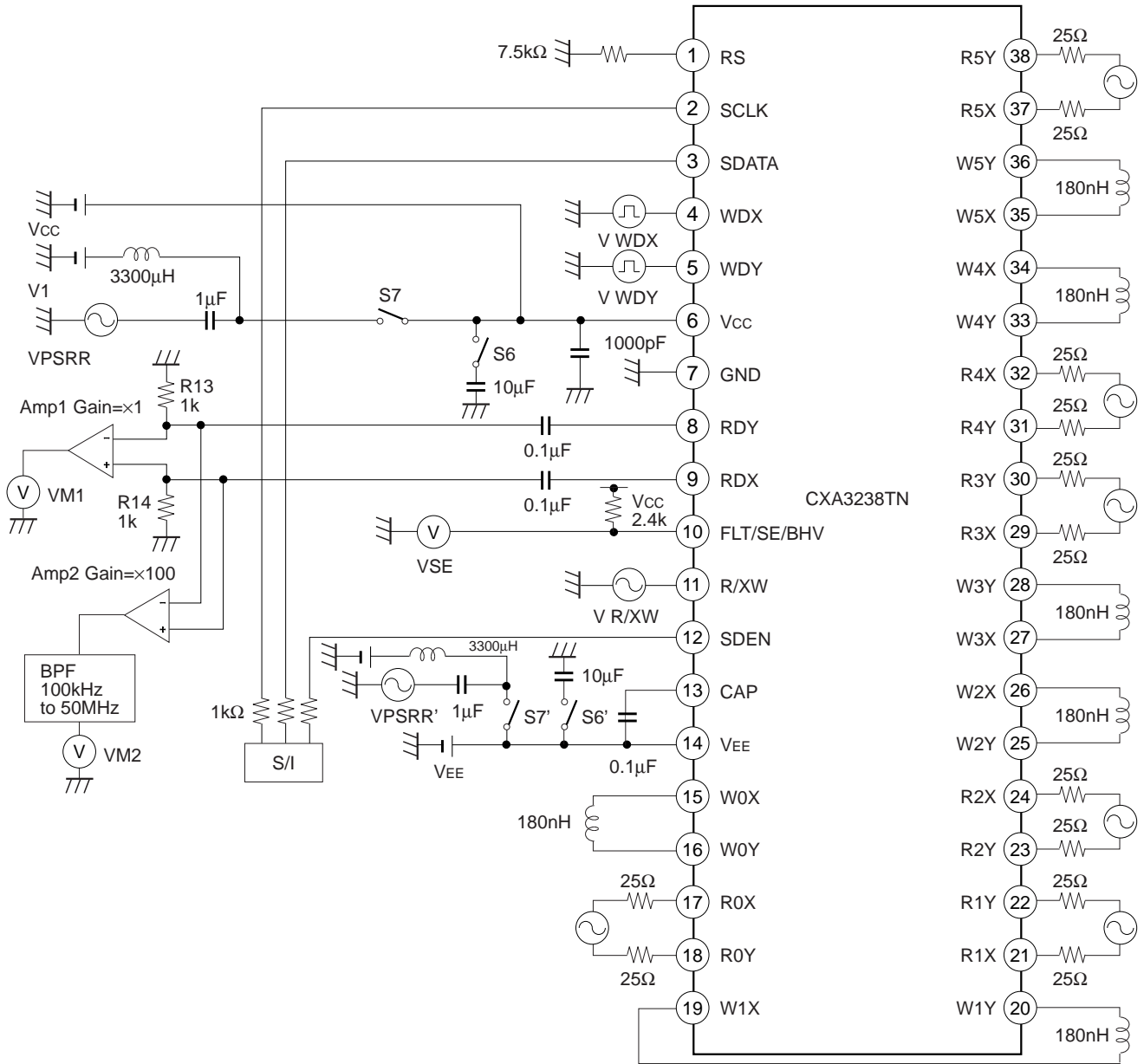
CXA3238TN

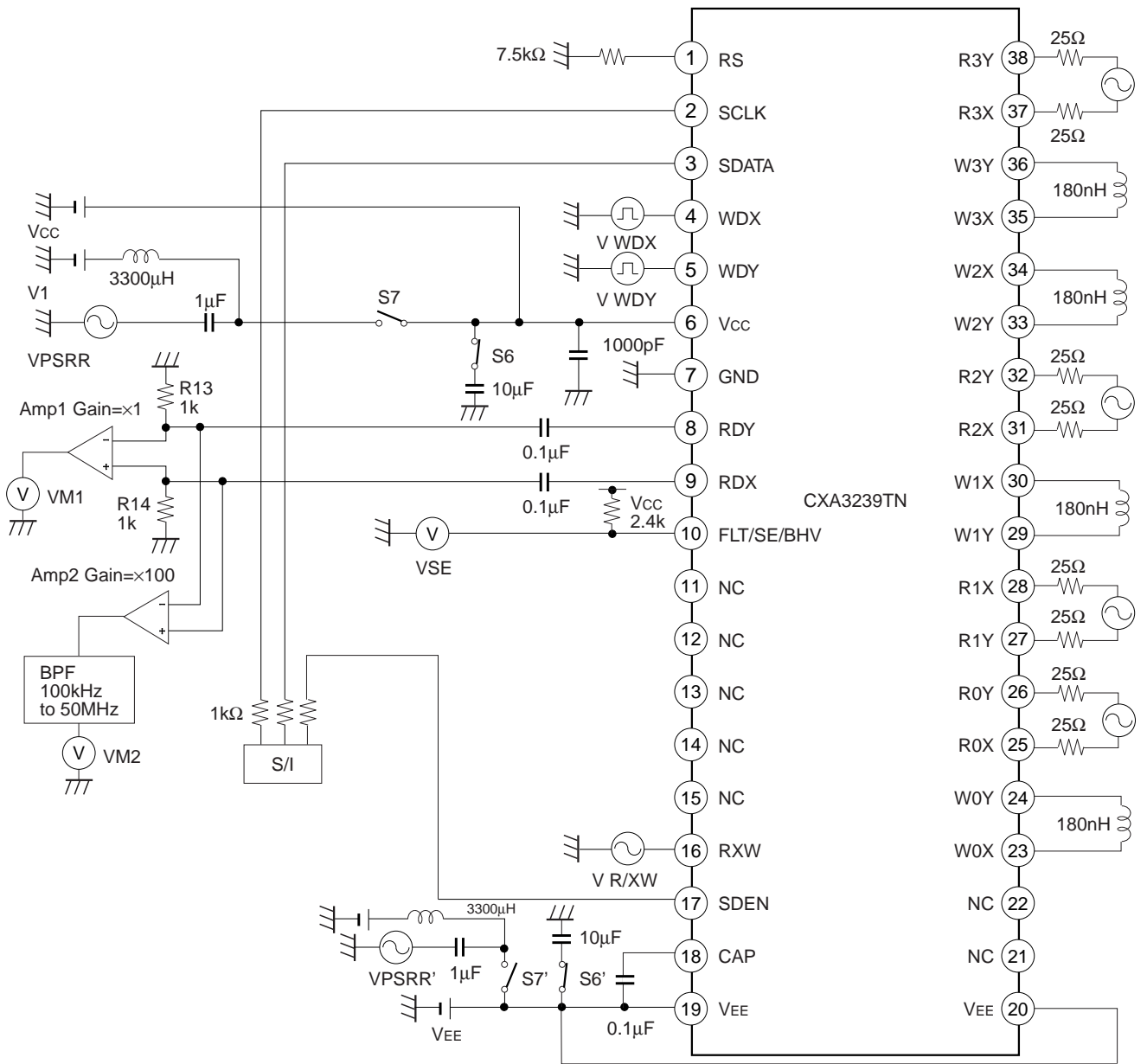


CXA3239TN

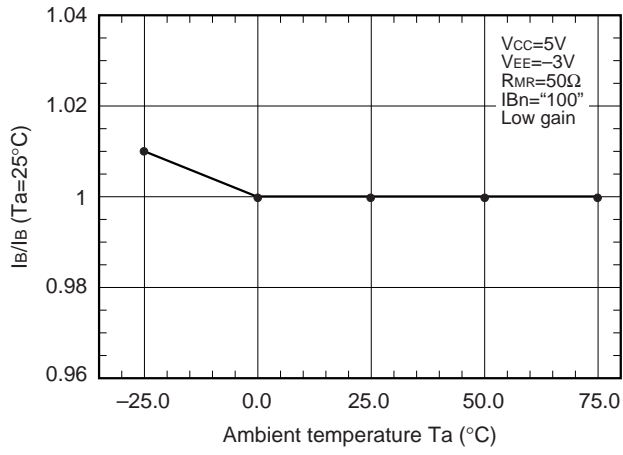


Measurement Spec.Circuit

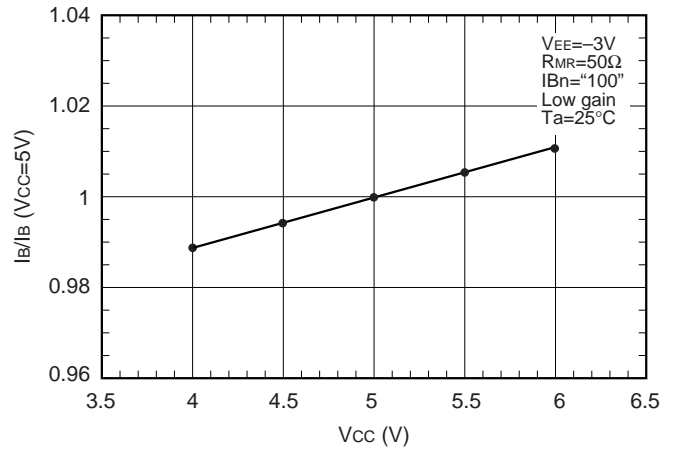




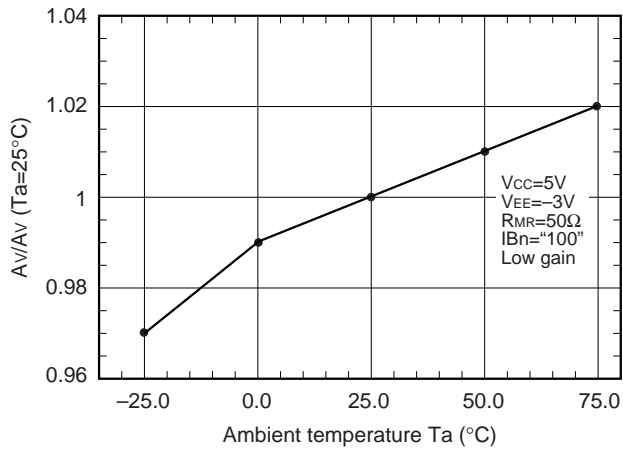
Normalized bias current vs Ambient temperature



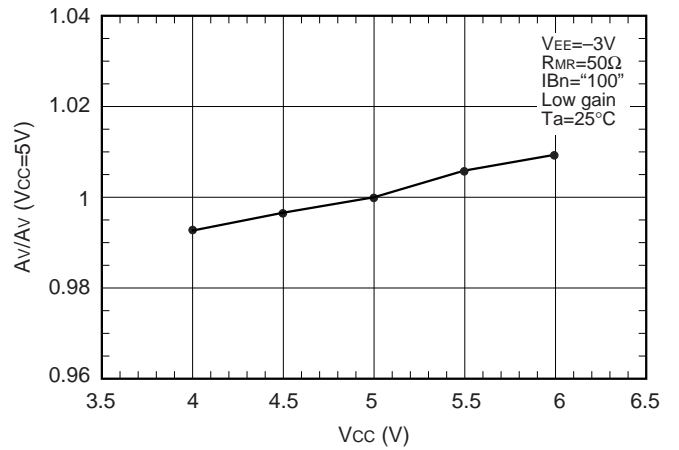
Normalized bias current vs Power supply voltage



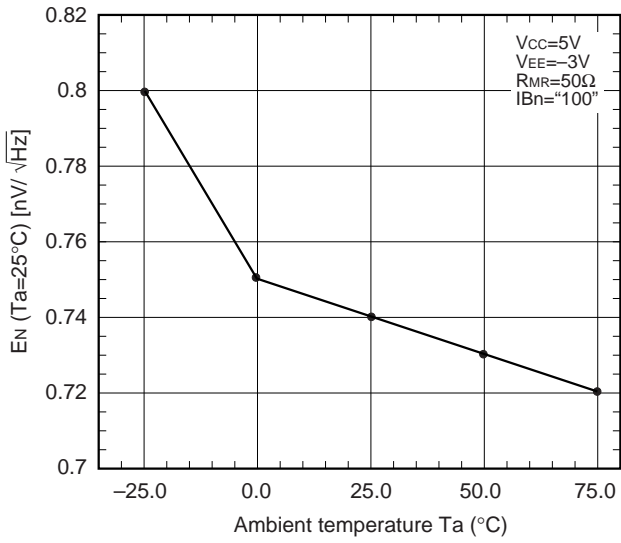
Normalized read amplifier voltage gain vs Ambient temperature



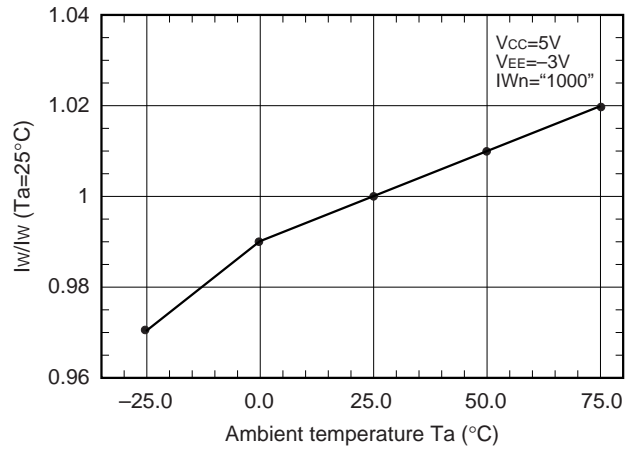
Normalized read amplifier voltage gain vs Power supply voltage



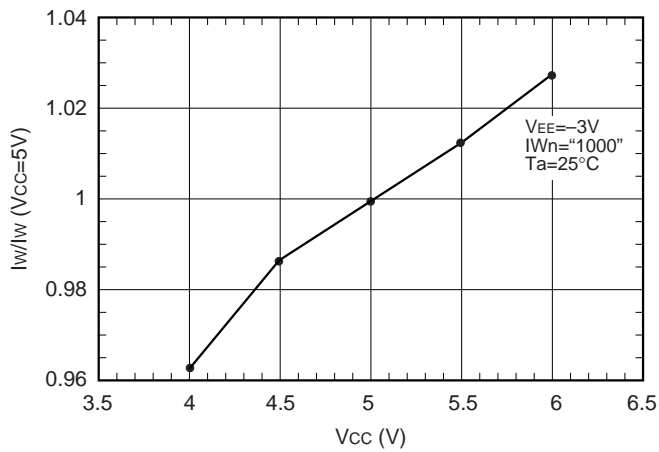
Input referred noise voltage vs Ambient temperature



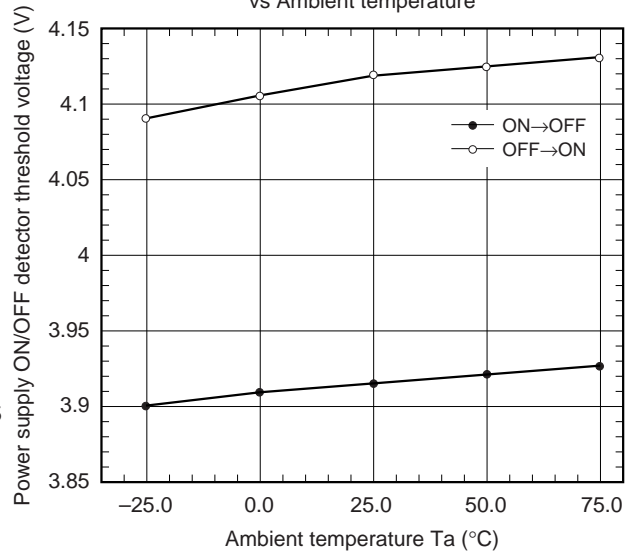
Normalized write current vs Ambient temperature



Normalized write current vs Power supply voltage

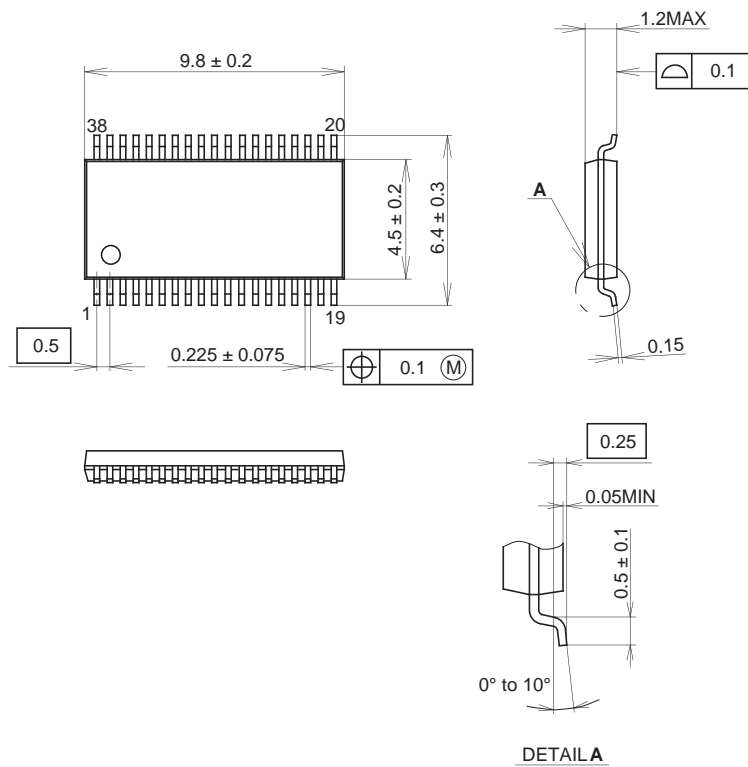


Power supply ON/OFF detector threshold voltage vs Ambient temperature



Package Outline Unit : mm

38PIN TSSOP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	TSSOP-38P-L121
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g