SONY

CXB1454R

VGA/SVGA/XGA 24bit Receiver

Description

CXB1454R is the 1 chip deserializer for VGA/SVGA/XGA 24bit color digital RGB, and meet to the Gigabit Video Interface specification.

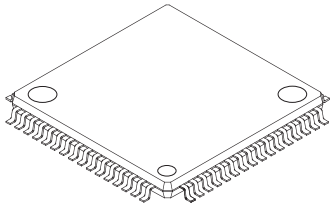
Features

- 1 chip receiver for serial transmission of 24-bit color VGA/SVGA/XGA picture
- On chip cable equalizer circuit to compensate the cable loss
- On chip PLL circuit for data and clock recovery
- On chip panel mode automatically selectable circuit
- TTL compatible I/O
- Support 1 pixel/shiftclock mode with 1 chip and 2 pixel/shiftclock mode with 2 chips
- +3.3V single power supply
- Low power consumption
- 64pin plastic LQFP package with body size 14mm × 14mm

Structure

Bipolar silicon monolithic IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	Vcc	4.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1710	mW

Recommended Operating Condition

• Supply voltage	Vcc	3.3 ± 0.16	V
• Operating temperature	Topr	0 to +60	°C

Block Digagram & Pin out

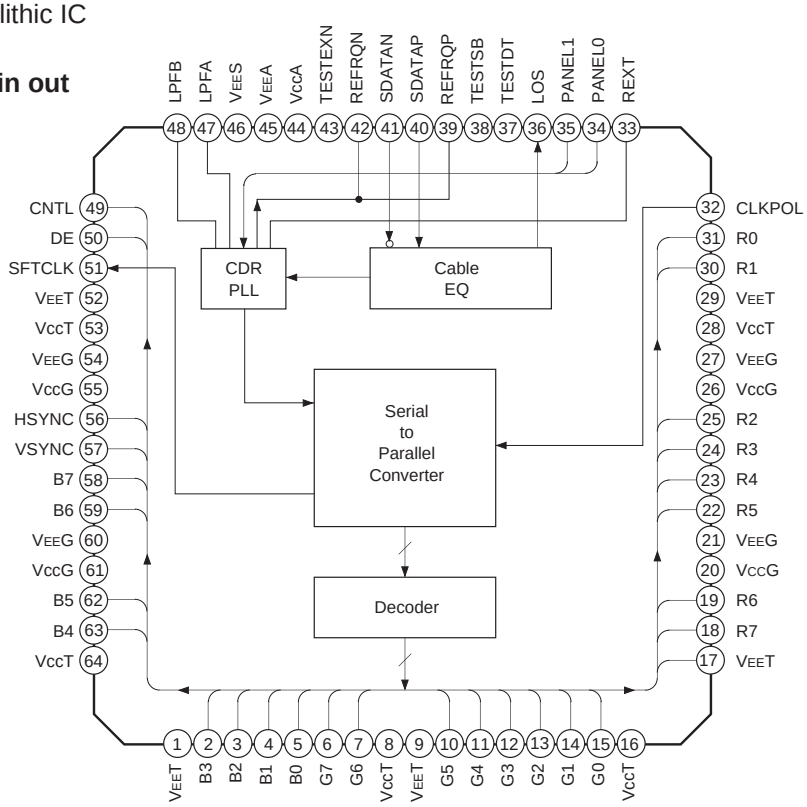


Fig. 1. Block Diagram & Pin out

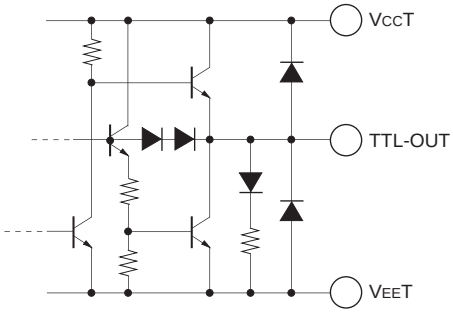
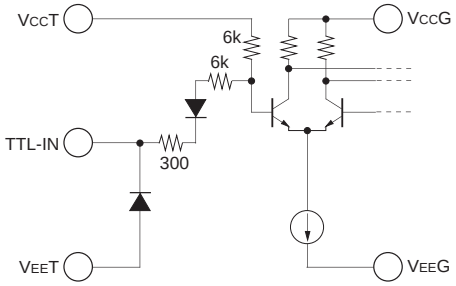
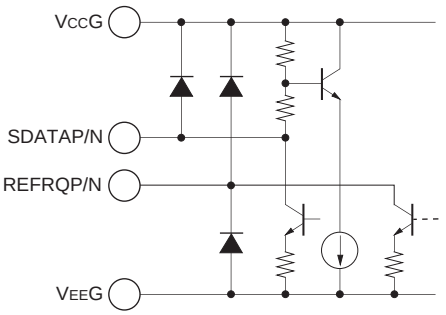
E98X24B03

Pin List

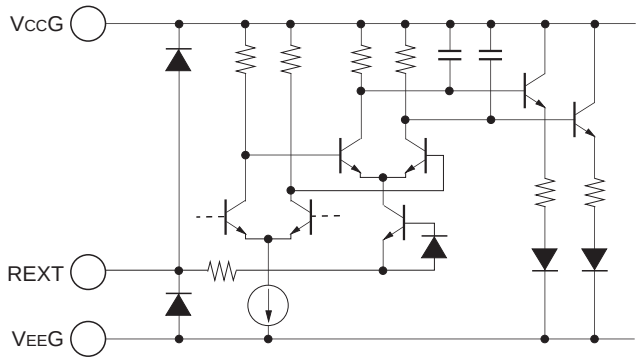
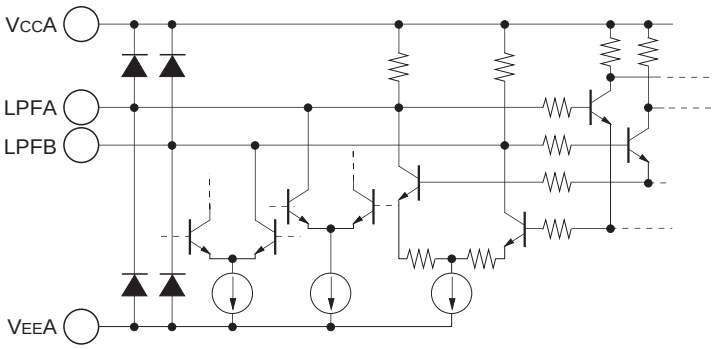
Tab. 1. Power/Ground

Pin Name	Pin Number	Descriptions
V_{CC}T	8, 16, 28, 53, 64	TTL power surpply, should be connected to 3.3V ± 5%
V_{EE}T	1, 9, 17, 29, 52	TTL ground, connected to 0V
V_{CC}G	20, 26, 55, 61	Logical core power surpply, connected to 3.3V ± 5%
V_{EE}G	21, 27, 54, 60	Logical core ground, connected to 0V
V_{CC}A	44	Analog power surpply, connected to 3.3V ± 5%
V_{EE}A	45	Analog ground, connected to 0V
V_{EE}S	46	Analog substrate, connected to 0V

Tab. 2. Digital Signals

Pin Name	Pin Number	Type	Descriptions	Equivalent circuit
SFTCLK	51	TTL out	Shift clock, for the data fetch at falling or rising edge	
RED (7 to 0) GRN (7 to 0) BLU (7 to 0)	18, 19, 22, 23, 24, 25, 30, 31, 6, 7, 10, 11, 12, 13, 14, 15, 58, 59, 62, 63, 2, 3, 4, 5	TTL out	Pixel data	
HSYNC	56	TTL out	Hsync data	
VSYNC	57	TTL out	Vsync data	
CNTL	49	TTL out	Control data	
DE	50	TTL out	Display enable data	
LOS	36	TTL out	Los of signal	
PANEL (1, 0)	35, 34	TTL in	Panel mode select switch	
CLKPOL	32	TTL in	Trigger edge select switch	
TESTEXN TESTDT TESTSB	43, 37, 38	TTL in	Reserved for TEST under fabrication	
SDATAP/N	40, 41	Rx	Serial input	
REFRQP/N	39, 42	Rx	Refclk request	

Tab. 3. Special

Pin Name	Pin Number	Descriptions	Equivalent circuit
REXT	33	External Resister	
LPFA/B	47, 48	External loop filter	

Electrical characteristics

Tab. 4. Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V_{CC}	–0.3		4	V	
TTL DC input voltage	V_I_T	–0.5		5.5	V	
TTL output current (High)	I_{OH}_T	–20		0	mA	
TTL output current (Low)	I_{OL}_T	0		20	mA	
Serial input pin voltage	Vsdin	–0.5		V_{CC} + 0.5	V	
REFRQ output pin voltage	V_{RQ}out	0.5		V_{CC} + 0.5	V	
Storage temperature	Tstg	–65		150	°C	

Tab. 5. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage (Include V_{CC}T5)	V_{CC}	3.135	3.3	3.465	V	
Operating temperature	Topr	0		60	°C	

Tab. 6. DC Characteristics (Under the recommended conditons. See Tab. 5)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input HIGH voltage (TTL)	V_{IH}_T	2		5.5	V	
Input LOW voltage (TTL)	V_{IL}_T	0		0.8	V	
Input HIGH current (TTL)	I_{IH}_T			20	µA	$V_{IN} = V_{CC}$
Input LOW current (TTL)	I_{IL}_T	–400			µA	$V_{IN} = 0$
Output HIGH voltage (TTL)	V_{OH}_T	2.25			V	I_{OH} = –0.2mA
Output LOW voltage (TTL)	V_{OL}_T			0.5	V	I_{OL} = 4mA
Output HIGH current (REFRQ)	I_{OH}_RQ	–0.1	0	+0.1	mA	See Fig. 3, 4 REXT = 1.3kΩ
Output LOW current (REFRQ)	I_{OL}_RQ	7.8		11	mA	
Input dynamic range (SDATA)	V_{IM}_SD	V_{CC} – 0.4		V_{CC} + 0.2	V	Common mode voltage
Input dynamic range (SDATA)	V_{ID}_SD	–0.5		+0.5	V	Differential voltage
Supply current	I_{CC}		325	440	mA	65MHz, All low pattern, Outputs open
			350	465	mA	65MHz, Worst case pattern See Fig. 8 Outputs open

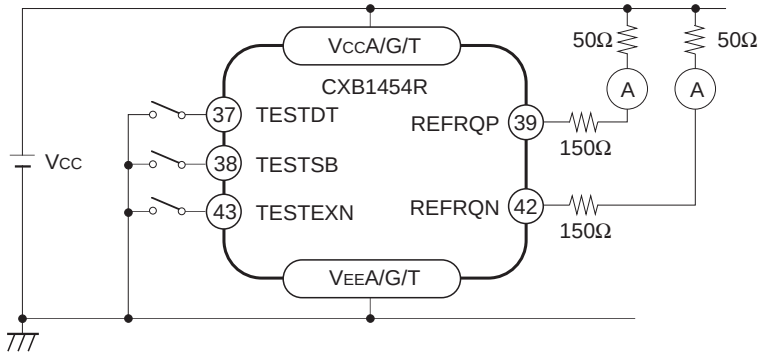


Fig. 2. I_{OH}_RQ and I_{OL}_RQ DC measurement

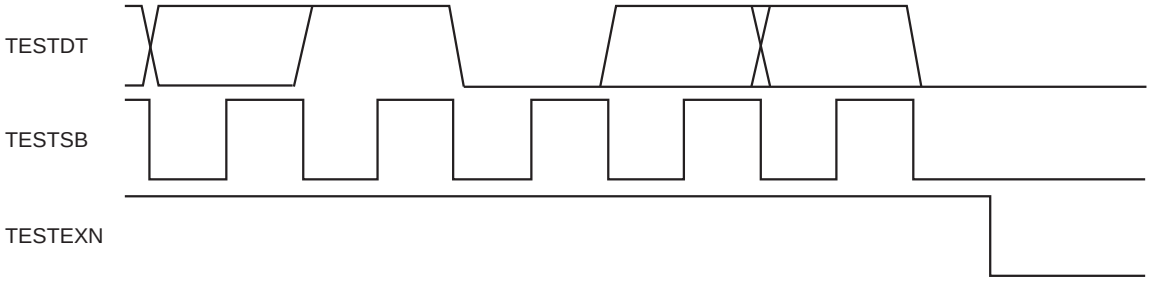


Fig. 3. I_{OH}_RQ and I_{OL}_RQ DC measurement setting

Electrical characteristics

Tab. 7. AC Characteristics (Under the recommended conditons. See Tab. 5)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Minimum SFTCLK frequency Maximum SFTCLK frequency	Fsftclk	 65.0		25.0	MHz MHz	
SFTCLK duty factor	Dsftclk	40		60	%	Vth = 1.4V, C_L = 10pF
Pixel/Sync/Cntl/DE setup to SFTCLK	Tsetup	16 10 5			ns ns ns	Vth = 1.4V, C_L = 10pF 25MHz 40MHz 65MHz
Pixel/Sync/Cntl/DE hold to SFTCLK	Thold	17 11 6			ns ns ns	Vth = 1.4V, C_L = 10pF 25MHz 40MHz 65MHz
SFTCLK rise time	Torc			3	ns	0.8 to 2.0V, C_L = 10pF
SFTCLK fall time	Tofc			2.5	ns	2.0 to 0.8V, C_L = 10pF
Pixel/Sync/Cntl/DE rise time	Tofd			4.5	ns	0.8 to 2.0V, C_L = 10pF
Pixel/Sync/Cntl/DE fall time	Tord			2	ns	2.0 to 0.8V, C_L = 10pF
CLOCK mode assert time	TAclk		0.9		µs	
CLOCK mode deassert time	TDclk		50		µs	
LOS signal assert time	TAlos		0.5		µs	
LOS signal deassert time	TDlos		0.1		µs	

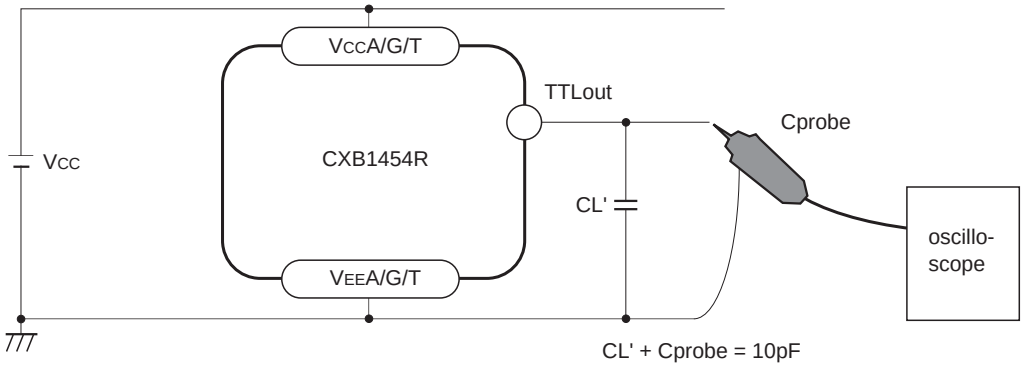


Fig. 4. Pixel/Sync/Cntl/DE waveform measurement

Timing Chart

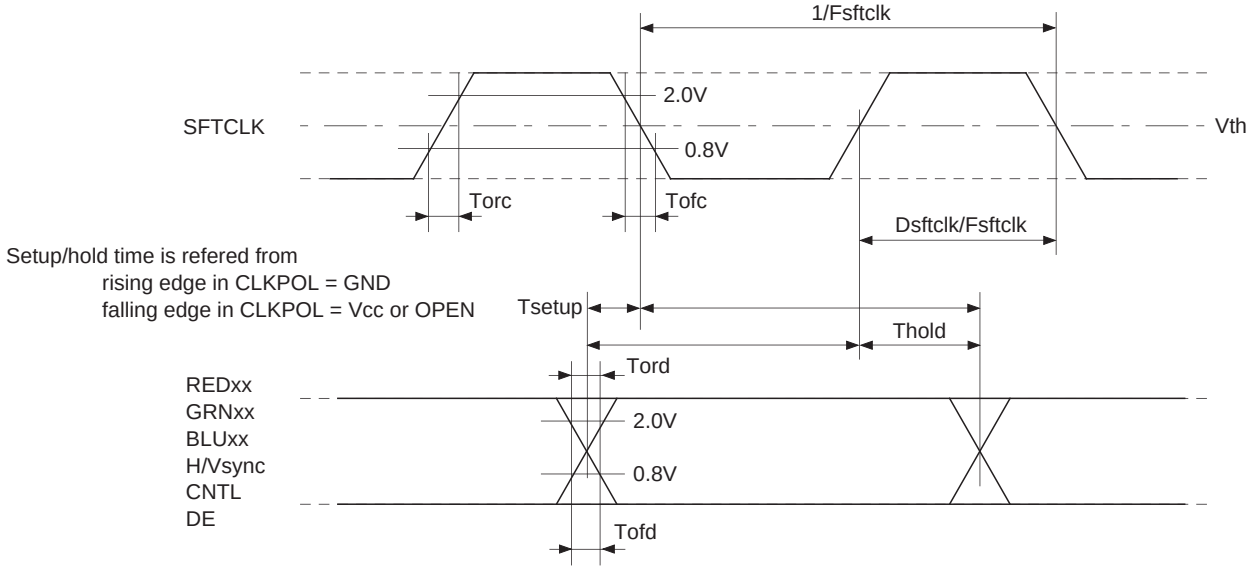


Fig. 5. TTL output timing

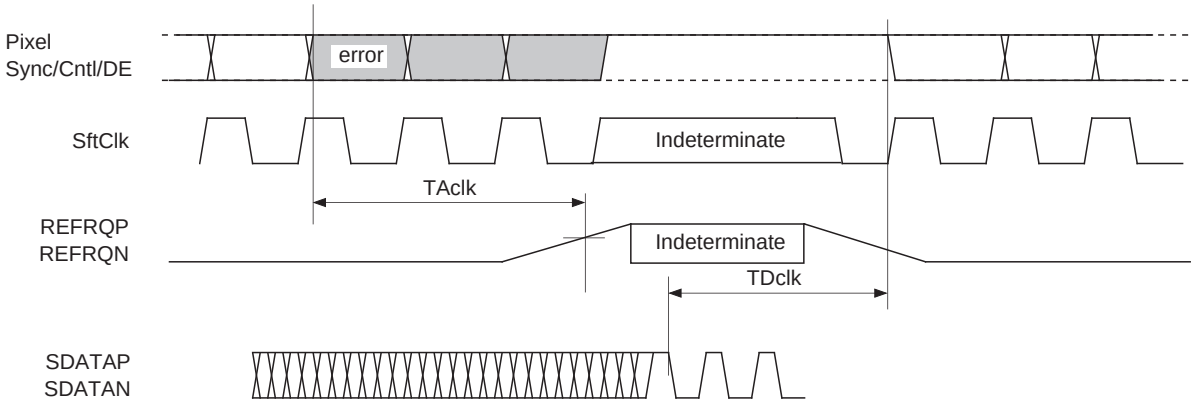


Fig. 6. Refclk request timing

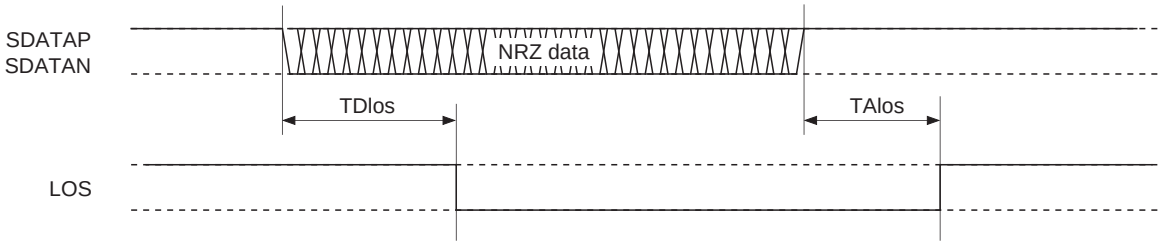


Fig. 7. Idle mode timing

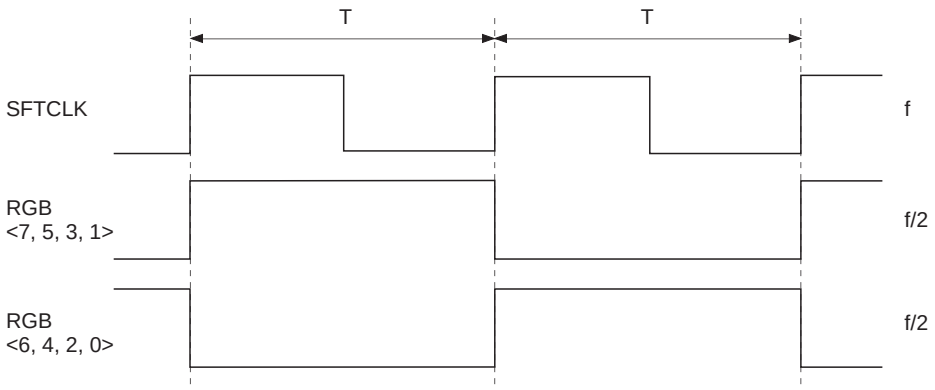


Fig. 8. Worst case test pattern

CLKPOL Pin Control

The CLKPOL pin is used to select the SFTCLK trigger edge. (See Table 8.)
The CLKPOL pin is open High TTL input.

Table 8. SFTCLK Polarity

CLKPOL	Receiver operation trigger
L	Rising edge
H	Falling edge

PANEL1 and 0 Pin Control

The PANEL1 and 0 pins are used to select the panel mode. (See Table 9.)
For the normal use, the all frequencies of SFTCLK (25MHz to 65MHz) can be covered by fixing both PANEL1 and 0 to High.
The PANEL1 and 0 pins are open High TTL inputs.

Table 9. Panel Mode

PANEL1	PANEL0	Supporting panel size	Shift clock	Serial rate
L	L	VGA (640 × 480)	25MHz	750Mbps
L	H	SVGA (800 × 600)	40MHz	1200Mbps
H	L	XGA (1024 × 768)	65MHz	1950Mbps
H	H	VGA to XGA	25MHz to 65MHz	750Mbps to 1950Mbps

Test Pin Control

The TESTEXN, TESTDT and TESTSB pins are for test only. Select normal mode. (See Table 10.)
The TESTEXN, TESTDT and TESTSB pins are open High, TTL inputs.

Table 10. Test Mode

TESTEXN	TESTDT	TESTSB	Operation mode
L	X	X	Test mode
H	H	H	Normal mode

LOS Pin Output

The LOS pin shows the absence of proper level of SDATA signal. The LOS pin is High when the connector is disconnected or the transmitter is idle.
The LOS pin is TTL output.

Applications

CXB1454R GVIF receiver is applied to the digital RGB signal transmission for

P/C with LCD monitor
Video on demand system
Monitoring system
Graphical controller
Projector
Digital TV monitor
Car navigation system

with GVIF transmitter, CXB1455R.

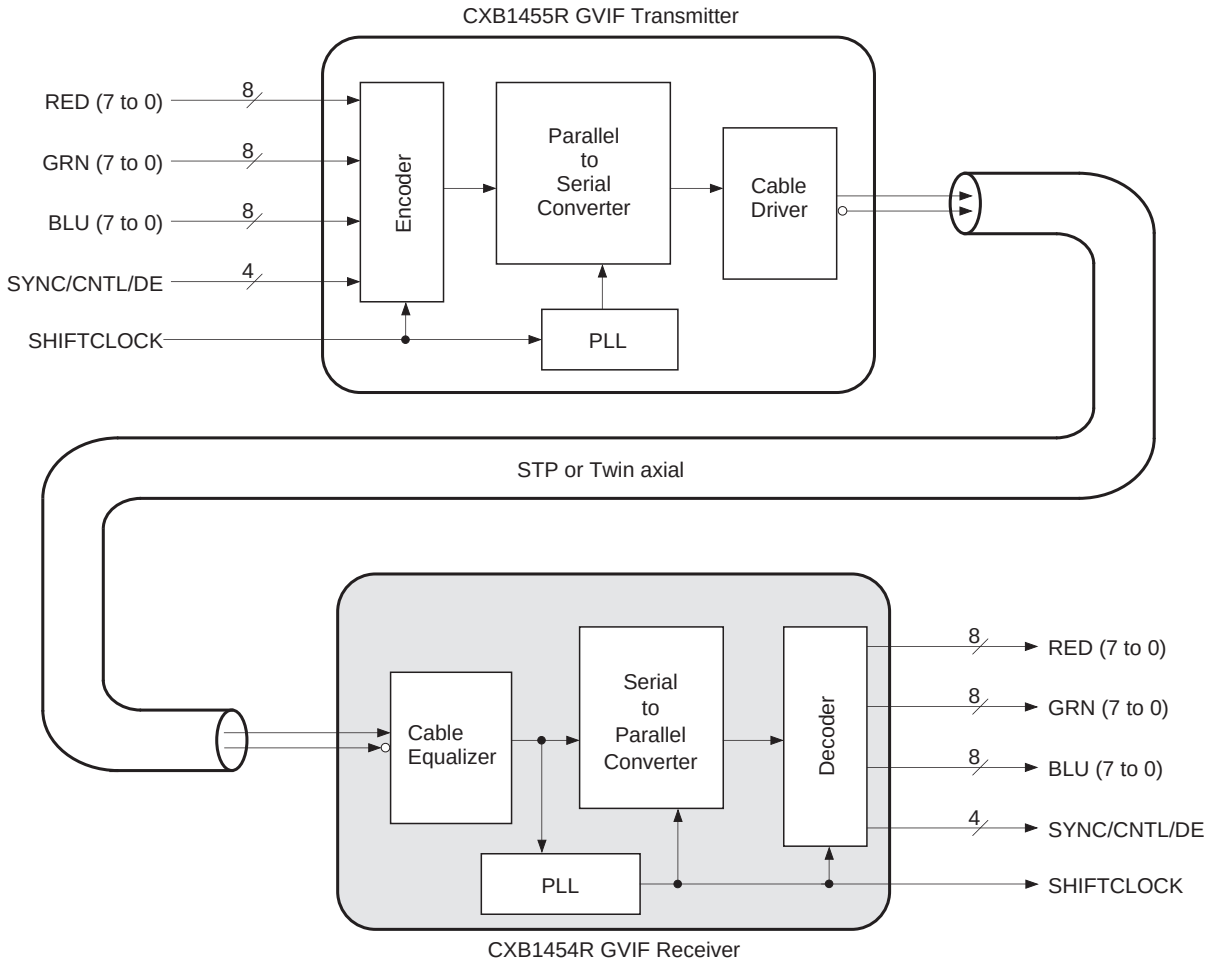
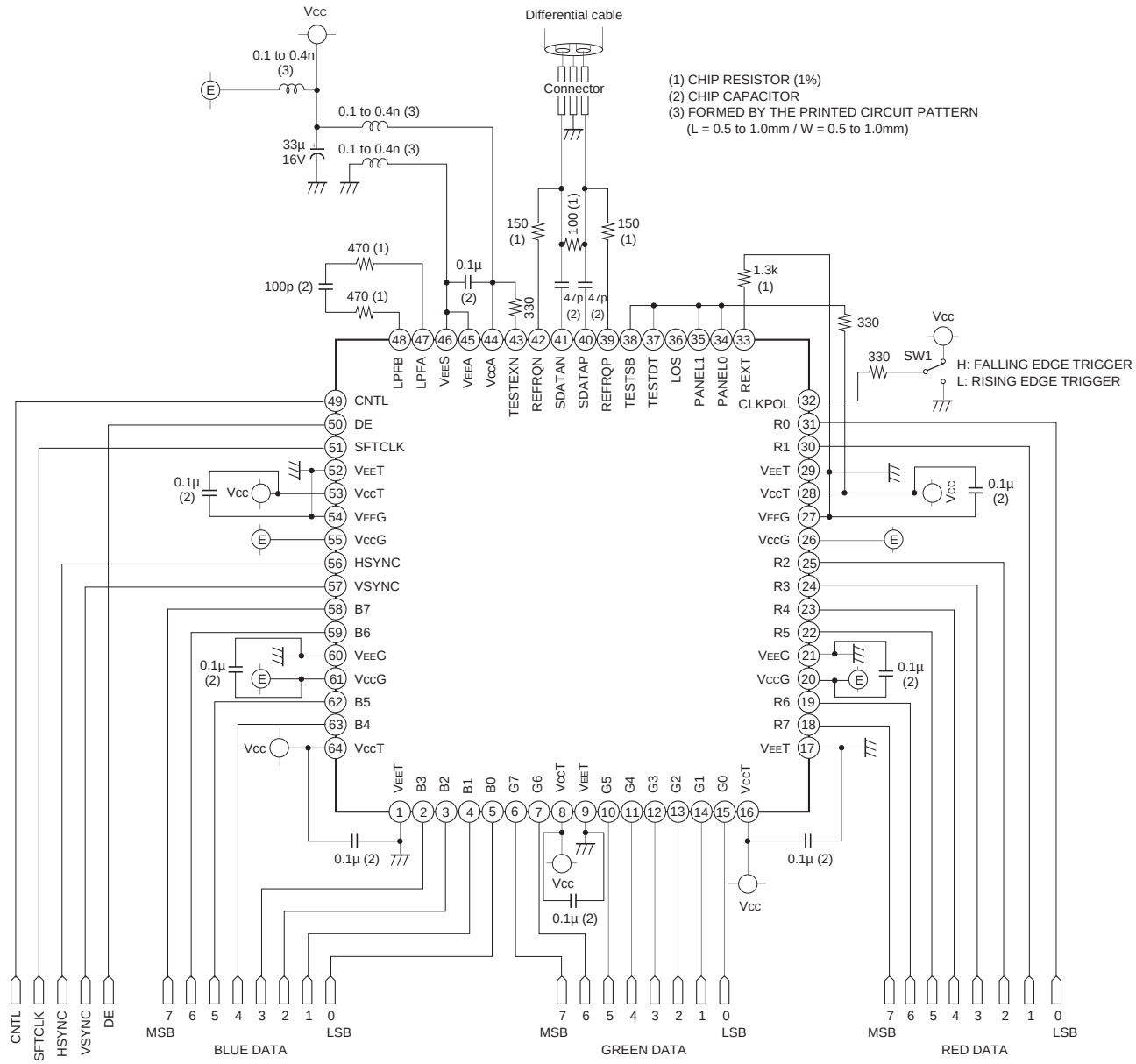


Fig. 9. Block Diagram of GVIF transceiver chip set

Application Cicuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Fig. 10. Recommended application circuit

Recommended Printed Circuit Board Structure

L1: Cu plate (18µm) + solder coat
I1: Fiber-glass epoxy core (0.3mm)
L2: Cu plate (36µm)
I2: Fiber-glass epoxy core (0.8mm)
L3: Cu plate (36µm)
I3: Fiber-glass epoxy core (0.3mm)
L4: Cu plate (18µm) + solder coat

Fig. 11. Recommended Printed Circuit Board Structure

Recommended Printed Circuit Board Pattern

POWER and special signal routing example

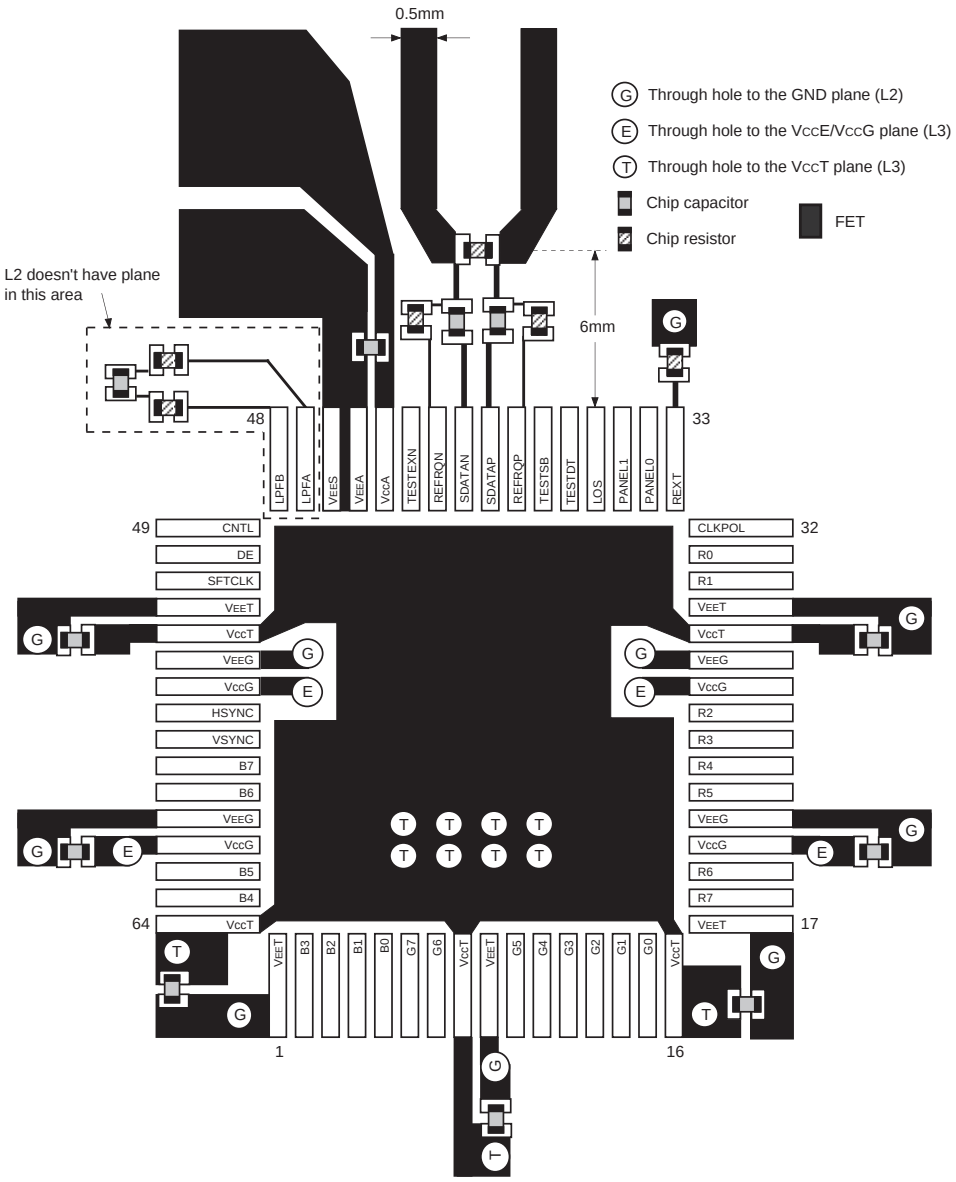


Fig. 12. Recommended Printed Circuit Board Pattern

Micro Strip Line

For maximum performance, the impedance between the pins SDDATAP/N of the LSI and the footprint of the connector should be 50Ω using a micro strip line. 50Ω impedance can be reached when using 0.5mm width pattern lines on L1 using this circuit board structure. The length of the lines should be identical and through-hole should not be used. L2 is recommended as the large ground plane.

Terminators

Terminators (100Ω resistor) should be located as close to the LSI as possible.

Filter Devices and Reference Registors

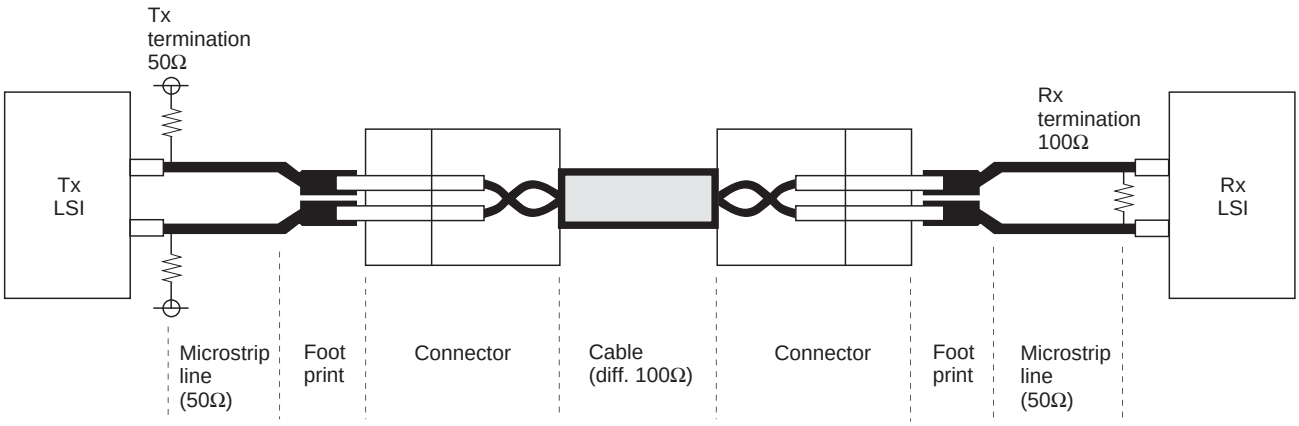
Capacitors and resistors which are connected to LPFA/B and REXT are filters and reference resistors. The region of Layer 2 (L2) is under the device and conductive patterns. The ground plane should be taken off in order to reduce parasitic capacitors.

Bypass Capacitors

Bypass capacitors (0.1µF SMD type) should be located as close to the pins as possible. Refer to the recommendation.

Recommendation for Cable and Connector Characteristics

The GVIF system uses terminators at both ends (transmitter and receiver), a cable equalizer and a small amplitude differential signal. In order to solve the problems of high speed data transmission such as signal reflection, reduce the signal level and EMI. In order to achieve the best solution, note the following:



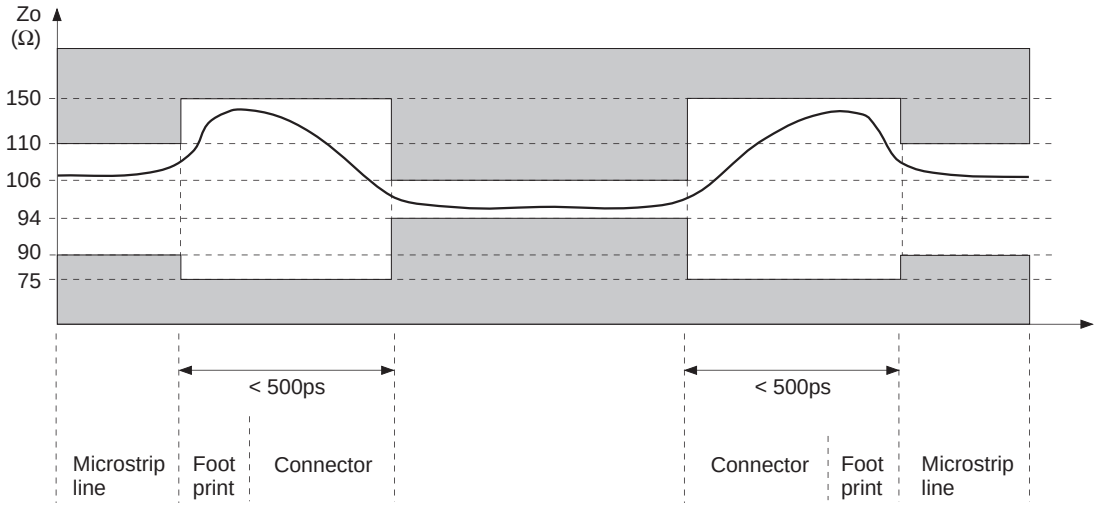
It is important to note the following issues for a good data transmission system:

- Good impedance matching
  Differential impedance should be fit to the recommended template on the next page.
- Cable loss should be small and the loss curve should be smooth.
  Maximum loss should be less than 15dB at 1GHz for the CXB1454R which has a built-in cable equalizer. See the next page.
- Skew of POS/NEG (differential signal) should be small
  Less than 12% of 1-bit time or 160ps@VGA, 100ps@SVGA, 60ps@XGA.
- Good EMI performance cable and connectors.

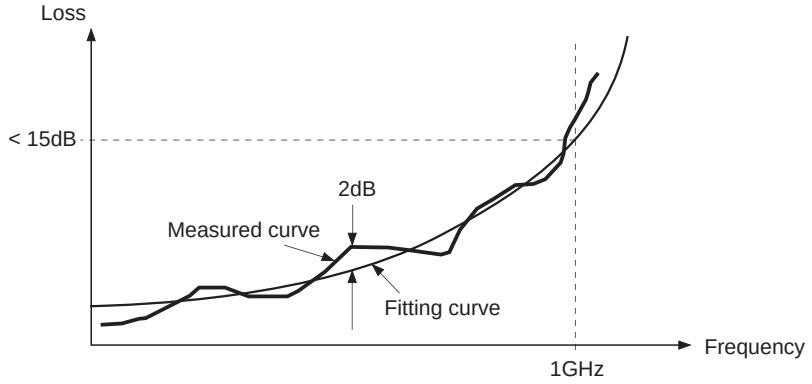
In order to satisfy these issues, the recommendations are as follows:

- Use the differential cable which provides good controlled impedance, low loss and good skew matching.
  A shielded twisted pair (STP) cable is recommended.
- Use a low reflectance connector.
- To minimize interference from other signals, high speed signal lengths should be identical.
- Use double shielded cable.

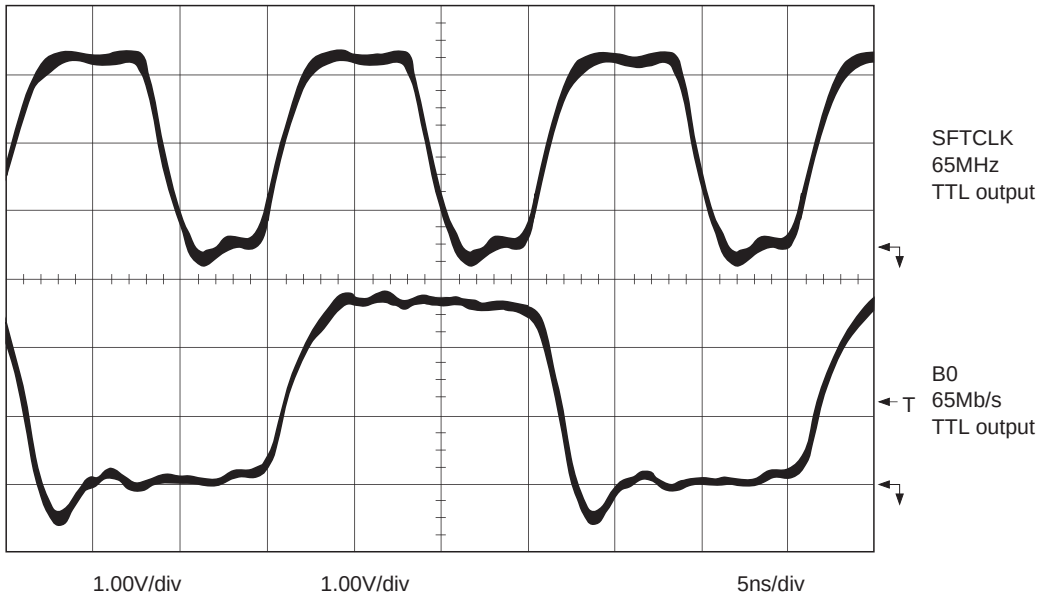
Recommended Transmission Path : Differential impedance template



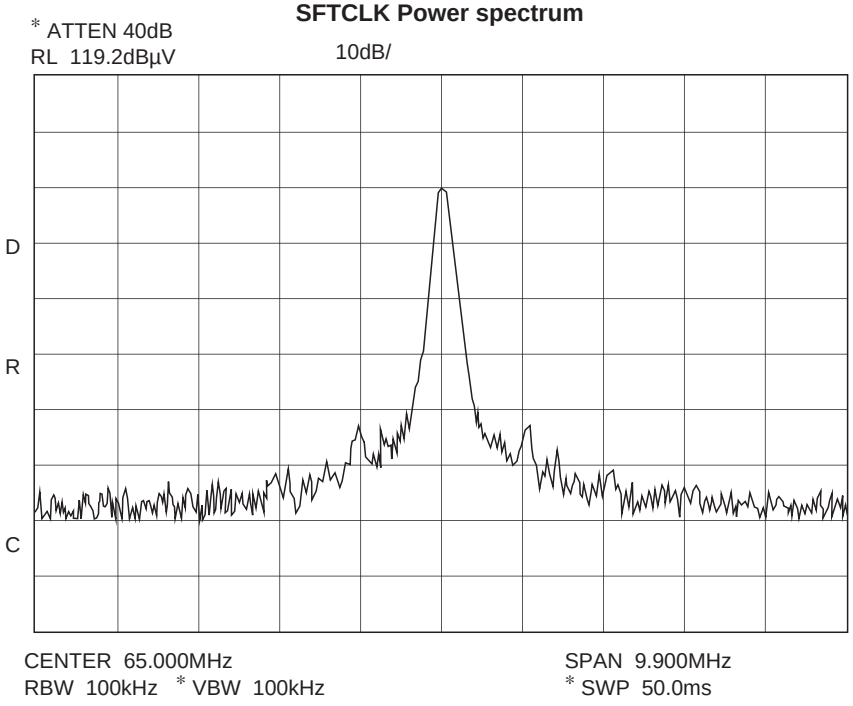
Recommended Transmission Path : Attennation Characteristics



TTL output waveform with C_L = 10pF

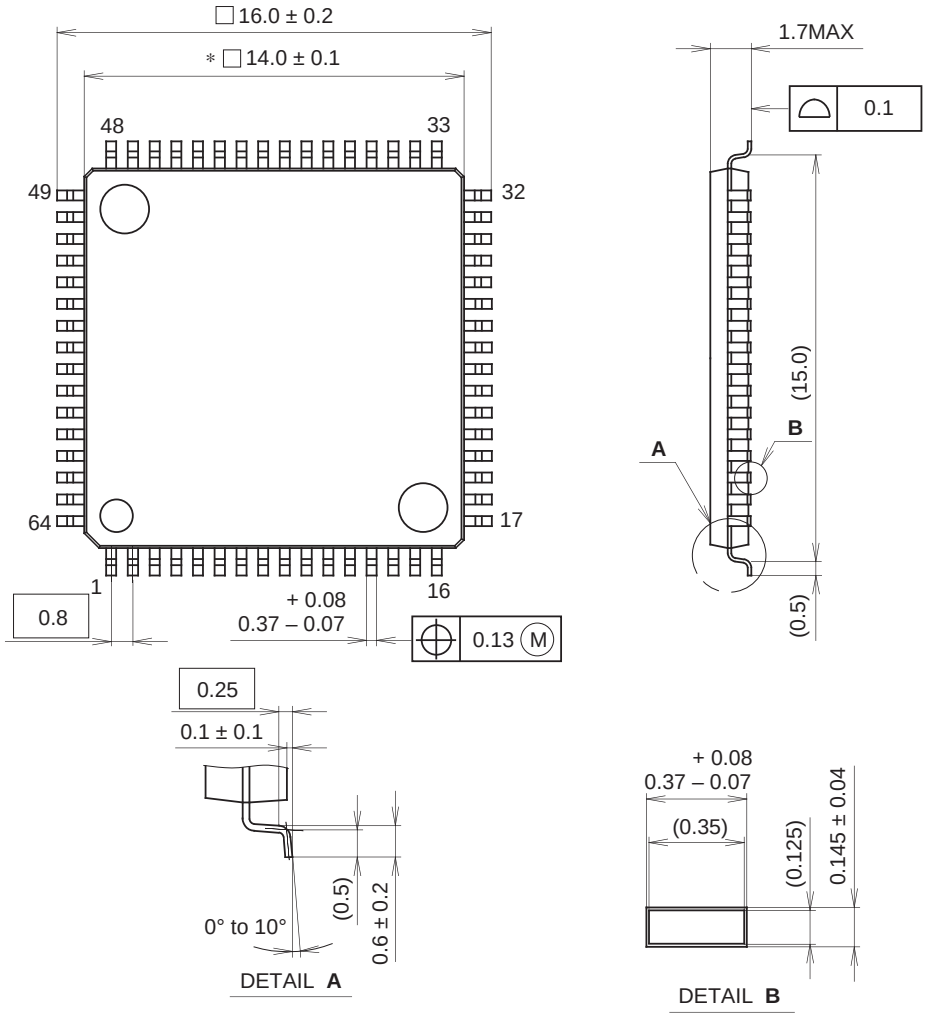


SFTCLK Power spectrum



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L02
EIAJ CODE	LQFP064-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).