SONY

CXD1178Q

8-bit 40MSPS RGB 3-channel D/A Converter

Description

The CXD1178Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, and others.

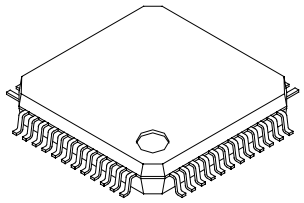
Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- RGB 3-channel input/output
- Differential linearity error ±0.3LSB
- Low power consumption 240 mW
  (200 Ω load at 2 Vp-p output)
- Single 5 V power supply
- Low glitch noise
- Stand-by function

Structure

Silicon gate CMOS IC

48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD}+0.5 to V_{SS}–0.5	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	2.0	V
• Clock pulse width	T_{PW1}, T_{PW0}	11.2 ns (min.) to 1.1 µs (max.)	
• Operating temperature	Topr	–40 to +85	°C

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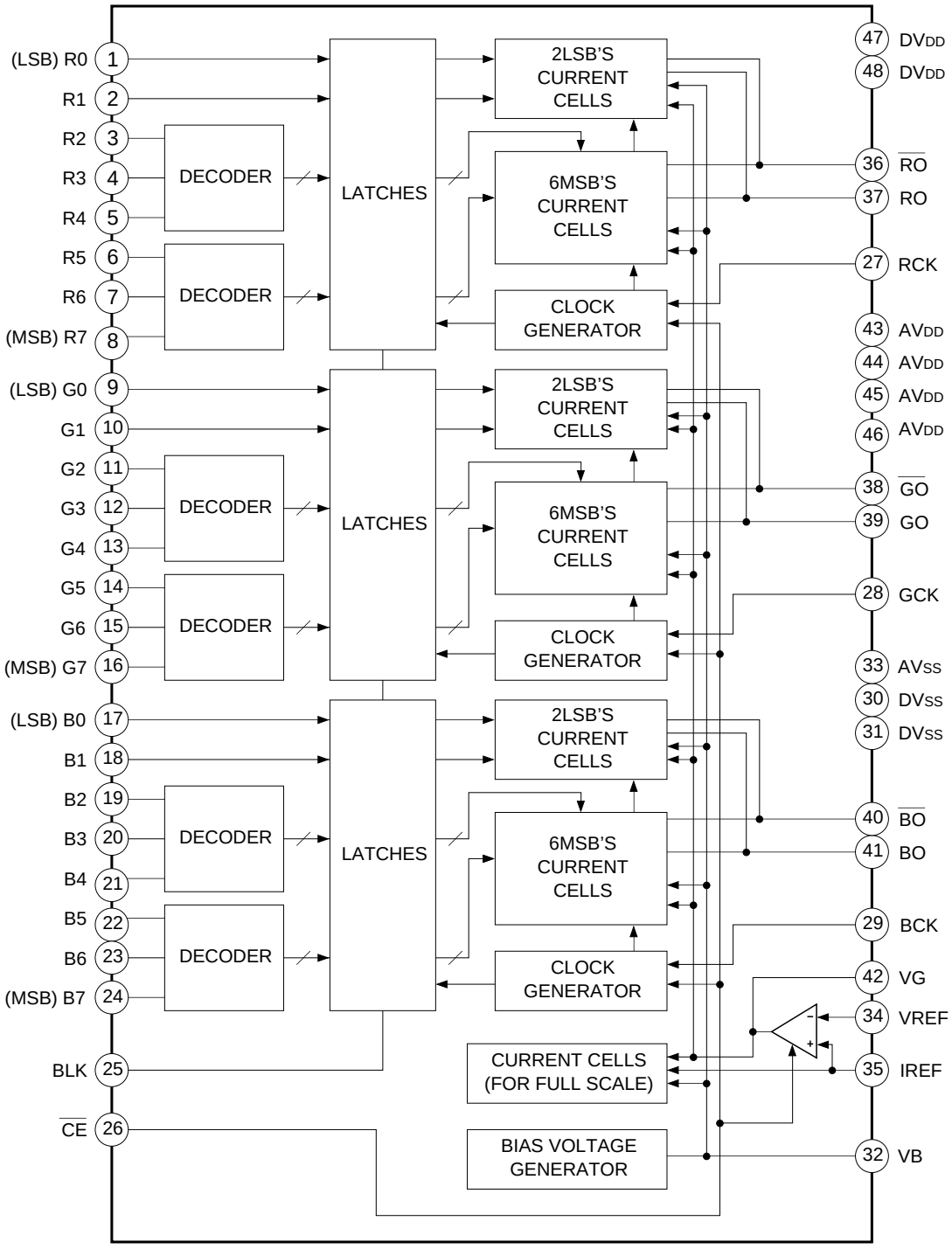
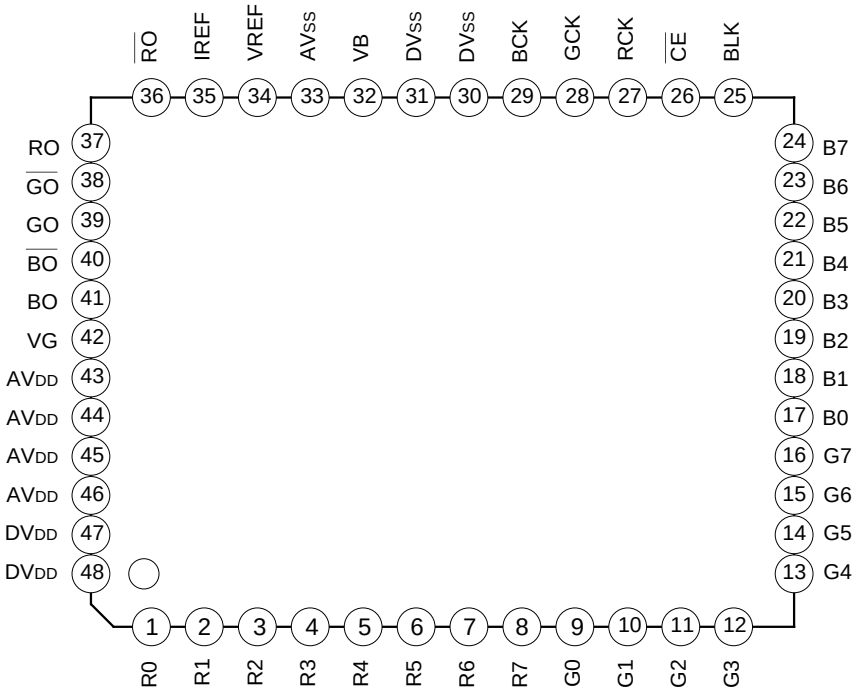
E90603H0Z-PS

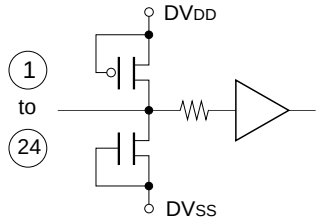
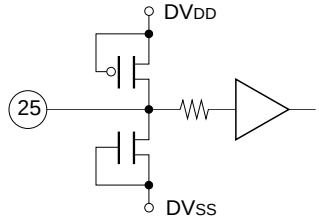
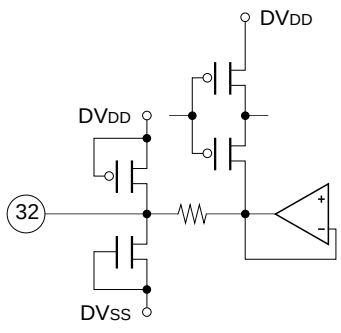
Block Diagram

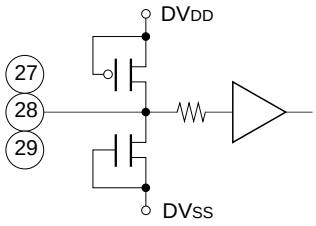
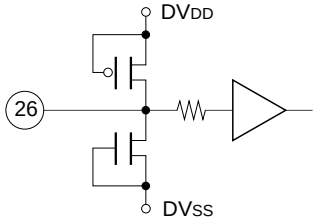
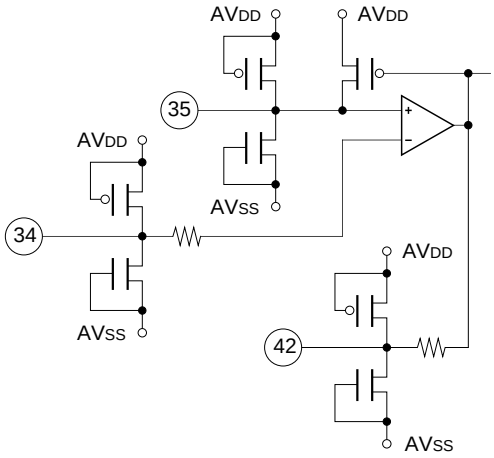


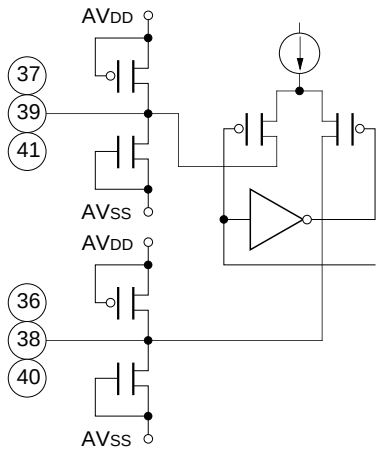
Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
1 to 8	R0 to R7	I		Digital input R0 (LSB) to R7 (MSB) G0 (LSB) to G7 (MSB) B0 (LSB) to B7 (MSB)
9 to 16	G0 to G7			
17 to 24	B0 to B7			
25	BLK	I		Blanking input. This is synchronized with the clock input signal for each channel. No signal at “H” (Output 0 V). Output condition at “L”.
32	VB	O		Connect a capacitor of about 0.1 µF.

Pin No.	Symbol	I/O	Equivalent circuit	Description
27	RCK	I		Clock input. Note) Even though 1 channel and/ or 2 channel are used, be sure to input the clock signal to RCK.
28	GCK			
29	BCK			
30, 31	DVSS	—		Digital GND
33	AVSS	—		Analog GND
26	$\overline{CE}$	I		Chip enable input. This is not synchronized with the clock input signal. No signal (Output 0 V) at “H” and minimizes power consumption.
35	IREF	O		Reference current output. Connect a resistance 16 times “16ROUT” that of output resistance value “ROUT”.
34	VREF	I		Reference voltage input. Set full scale output value.
42	VG	O		Connect a capacitor of about 0.1 µF.
43 to 46	AVDD	—		Analog VDD

Pin No.	Symbol	I/O	Equivalent circuit	Description
37	RO	O		Current output pins. Voltage output can be obtained by connecting a resistance.
39	GO			
41	BO			
36	$\overline{RO}$			Inverted current output. Normally dropped to analog GND.
38	$\overline{GO}$			
40	$\overline{BO}$			
47, 48	DV_{DD}	—		Digital V_{DD}

(f_{CLK}=40 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, V_{REF}=2.0 V, Ta=25 °C)

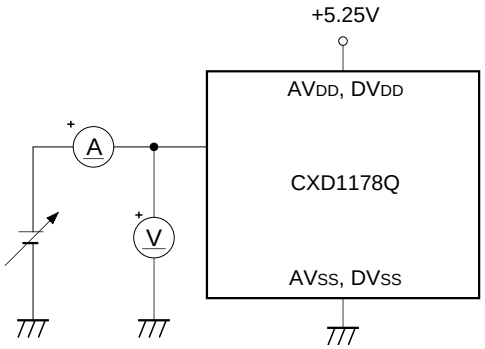
Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Resolution	n				8		bit
Conversion speed	f_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–40 to 85 °C		0.5		40	MSPS
Integral non-linearity error	E_L	Endpoint		–2.5		2.5	LSB
Differential non-linearity error	E_D			–0.3		0.3	LSB
Output full-scale voltage	V_{FS}			1.8	2.0	2.2	V
Output full-scale ratio *1	F_{SR}			0	1.5	3.0	%
Output full-scale current	I_{FS}				10	15	mA
Output offset voltage	V_{OS}	When “00000000” data input				1	mV
Glitch energy	GE	R_{OUT}=75 Ω			30		pV•s
Crosstalk	CT	When 1 MHz sine wave input			57		dB
Supply current	I_{DD}	14.3MHz color bar data input	$\overline{CE}$= “L”		42	48	mA
	I_{STB}		$\overline{CE}$= “H”		1	2	
Analog input resistance	R_{IN}	VREF		1			MΩ
Input capacitance	C_I					9	pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to 75 °C		2.4			V
	V_{IL}					0.8	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to 75 °C		–5		5	µA
	I_{IL}						
Setup time	t_s	R_{OUT}=75 Ω		5			ns
Hold time	t_h	R_{OUT}=75 Ω		10			ns
Propagation delay time	t_{PD}				10		ns
$\overline{CE}$ enable time *2	t_E	$\overline{CE}$= H→L			1.8	4	ms
$\overline{CE}$ disable time *2	t_D	$\overline{CE}$= L→H			1.8	4	ms

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100$ (%)

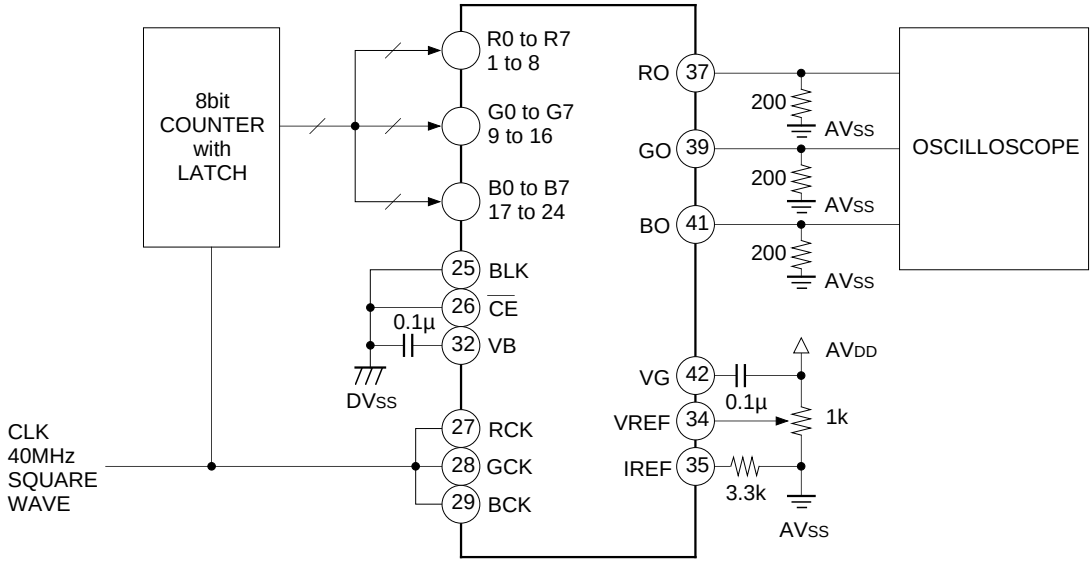
*2 When the external capacitor for the VG pin is 0.1 µF.

Electrical Characteristics Measurement Circuit

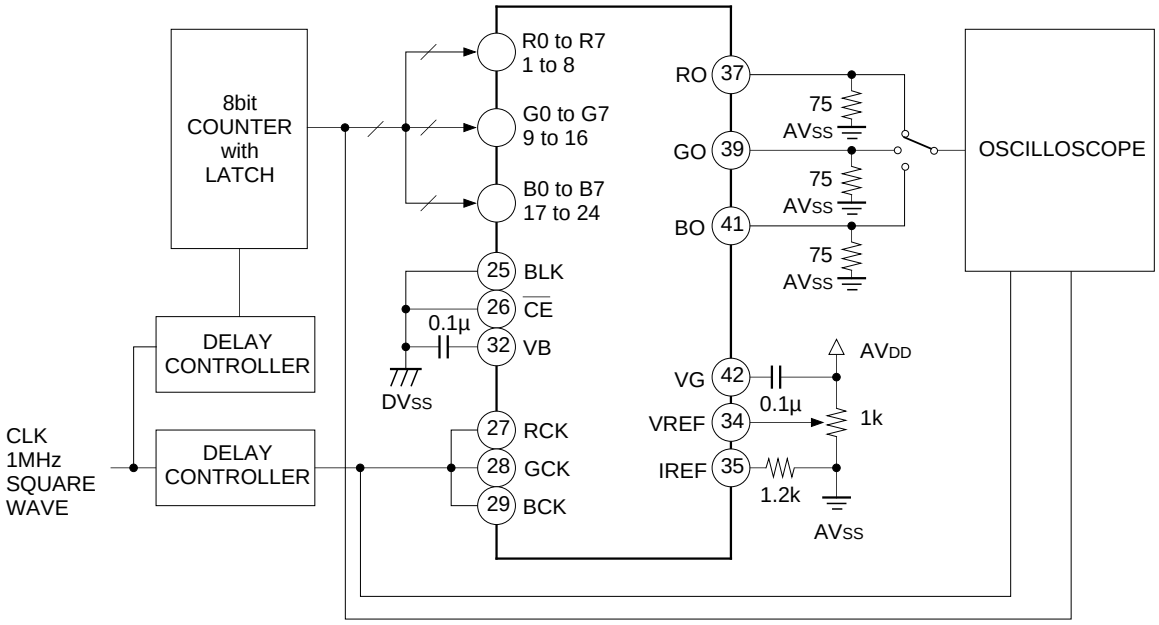
Analog Input Resistance
Digital Input Current } **Measurement Circuit**



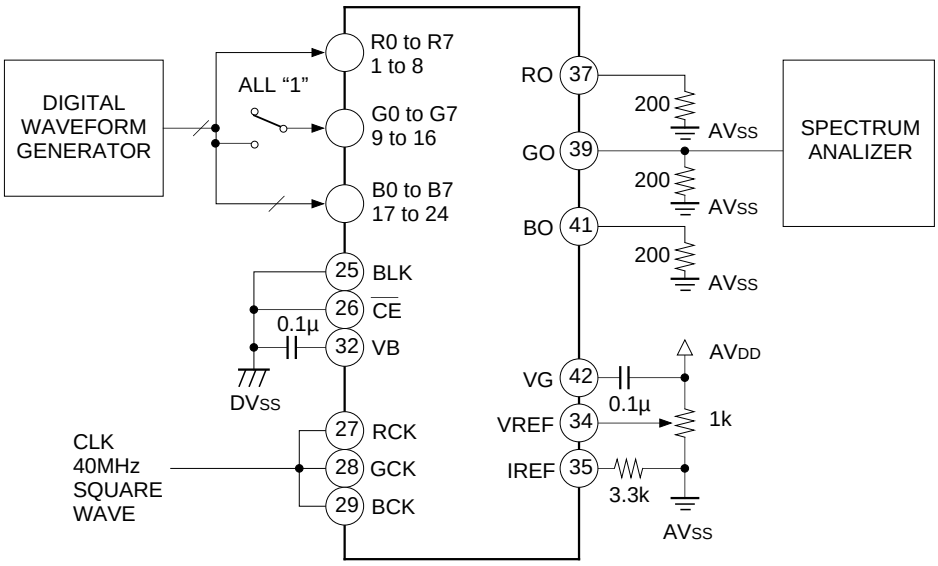
Maximum Conversion Velocity Measurement Circuit



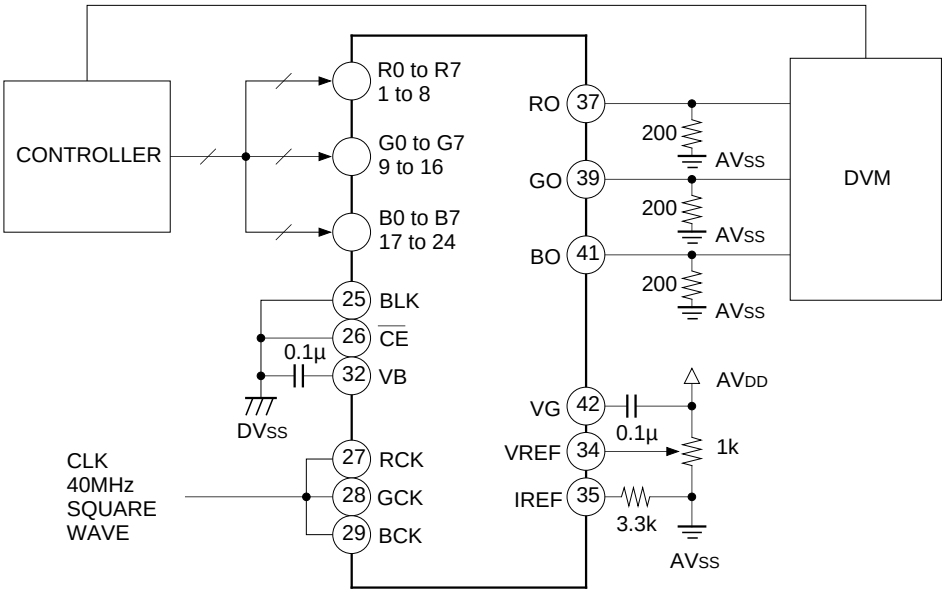
Setup Time
Hold Time } **Measurement Circuit**
Glitch Energy



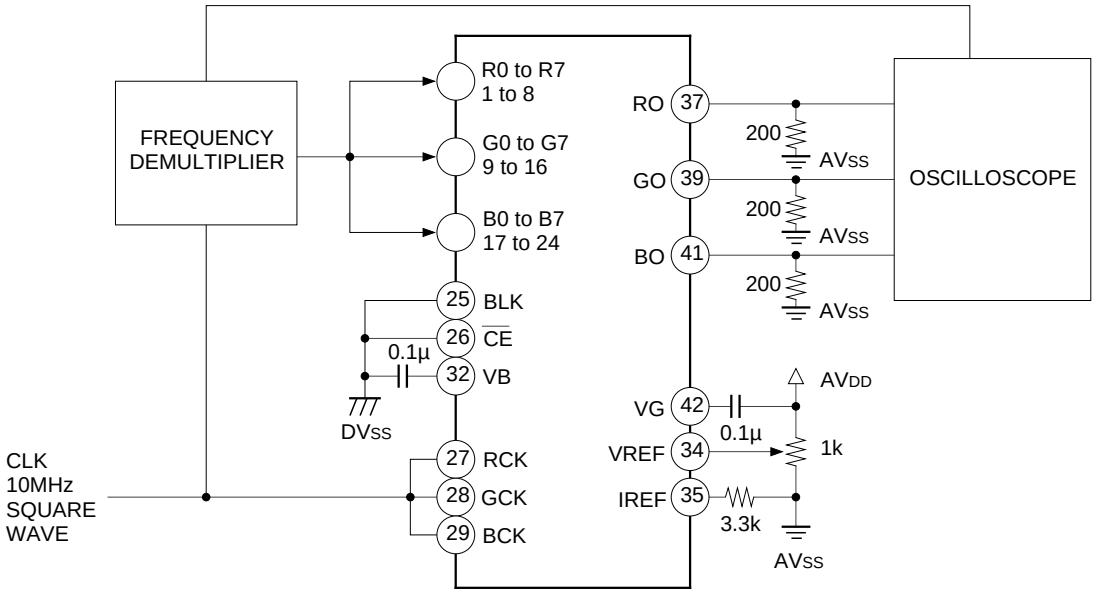
Crosstalk Measurement Circuit



DC Characteristics Measurement Circuit

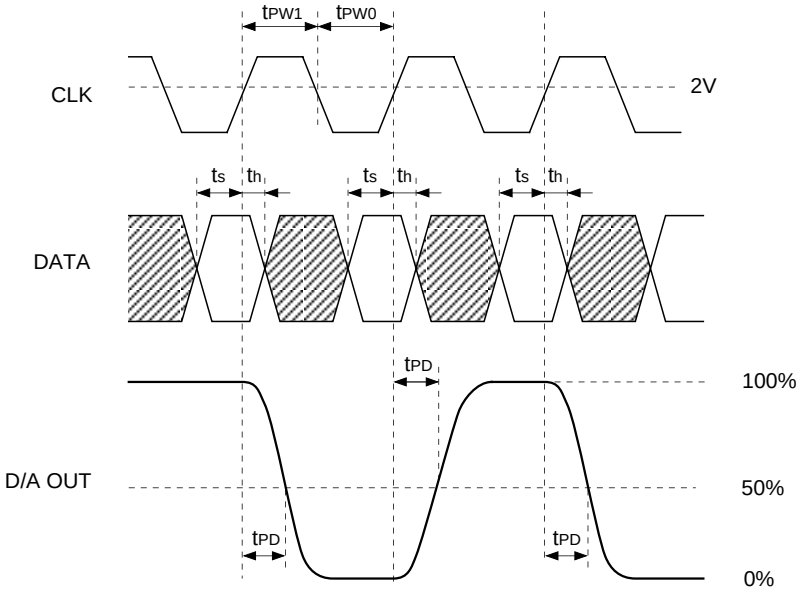


Propagation Delay Time Measurement Circuit



Description of Operation

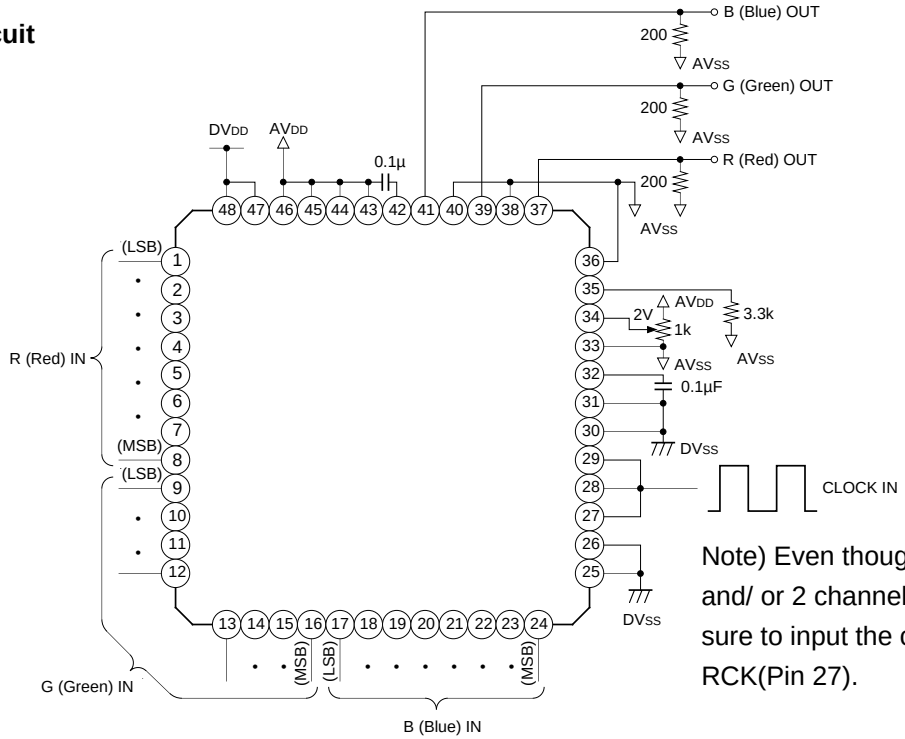
Timing Chart



I/O Chart (when full scale output voltage at 2.00 V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	2.0 V
:	
1 0 0 0 0 0 0 0	1.0 V
:	
0 0 0 0 0 0 0 0	0 V

Application Circuit



Note) Even though 1 channel and/ or 2 channel are used, be sure to input the clock signal to RCK(Pin 27).

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- How to select the output resistance

  The CXD1178Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to current output pins (RO, GO and BO). For specifications we have;

  Output full scale voltage V_{FS}=1.8 to 2.2 [V]

  Output full scale current I_{FS}=less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance is connected to reference current pin IREF. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute.

  Here please note that V_{FS} becomes

  $$V_{FS}=V_{REF} \times 16R_{OUT}/R_{IR}.$$

  V_{REF} is the voltage set at the VREF pin and R_{OUT} is the resistance connected to current output pins (RO, GO and BO) while R_{IR} is connected to IREF.

  Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- Power supply and ground

  To reduce noise effects separate analog and digital systems in the device periphery. For power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

- Latch up

  Analog and digital power supply have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

- On inverted current output pins

  The $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ are the inverted current output terminal as described in the Pin Description.

  The sums shown below become the constant value for any input data.

  a) The sum of the currents output from the $\overline{RO}$ and RO pins.

  b) The sum of the currents output from the $\overline{GO}$ and GO pins.

  c) The sum of the currents output from the $\overline{BO}$ and BO pins.

  However, the output current from the $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ pins is not guaranteed of its performances such as linearity errors, etc.

- On output full-scale voltage

  When the output full-scale voltage is used without adjustment in the application that uses the RGB signal, the color balance may be broke.

- Clock input signal

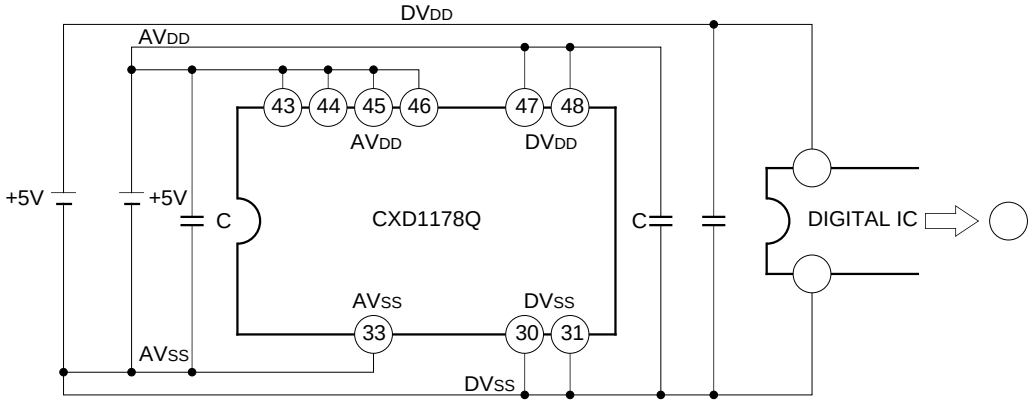
  Even though 1 channel and/ or 2 channel are used, be sure to input the clock signal to RCK(Pin 27).

Latch Up Prevention

The CXD1178Q is a CMOS IC which required latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 43 to 46) and DV_{DD} (Pins 47 and 48), when power supply is ON.

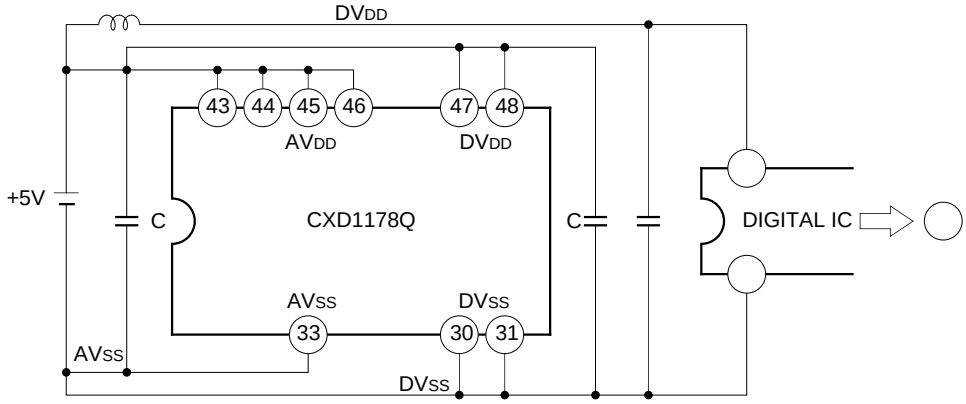
1. Correct usage

a. When analog and digital supplies are from different sources

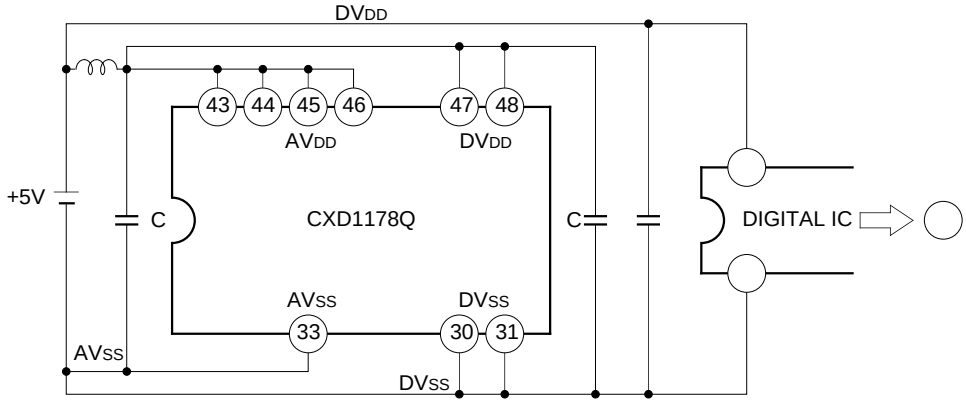


b. When analog and digital supplies are from a common source

(i)

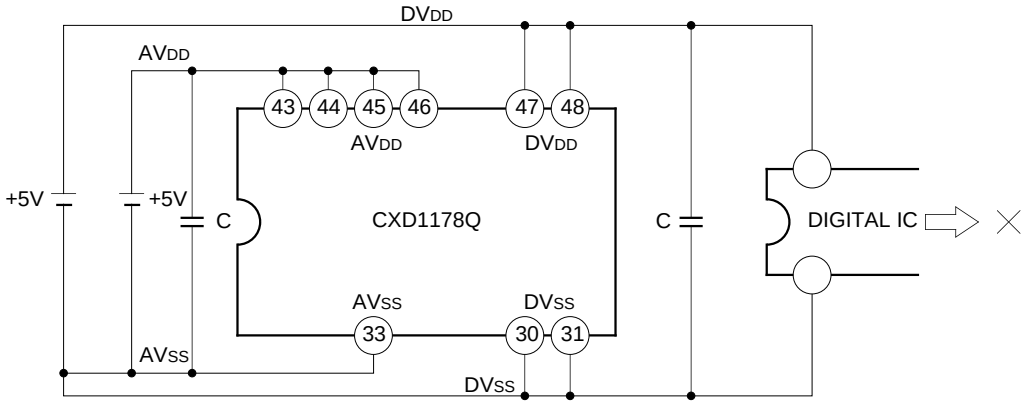


(ii)



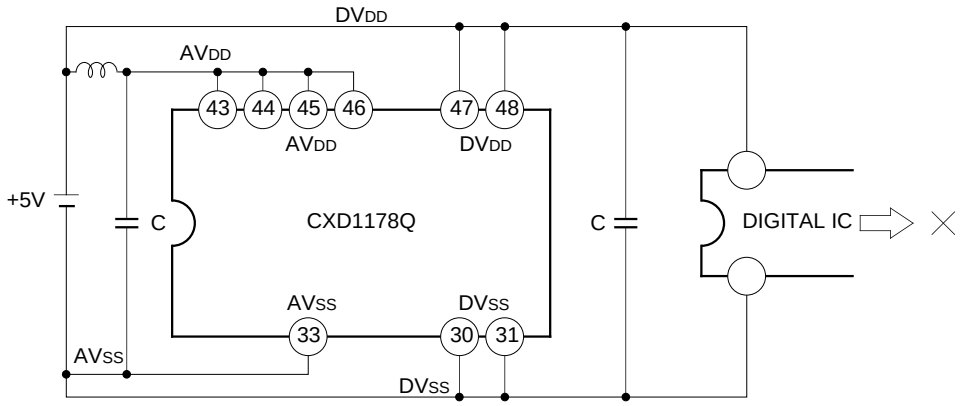
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

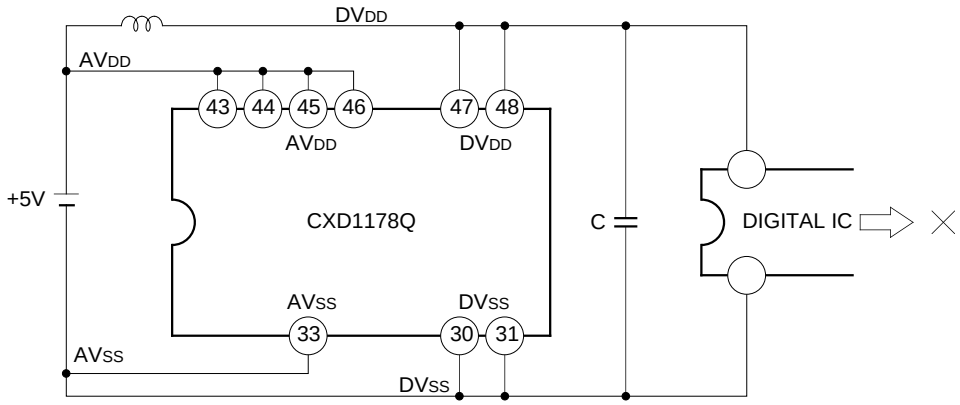


b. When analog and digital supplies are from common source

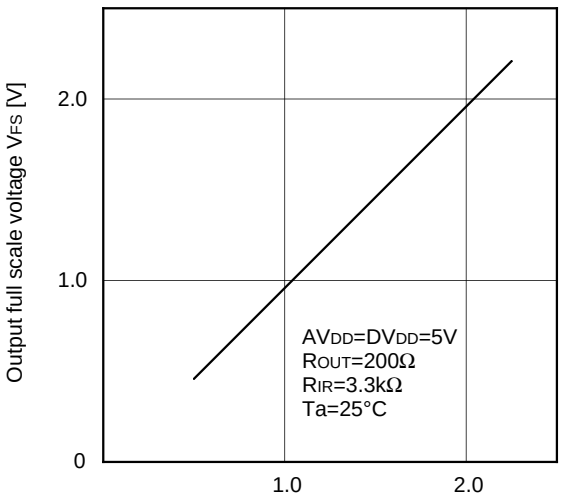
(i)



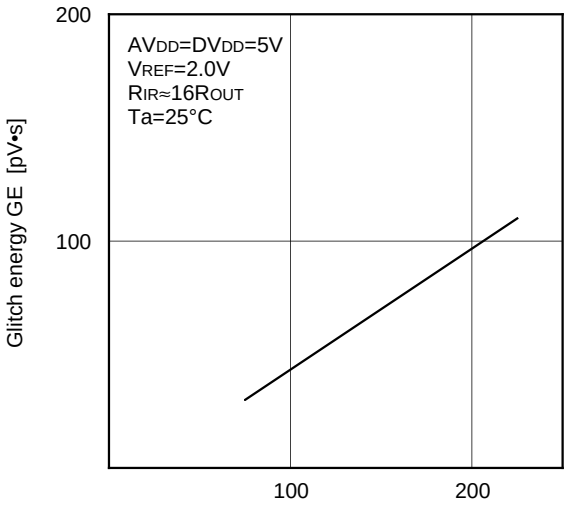
(ii)



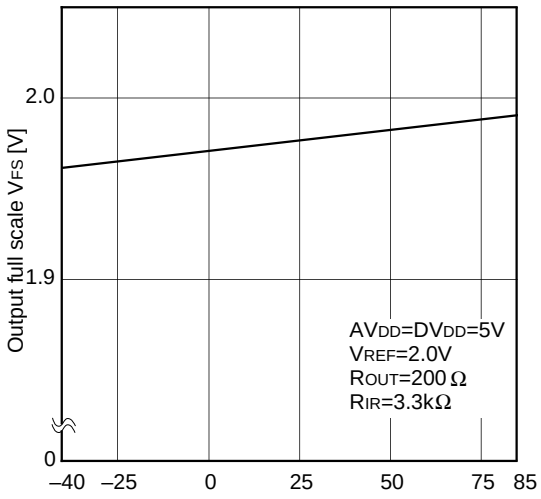
Example of Representative Characteristics



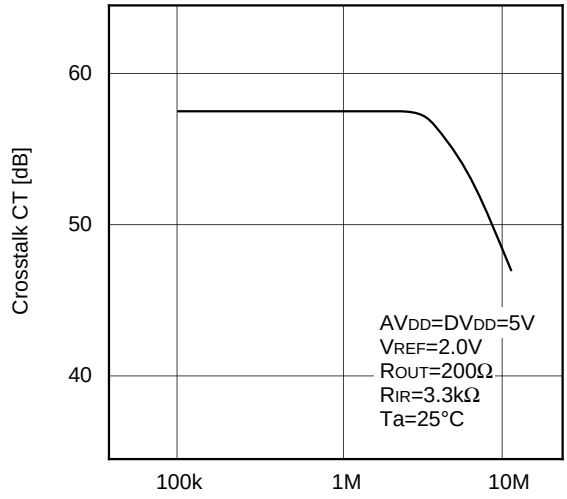
Output full scale voltage vs. Reference voltage



Glitch energy vs. Output resistance



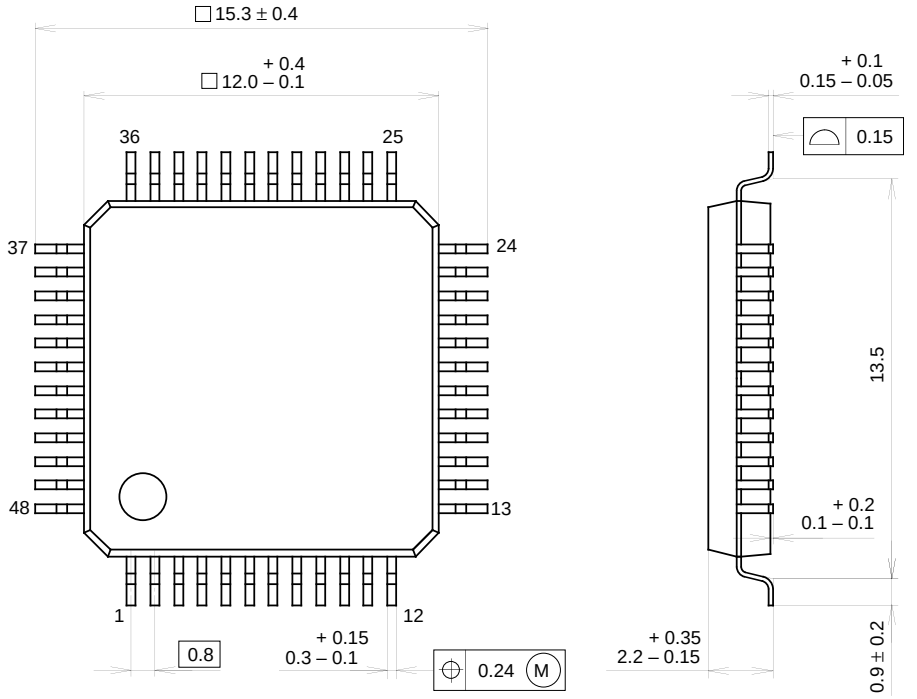
Output full scale voltage vs. Ambient temperature



Crosstalk vs. Output frequency

Package Outline Unit : mm

48PIN QFP (PLASTIC)



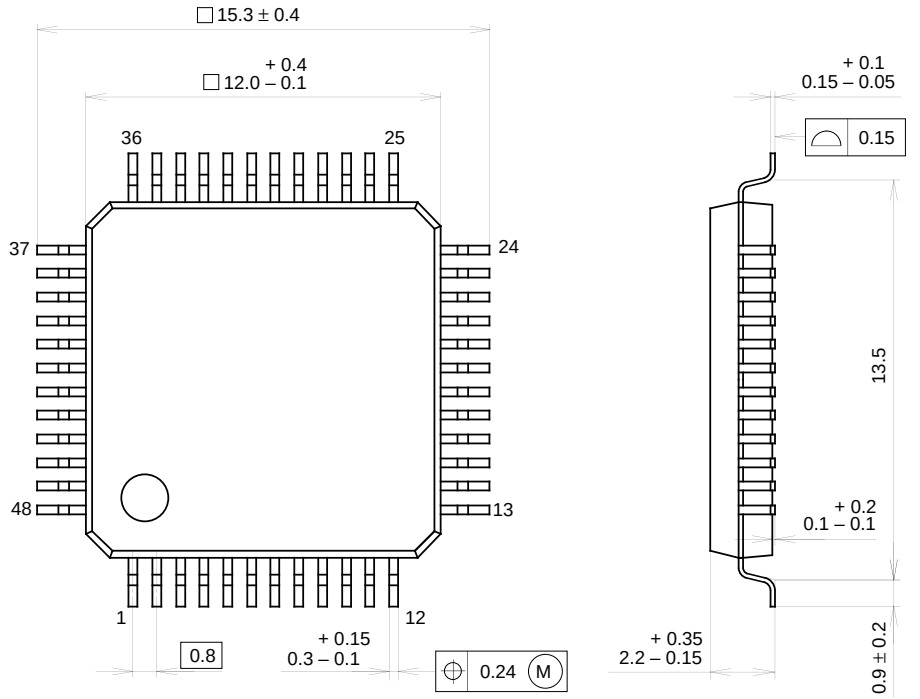
SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

Package Outline Unit : mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g