

8-bit 35MSPS Video A/D Converter with Clamp Function

Description

The CXD1179Q is an 8-bit CMOS A/D converter for video with synchronizing clamp function. The adoption of 2 step-parallel method achieves ultra-low power consumption and a maximum conversion speed of 35MSPS.

Features

- Resolution: 8-bit $\pm 1/2$ LSB (DL)
- Maximum sampling frequency: 35MSPS
- Low power consumption: 80 mW (at 35MSPS typ.) (reference current excluded)
- Synchronizing clamp function
- Clamp ON/OFF function
- Reference voltage self bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5V power supply
- Low input capacitance: 8 pF
- Reference impedance: 330 Ω (typ.)

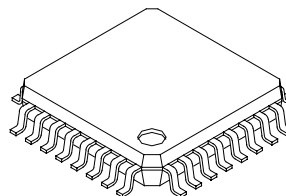
Applications

Wide range of applications that require high-speed A/D conversion such as TV and VCR.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)

**Absolute Maximum Ratings** (Ta=25 °C)

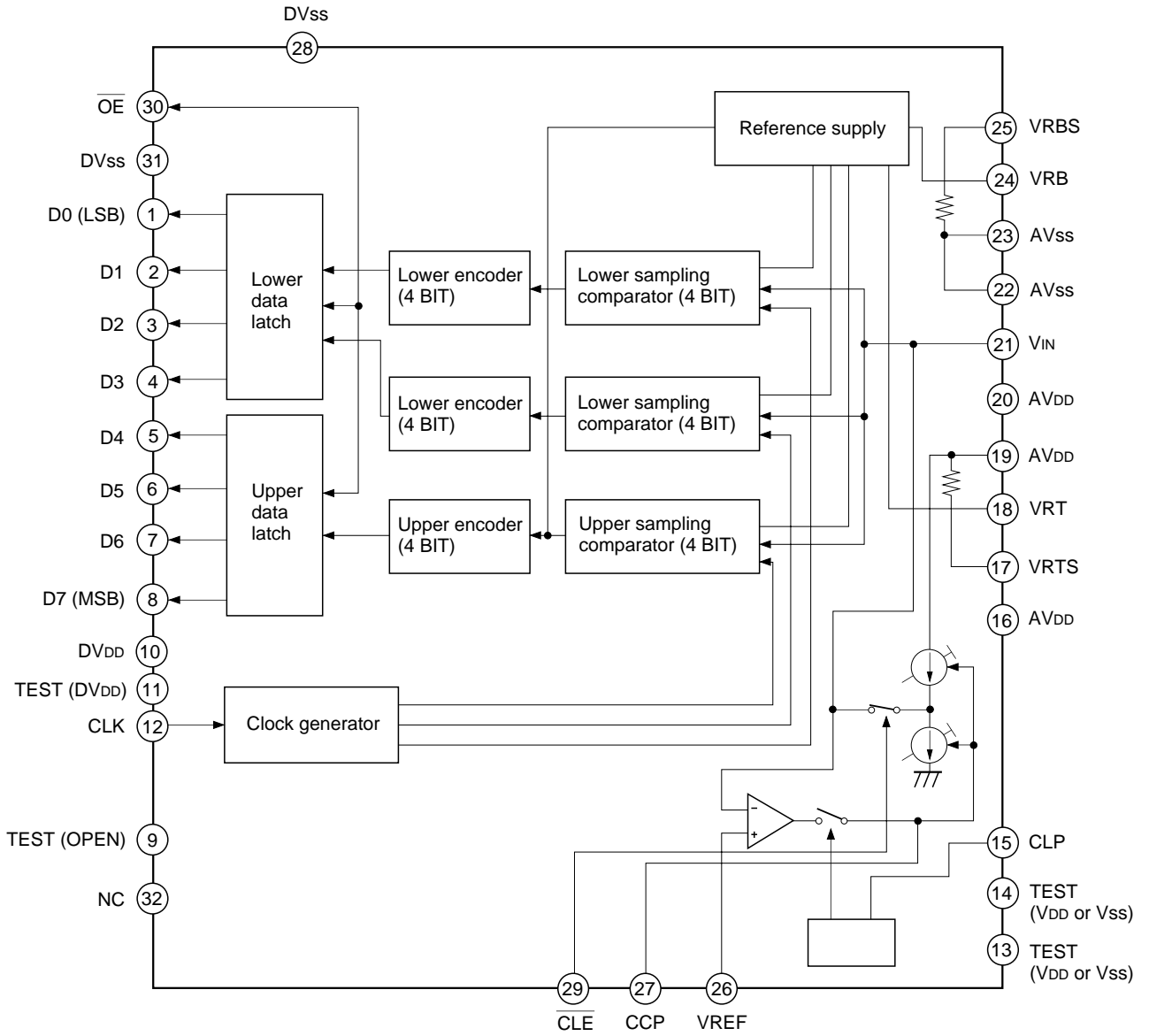
• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	$V_{DD} + 0.5$ to $V_{SS} - 0.5$	V
• Input voltage (Analog)	V_{IN}	$V_{DD} + 0.5$ to $V_{SS} - 0.5$	V
• Input voltage (Digital)	V_I	$V_{DD} + 0.5$ to $V_{SS} - 0.5$	V
• Output voltage (Digital)	V_O	$V_{DD} + 0.5$ to $V_{SS} - 0.5$	V
• Storage temperature	T_{stg}	-55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}		
	$ DV_{SS} - AV_{SS} $	0 to 100	mV
• Reference input voltage	V_{RB}	0 and above	V
	V_{RT}	2.7 and below	V
• Analog input	V_{IN}	1.8 Vp-p above	
• Clock pulse width	T_{pw1}, T_{pw0}	13 ns (min) to 1.1 μ s (max)	
• Operating ambient temperature	T_{opr}	-40 to +85	°C

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Block Diagram



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) output
9	TEST		Leave open during normal usage.
10	DVDD		Digital +5 V
12	CLK		Clock input
11, 13, 14	TEST		Fix Pin 11 to VDD, Pins 13 and 14 to VDD or VSS during normal usage.

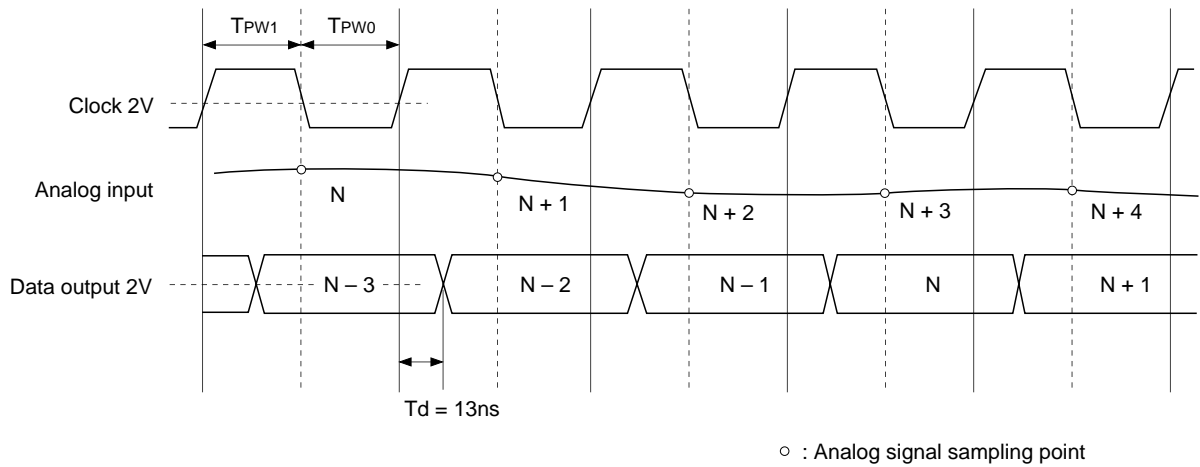
Pin No.	Symbol	Equivalent circuit	Description
15	CLP		Inputs clamp pulse to Pin 15 (CLP). Clamps the signal voltage during Low interval.
16, 19, 20	AVDD		Analog +5 V
17	VRTS		Generates about +2.6 V when shorted with VRT.
18	VRT		Reference voltage (top)
24	VRB		Reference voltage (bottom)
21	V _{IN}		Analog input
22, 23	AVSS		Analog ground
25	VRBS		Generates about +0.6 V when shorted with VRB.

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		Clamp reference voltage input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DVSS		Digital ground
29	\overline{CLE}		The clamp function is enabled when $\overline{CLE} = \text{Low}$. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE} = \text{High}$. The clamp pulse can be measured by connecting \overline{CLE} to DV_{DD} through a several hundred Ω resistor.
30	\overline{OE}		Data is output when $\overline{OE} = \text{Low}$. Pins D0 to D7 are at high impedance when $\overline{OE} = \text{High}$.
32	NC		NC pin

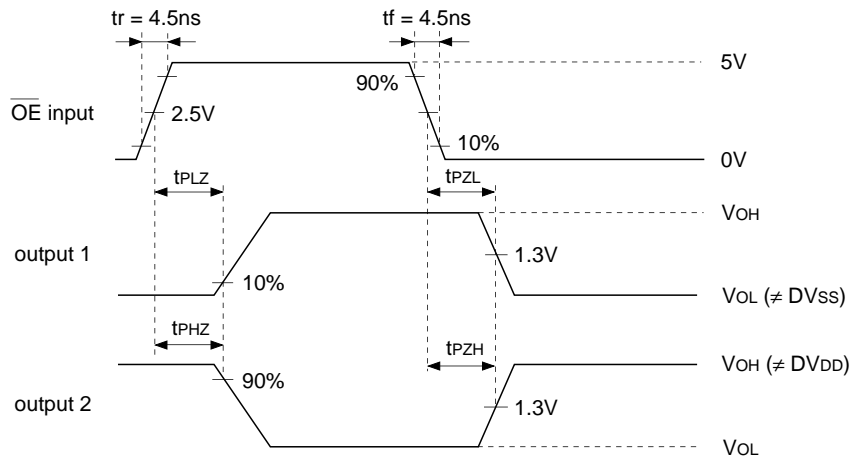
Digital Output

The following table shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code	
		MSB	LSB
V_{RT}	0	1 1 1 1 1 1 1 1	
⋮	⋮	⋮	
	127	1 0 0 0 0 0 0 0	
⋮	⋮	⋮	
	128	0 1 1 1 1 1 1 1	
⋮	⋮	⋮	
V_{RB}	255	0 0 0 0 0 0 0 0	



Timing Chart I.



Timing Chart II.

Electrical Characteristics

Analog characteristics

(F_C = 35MSPS, V_{DD} = 5 V, V_{RB} = 0.5 V, V_{RT} = 2.5 V, T_a = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Conversion speed	F _C	V _{DD} = 4.75 to 5.25 V T _a = -40 to +85 °C V _{IN} = 0.5 to 2.5 V f _{IN} = 1 kHz ramp	0.5		35	MSPS	
Analog input band width (-1 dB)	BW	Envelope		25		MHz	
Offset voltage*1	E _{OT}	Potential difference to V _{RT}	-60	-40	-20	mV	
	E _{OB}	Potential difference to V _{RB}	+55	+75	+95		
Integral non-linearity error	E _L	End point		+0.5	+1.3 -1.0	LSB	
Differential non-linearity error	E _D			±0.3	±0.5		
Differential gain error	DG	NTSC 40 IRE mod ramp F _C = 14.3MSPS		1		%	
Differential phase error	DP			0.5		deg	
Aperture jitter	t _{aj}			30		ps	
Sampling delay	t _{sd}			2		ns	
Clamp offset voltage*2	E _{oc}	V _{IN} = DC, PWS = 3 μs	V _{REF} = 0.5 V	-20	0	+20	mV
			V _{REF} = 2.5 V	-30	-10	+10	
Clamp pulse delay	t _{cpd}			25		ns	

*1 The offset voltage E_{OB} is a potential difference between V_{RB} and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from "00000000" to "00000001".
E_{OT} is a potential difference between V_{RT} and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from "11111111" to "11111110".

*2 Clamp offset voltage varies individually. When using with R, G, B 3 channels, color sliding may be generated.

DC characteristics

(F_C = 35MSPS, V_{DD} = 5 V, V_{RB} = 0.5 V, V_{RT} = 2.5 V, T_a = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Supply current	I _{DD}	F _C = 35MSPS NTSC ramp wave input		16	22	mA	
Reference pin current	I _{REF}		4.5	6.1	8.7	mA	
Analog input capacitance	C _{IN}	V _{IN} = 1.5 V + 0.07 V _{rms}		8		pF	
Reference resistance (V _{RT} to V _{RB})	R _{REF}		230	330	440	Ω	
Self-bias I	V _{RB1}	Shorts V _{RB} and V _{RB} S Shorts V _{RT} and V _{RT} S	0.52	0.56	0.60	V	
	V _{RT1} – V _{RB1}		1.96	2.10	2.24		
Self-bias II	V _{RT2}	V _{RB} = AGND Shorts V _{RT} and V _{RT} S	2.13	2.33	2.53	V	
Digital input voltage	V _{IH}	V _{DD} = 4.75 to 5.25 V T _a = –40 to +85 °C	3.5			V	
	V _{IL}				0.5		
Digital input current	I _{IH}	V _{DD} = max	V _{IH} = V _{DD}			5	μA
	I _{IL}		V _{IL} = 0 V			5	
Digital output current	I _{OH}	OE = V _{SS} V _{DD} = min	V _{OH} = V _{DD} – 0.5 V	–1.1	–2.5		mA
	I _{OL}		V _{OL} = 0.4 V	3.7	6.5		
	I _{ozH}	OE = V _{DD} V _{DD} = max	V _{OH} = V _{DD}			16	μA
	I _{ozL}		V _{OL} = 0 V			16	

Timing

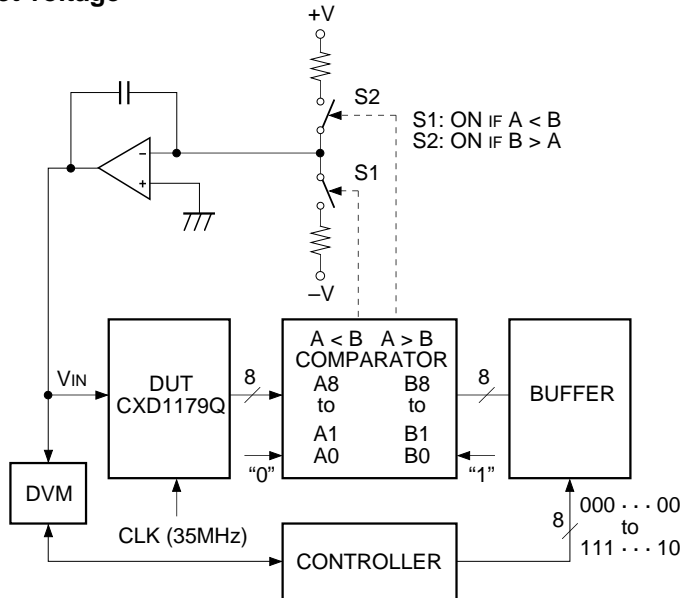
(F_C = 35MSPS, V_{DD} = 5 V, V_{RB} = 0.5 V, V_{RT} = 2.5 V, T_a = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output data delay	T _{DL}	With TTL 1 gate and 10 pF load V _{DD} = 4.75 to 5.25 V T _a = –40 to +85 °C	7	13	18	ns
Tri-state output enable time	t _{PZH}	R _L = 1 kΩ, C _L = 15 pF OE = 5 V → 0 V V _{DD} = 4.75 to 5.25 V T _a = –40 to +85 °C	5	8	14	ns
	t _{PZL}					
Tri-state output disable time	t _{PHZ}	R _L = 1 kΩ, C _L = 15 pF OE = 0V → 5 V V _{DD} = 4.75 to 5.25 V T _a = –40 to +85 °C	4	6.5	11	ns
	t _{PLZ}					
Clamp pulse width*1	t _{cpw}	F _C = 14MSPS, C _{IN} = 10 μF for NTSC wave	1.75	2.75	3.75	μs

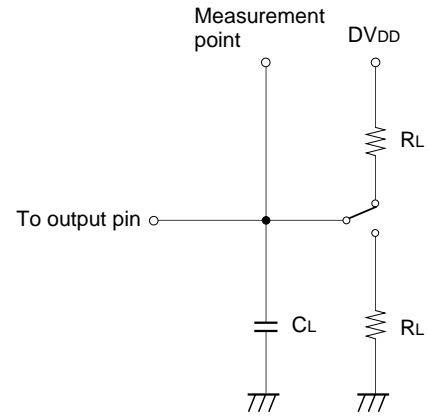
*1 The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75 kHz for NTSC) for other processing systems to equal the values for NTSC.

Electrical Characteristics Measurement Circuit

Integral non-linearity error } measurement circuit
 Differential non-linearity error }
 Offset voltage }

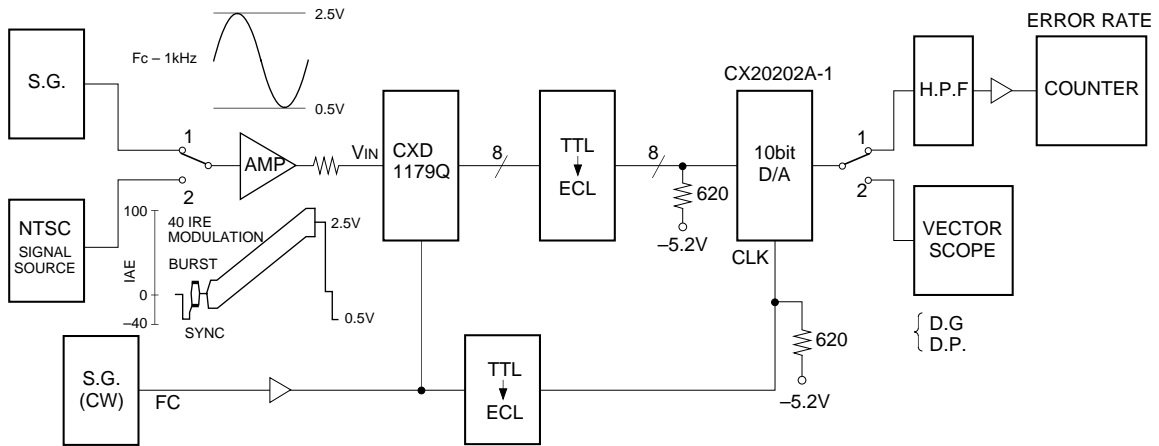


Tri-state output measurement circuit

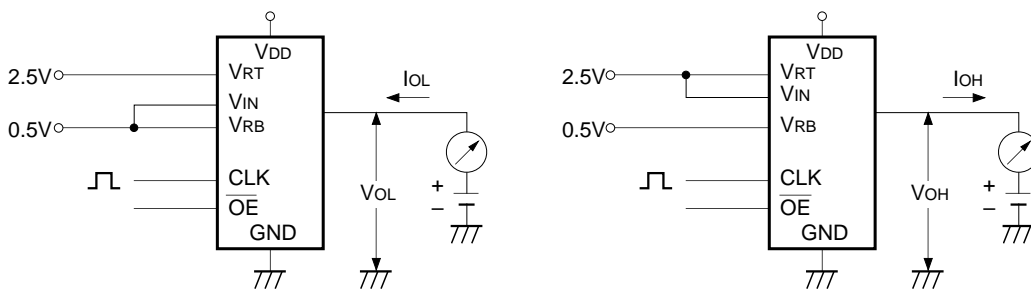


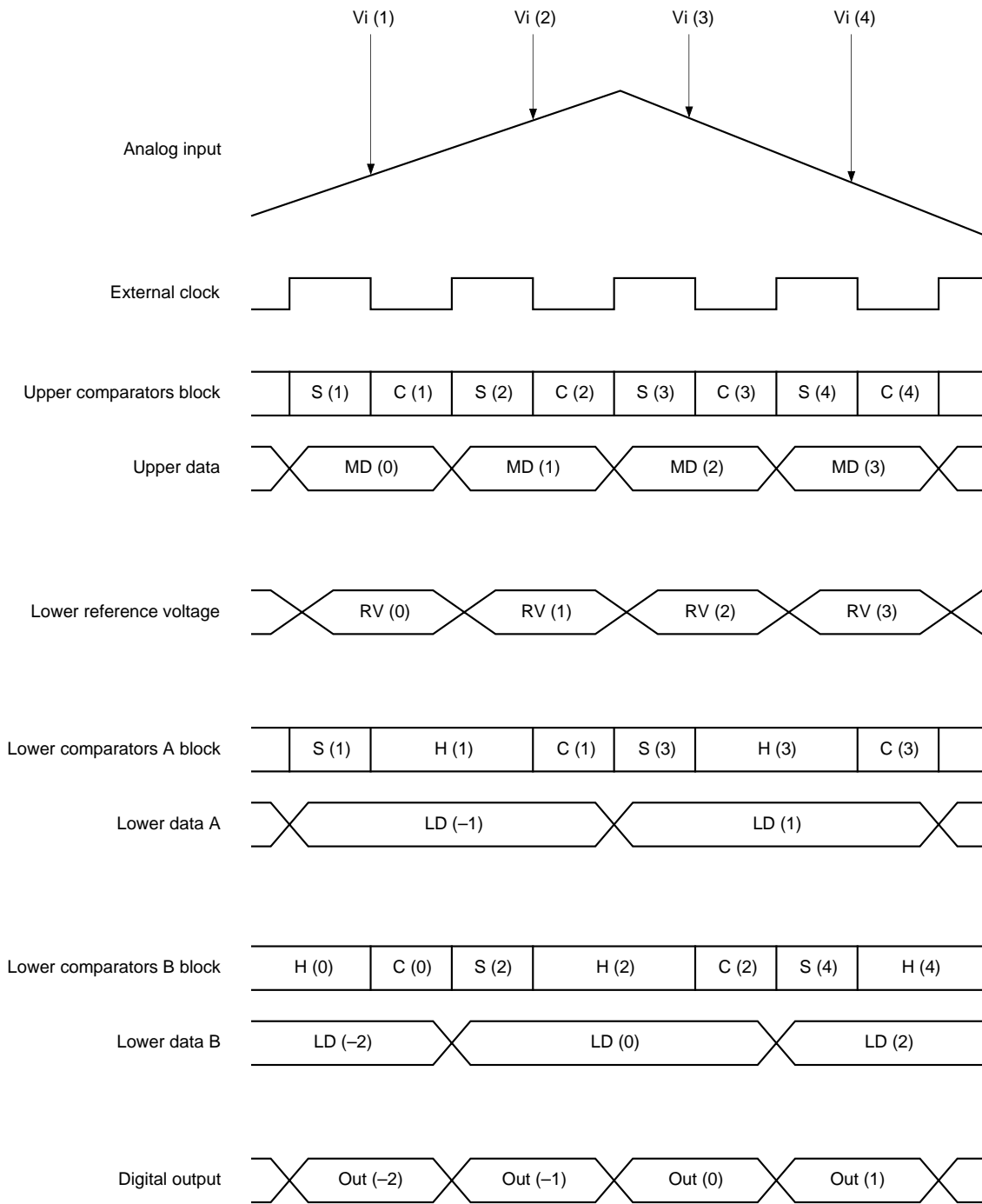
Note) CL includes capacitance of the probe and others.

Maximum operational speed } measurement circuit
 Differential gain error }
 Differential phase error }



Digital output current measurement circuit





Timing Chart 3

Operation (See Block Diagram and Timing Chart 3)

1. The CXD1179Q is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between VRT – VRB/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of VRT (Reference voltage top) and VRB (Reference voltage bottom).

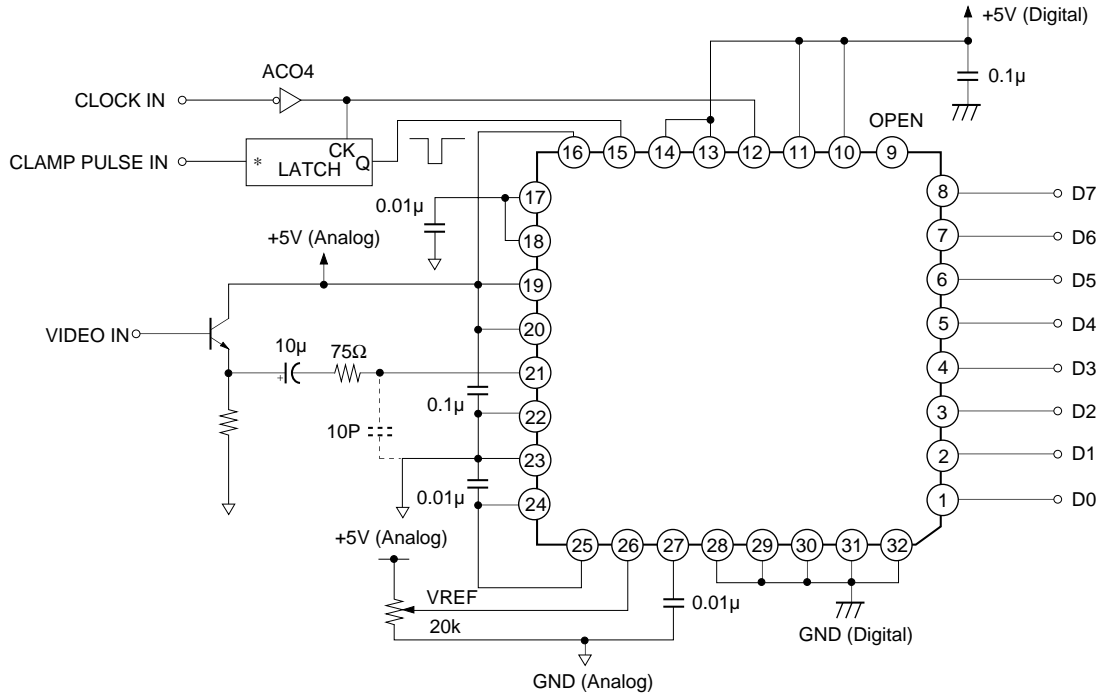
2. This IC uses an offset cancel type comparator and the comparator operates synchronously with an external clock. These modes are respectively indicated on the timing chart with S, H, C symbols. That is, the comparator performs input sampling (auto zero) mode, input hold mode and comparison mode using the external clock.
3. The operation of respective parts is as indicated in the chart. For instance input voltage V_i (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. Power supply and ground
To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog power supply pins, use a ceramic capacitor of about 0.1 μF set as close as possible to the pin to bypass to the respective grounds.
2. Analog input
Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.
3. Clock input
The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.
4. Reference input
Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to analog ground, by means of a capacitor about 0.1 μF , the stable characteristics of the reference voltage are obtained. By shorting V_{RT} and V_{RTS} , V_{RB} and V_{RBS} , the self-bias function that generates $V_{RT} = \text{about } 2.6 \text{ V}$ and $V_{RB} = \text{about } 0.6 \text{ V}$, is activated.
5. Timing
Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 13ns.
6. $\overline{\text{OE}}$ pin
By connecting $\overline{\text{OE}}$ to DV_{SS} output mode is obtained. By connecting $\overline{\text{OE}}$ to DV_{DD} high impedance is obtained.

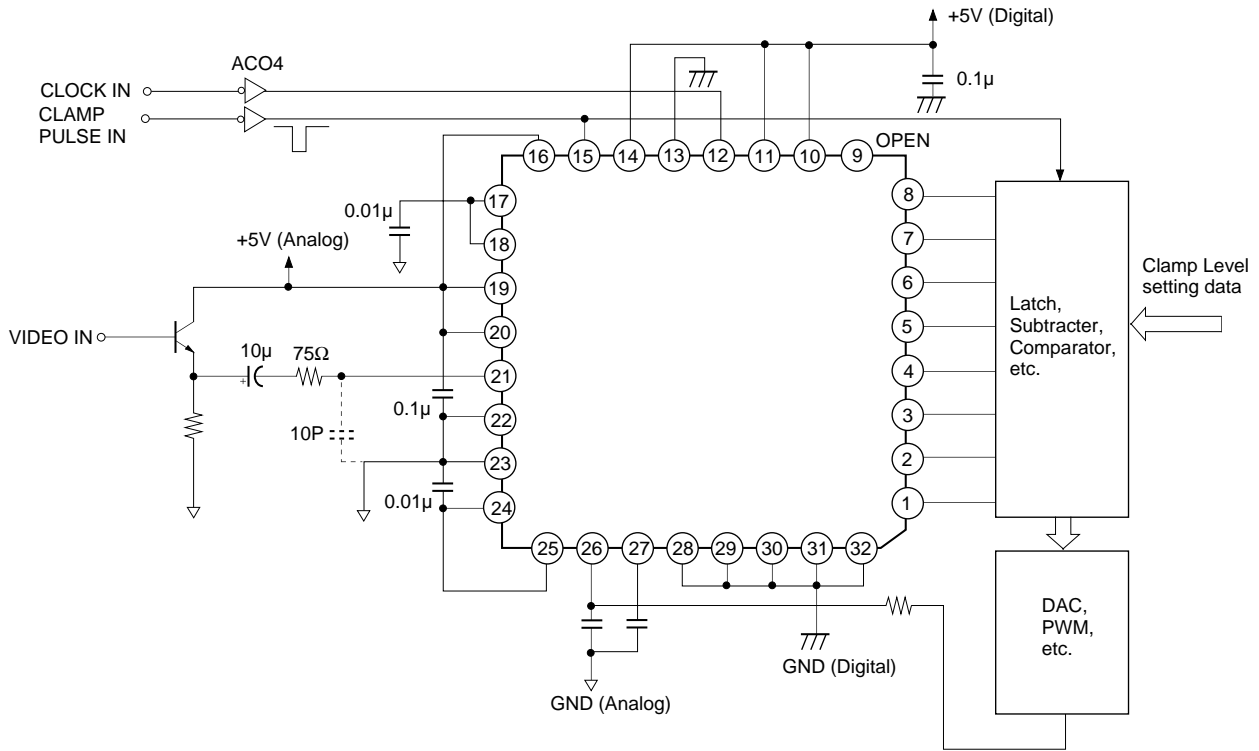
Application Circuit

(1) When clamp is used (self bias used)

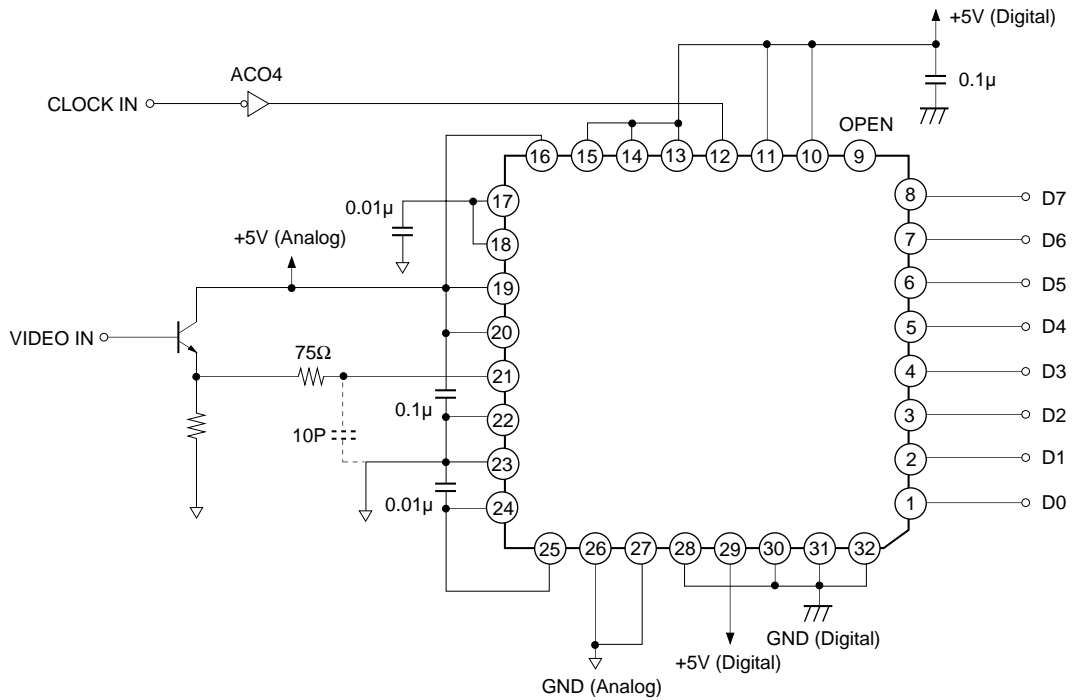


* The clamp pulse is latched by the sampling clock of ADC, but that is not necessary for basic clamp operation. However, slight small beat may be generated as vertical sag according to the relationship between the sampling frequency and the clamp pulse frequency. At such time, the latch circuit is effective in this case.

(2) Digital clamp (self bias used)

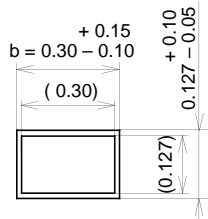
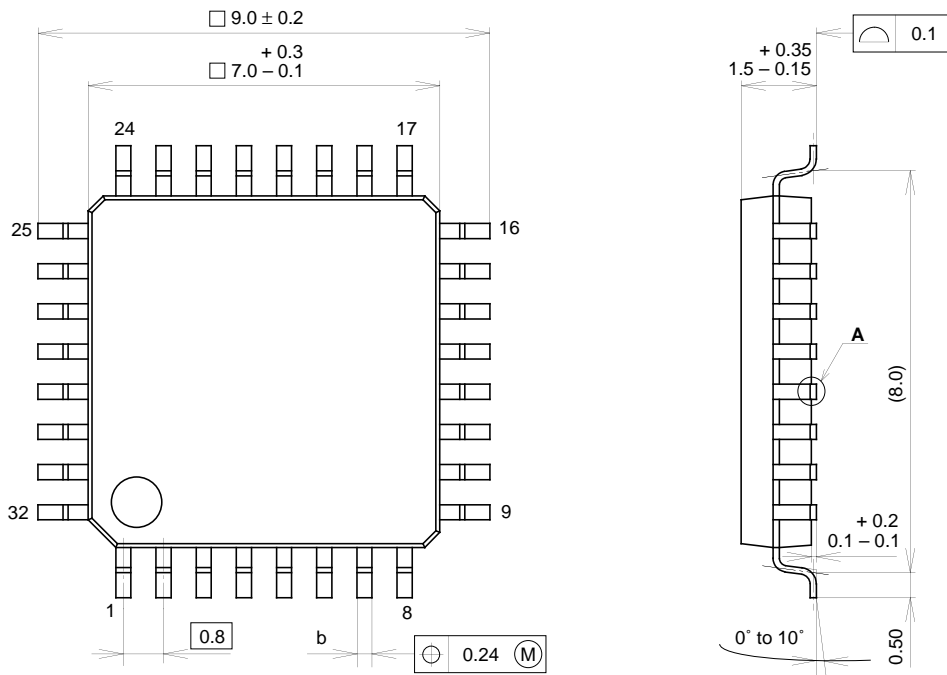


(3) When clamp is not used (self bias used)



Package Outline Unit : mm

32PIN QFP (PLASTIC)

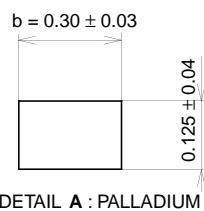
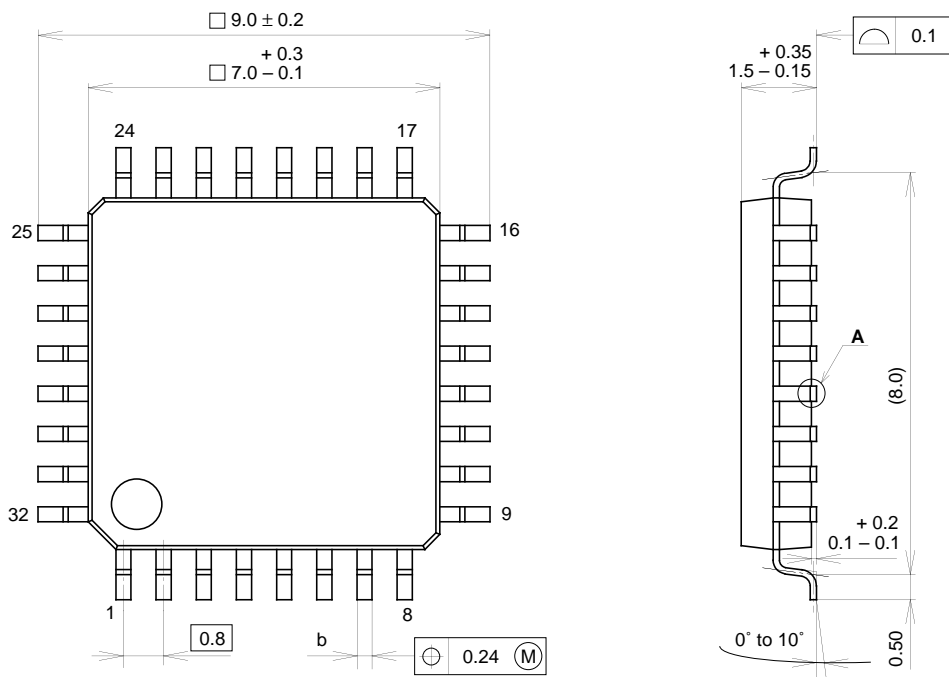


SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g