SONY

CXD1265R

CCD Camera Timing Generator

Description

The CXD1265R generates the timing pulses required by the CCD image sensors as well as signal processing circuits.

Features

- NTSC and PAL compatible
- Compatible with digital and analog camera systems
- Black-and-white mode compatible (EIA/CCIR compatible)
- Electronic shutter function
- H-driver
- Standby function
- Compatible with field/frame accumulation modes*1, *2

*1 Characteristics of CCD image sensor are guaranteed by field accumulation.

*2 Low speed shutter can not be used during frame accumulation mode.

Applications

CCD cameras

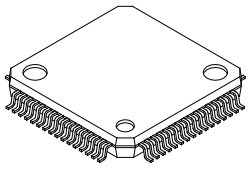
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX038BNA, ICX038BNB, ICX038BLA
ICX039BNA, ICX039BNB, ICX039BLA
ICX058AK, ICX058AKB, ICX058AL
ICX059AK, ICX059AKB, ICX059AL

64 pin LQFP (Plastic)



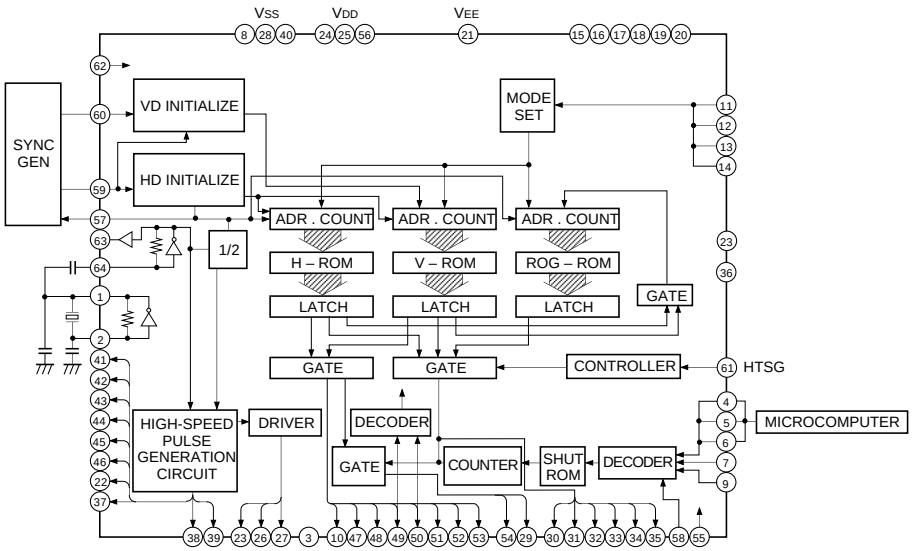
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	Vss – 0.5 to +7.0	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Supply voltage	V_{EE}	–5 to Vss	V
• Allowable power dissipation	P_D	500	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0 ± 0.25	V
• Operating temperature	Topr	–20 to +75	°C

Block Diagram



E92611C52-ST

Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation.
2	OSCI	I	Inverter input for oscillation.
3	EF	I	Not used. (With pull-up resistor)
4	ED0	I	Shutter speed setting. Strobe input for serial mode. (With pull-up resistor)
5	ED1	I	Shutter speed setting. Clock input for serial mode. (With pull-up resistor)
6	ED2	I	Shutter speed setting. Data input for serial mode. (With pull-up resistor)
7	SMD1	I	Shutter mode setting. (With pull-up resistor)
8	Vss	—	GND
9	SMD2	I	Shutter mode setting. (With pull-up resistor)
10	XVCT	O	Not used. (Open)
11	D1	I	Fix at Low in normal operation. (With pull-down resistor)
12	D2	I	Low: Color, High: Black-and-white. (With pull-down resistor)
13	D3	I	Low: Field readout, High: Frame readout*. (With pull-down resistor)
14	D4	I	Low: NTSC/EIA, High: PAL/CCIR. (With pull-down resistor)
15	A5	O	Not used. (Open)
16	A4	O	Not used. (Open)
17	A3	O	Not used. (Open)
18	A0	O	Not used. (Open)
19	A1	O	Not used. (Open)
20	A2	O	Not used. (Open)
21	V_{EE}	—	GND
22	RG	O	Reset gate pulse output.
23	NC	—	Not used. (Open)
24	V_{DD}	—	Power supply.
25	V_{DD}	—	Power supply for H1 and H2.
26	H1	O	Clock output for CCD horizontal register drive.
27	H2	O	Clock output for CCD horizontal register drive.
28	Vss	—	GND for H1 and H2.
29	XSUB	O	CCD discharge pulse output.
30	XV2	O	Clock output for CCD vertical register drive.
31	XV1	O	Clock output for CCD vertical register drive.
32	XSG1	O	CCD sensor charge readout pulse output.
33	XV3	O	Clock output for CCD vertical register drive.
34	XSG2	O	CCD sensor charge readout pulse output.
35	XV4	O	Clock output for CCD vertical register drive.

* Characteristics of CCD image sensor are guaranteed by field accumulation.

Pin No.	Symbol	I/O	Description
36	TEST2	I	Test input. Set at Low in normal operation.
37	MCK	O	NTSC: 910f_H, PAL: 908f_H. Clock output.
38	XSHP	O	Precharge level sample-and-hold pulse.
39	XSHD	O	Data sample-and-hold pulse.
40	Vss	—	GND
41	XSP1	O	Color separation sample-and-hold pulse. Halted for black-and-white mode.
42	XSP2	O	Color separation sample-and-hold pulse. Halted for black-and-white mode.
43	XSH1/ SHP	O	Switching sample-and-hold pulse/precharge level sample-and-hold pulse (black-and-white mode).
44	XSH2/ SHD	O	Switching sample-and-hold pulse/data sample-and-hold pulse (black-and-white mode).
45	XDL1	O	Delay line clock output. Halted for black-and-white mode.
46	XDL2	O	Delay line clock output. Halted for black-and-white mode.
47	BFG	O	Pulse output for chroma modulator in encoder. Halted for black-and-white mode.
48	CLP1	O	Clamp pulse output.
49	CLP2	I/O	Clamp pulse output. When GM is set at High, standby mode switching input.
50	CLP3	I/O	Clamp pulse output. When GM is set at High, standby mode switching input.
51	CLP4	O	Clamp pulse output.
52	PBLK	O	Blanking cleaning pulse output.
53	ID	O	Line identification output. Halted for black-and-white mode.
54	WEN	O	Write enable output for low-speed shutter operation.
55	GM	I	Low: Analog signal processing, High: Digital signal processing. (With pull-down resistor)
56	V_{DD}	—	Power supply.
57	CL	O	NTSC/EIA: 910f_H, PAL/CCIR: 908f_H. Clock output.
58	PS	I	Switching for electronic shutter speed input method. (With pull-up resistor) Low: Serial input, High: Parallel input.
59	HD	I	Horizontal synchronizing signal input.
60	VD	I	Vertical synchronizing signal input. (During Low, 9H for NTSC and 7.5H for PAL)
61	HTSG	I	Control input for XSG1 and XSG2. (With pull-up resistor) Low: XSG1, XSG2 halted, High: XSG1, XSG2 generated.
62	TEST	I	Test input. Set at Low in normal operation. (With pull-down resistor)
63	XCK	O	NTSC/EIA: 1820f_H, PAL/CCIR: 1816f_H. Clock output.
64	CK	I	NTSC/EIA: 1820f_H, PAL/CCIR: 1816f_H. Clock input.

Electrical Characteristics

DC Characteristics

(V_{DD} = 5V ± 0.25V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1 (Input pins other than those below)	V_{IH1}		0.7V_{DD}			V
	V_{IL1}				0.3V_{DD}	V
Input voltage 2 (Pins 59 and 60)	V_{IH2}		2.2			V
	V_{IL2}				0.8	V
Output voltage 1 (Output pins other than those below)	V_{OH1}	I_{OH} = –2mA	V_{DD} – 0.5			V
	V_{OL1}	I_{OL} = 4mA			0.4	V
Output voltage 2 (Pins 22, 37, 38, 39, 57, and 63)	V_{OH2}	I_{OH} = –4mA	V_{DD} – 0.5			V
	V_{OL2}	I_{OL} = 8mA			0.4	V
Output voltage 3 (Pins 26 and 27)	V_{OH3}	I_{OH} = –8mA	V_{DD} – 0.5			V
	V_{OL3}	I_{OL} = 8mA			0.4	V
Output voltage 4 (Pin 1)	V_{OH4}	I_{OH} = –1mA	V_{DD}/2			V
	V_{OL4}	I_{OL} = 1mA			V_{DD}/2	V
Feedback resistor	R_{FB}	V_{IN} = Vss or V_{DD}	500k	2M	5M	Ω
Pull-up resistor	R_{PU}	V_{IL} = 0V	40k	100k	250k	Ω
Pull-down resistor	R_{PD}	V_{IH} = V_{DD}	40k	100k	250k	Ω
Current consumption	I_{DD}	V_{DD} = 5V ICX058AK in normal operating state		74		mA

* Power consumption: 370mW typ., ICX058 load (in normal operating state)

I/O Pin Capacitances

(V_{DD} = V_I = 0V, f_M = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

Description of Operation

1. Mode Control

Symbol	Pin No.	L	H
GM*2	55	Analog signal processing	Digital signal processing
PS	58	Serial shutter speed setting	Parallel shutter speed setting
EF	3	Fix at High in normal operation	
HTSG	61	XSG1, 2 OFF	XSG1, 2 ON
D1	11	Fix at Low in normal operation	
D2*2	12	Color	Black-and-white
D3	13	Field readout	Frame readout*1
D4	14	NTSC/EIA	PAL/CCIR

*1 Characteristics of CCD image sensor are guaranteed by field accumulation.

*2 Operation with GM = High and D2 = High (black-and-white digital signal processing) cannot be used.

2. Changes in I/O Signals in Each Mode

Symbol	Pin No.	Analog color	Digital color 1	Digital color 2	Analog B/W
GM	55	L	H	H	L
D2	12	L	L	L	H
TEST2	36	L	L	H	L
XSP1	41	Color separation sample-and-hold pulse output	Halted at High	Color separation sample-and-hold pulse output	Halted at High
XSP2	42	Color separation sample-and-hold pulse output	Halted at High	Color separation sample-and-hold pulse output	Halted at High
XSH1	43	Switching sample-and-hold pulse output	Halted at Low	Switching sample-and-hold pulse output	Precharge level sample-and-hold pulse output
XSH2	44	Switching sample-and-hold pulse output	Halted at Low	Switching sample-and-hold pulse output	Data sample-and-hold pulse output
XDL1	45	Delay line clock	Halted at High	Halted at High	Halted at High
XDL2	46	Delay line clock	Halted at Low	Halted at Low	Halted at Low
BFG	47	Burst flag gate pulse output	Burst flag gate pulse output (normally not used)	Burst flag gate pulse output (normally not used)	Halted at Low
CLP2	49	Clamp pulse output	Standby control input Low: Standby High: Normal operation	Standby control input Low: Standby High: Normal operation	Clamp pulse output
CLP3	50	Clamp pulse output	Standby control* Low: All circuits halted for standby mode High: Only CL output for standby mode	Standby control* Low: All circuits halted for standby mode High: Only CL output for standby mode	Clamp pulse output (phase change)
ID	53	Line identification output	Line identification output	Line identification output	Halted at Low

* When CLP2 = High, normal operation occurs regardless of whether CLP3 is high or low.
(Mode combinations other than those shown above cannot be used.)

Note) In the standby mode described above, XCK, XSG1, XSG2, XV1, XV2, XV3, XV4, XSUB, H1, H2, RG, XSHD, XSHP, XSP1, XSP2, XSH1, XSH2, XDL1, and XDL2 pins are halted at Low. MCK, CLP1, CLP4, PBLK, ID, XVCT, WEN, BFG, A0, A1, A2, A3, A4, and A5 pins are halted at the state just before standby.

3. Electronic Shutter

<Shutter Modes>

SMD1	SMD2	
L	L	Flickerless: Eliminates fluorescent frequency-induced flicker.
L	H	High-speed shutter: Shutter speed faster than 1/60 (NTSC), 1/50 (PAL)
H	L	Low-speed shutter: Shutter speed slower than 1/60 (NTSC), 1/50 (PAL)
H	H	No shutter operation

<Shutter Mode and Speed Setting Method>

PS = High: Parallel input; set by ED0 to ED2, SMD1, and SMD2.

PS = Low: Serial input; set by inputting ED0 (strobe), ED1 (clock), and ED2 (data) to each pin.

3-1. Parallel input (PS = H)

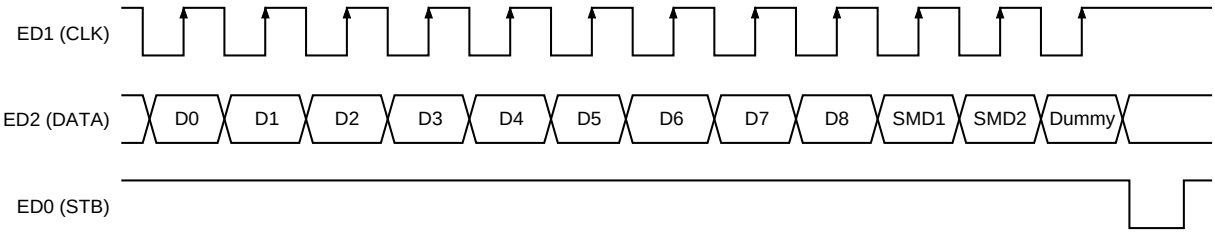
Shutter Speed Compatibility Chart

Mode	NTSC/PAL	SMD1	SMD2	ED0	ED1	ED2	Shutter speed
OFF	X	H	H	X	X	X	Shutter off
Flickerless	NTSC	L	L	X	X	X	1/100 (S)
	PAL	L	L	X	X	X	1/120 (S)
High-speed shutter	NTSC	L	H	H	H	H	1/60 (S)
	PAL	L	H	H	H	H	1/50 (S)
	X	L	H	L	H	H	1/125 (S)
	X	L	H	H	L	H	1/250 (S)
	X	L	H	L	L	H	1/500 (S)
	X	L	H	H	H	L	1/1000 (S)
	X	L	H	L	H	L	1/2000 (S)
	X	L	H	H	L	L	1/4000 (S)
	X	L	H	L	L	L	1/10000 (S)
Low-speed shutter*	X	H	L	H	H	H	2FLD
	X	H	L	L	H	H	4FLD
	X	H	L	H	L	H	6FLD
	X	H	L	L	L	H	8FLD
	X	H	L	H	H	L	10FLD
	X	H	L	L	H	L	12FLD
	X	H	L	H	L	L	14FLD
	X	H	L	L	L	L	16FLD

* During frame accumulation mode, low speed shutter data set to ED0 to ED2 are all invalid. Shutter speed is 1/30s for NTSC; 1/25s for PAL.

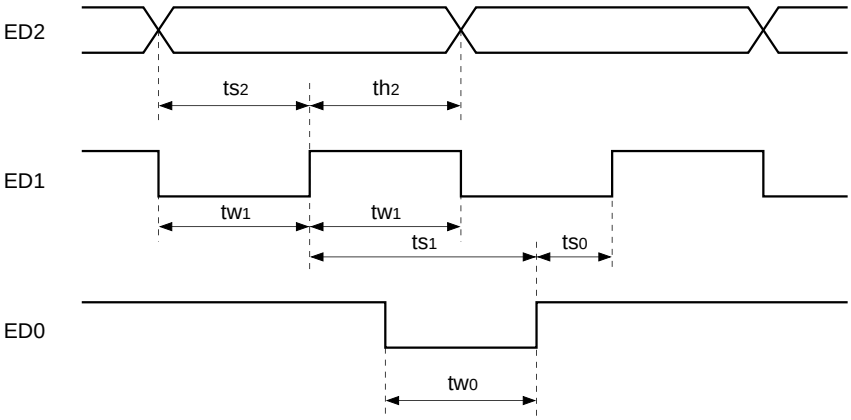
3-2. serial input (PS=L)

For serial input (PS = L), SMD1 and SMD2 bits within ED2 (DATA) take priority over SMD1 (Pin 7) and SMD2 (Pin 9) pins as SMD1 and SMD2 (shutter mode control).
In this case, control by SMD1 and SMD2 pins is invalid.



ED2 data is latched to the register at the rise of ED1, and transferred to the within during the Low period of ED0.

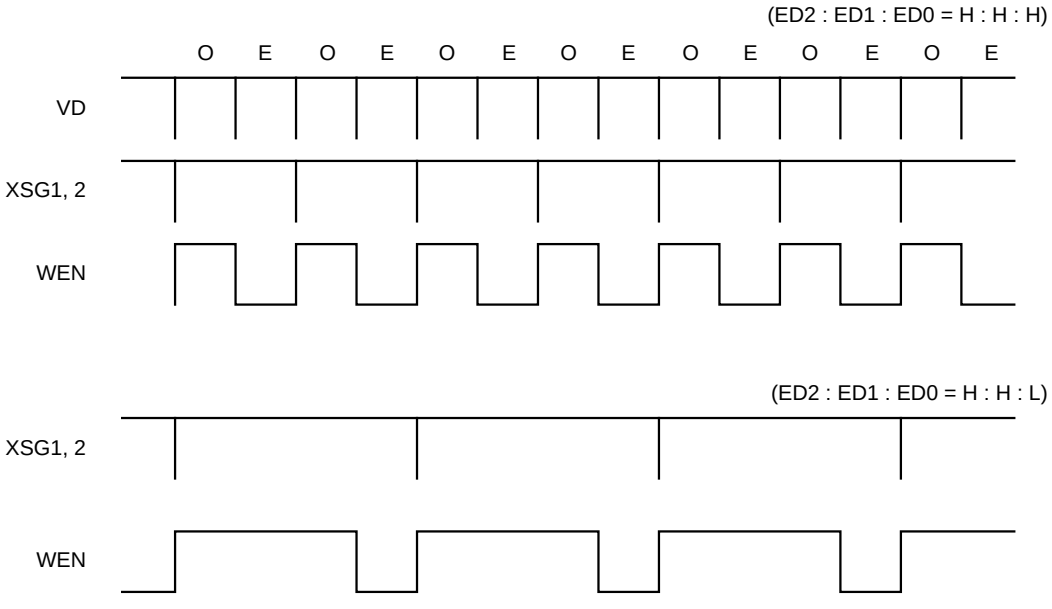
AC Characteristics



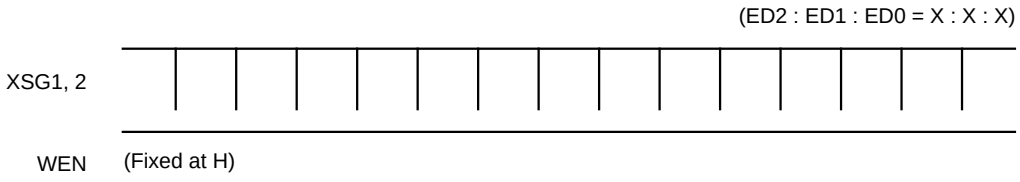
Symbol		Min.	Max.
t_{S2}	ED2 set-up time, activated by the rising edge of ED1	20ns	—
t_{h2}	ED2 hold time, activated by the rising edge of ED1	20ns	—
t_{S1}	ED1 rising set-up time, activated by the rising edge of ED0	20ns	—
t_{W0}	ED0 pulse width	20ns	50µs
t_{S0}	ED0 rising set-up time, activated by the rising edge of ED1	20ns	—
t_{W1}	ED1 pulse width (serial input)	20ns	—

3-4. Low-speed shutter timing chart

(During field accumulation mode)



(During frame accumulation mode)



3-5. Shutter speed calculation formula

1. High-speed shutter

- NTSC (L_{16} = load value)

  $T = [262_{10} – (1FF_{16} – L_{16})] \times 63.56\mu s + 34.9\mu s$

- PAL (L_{16}= load value)

  $T = [312_{10} – (1FF_{16} – L_{16})] \times 64.00\mu s + 35.0\mu s$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
$0FA_{16}$	1/10000	1/10156	$0C8_{16}$	1/10000	1/10101
$0FC_{16}$	1/4000	1/4433	$0CA_{16}$	1/4000	1/4405
100_{16}	1/2000	1/2084	$0CE_{16}$	1/2000	1/2070
108_{16}	1/1000	1/1012	$0D6_{16}$	1/1000	1/1005
118_{16}	1/500	1/499	$0E6_{16}$	1/500	1/495
137_{16}	1/250	1/252	105_{16}	1/250	1/250
176_{16}	1/125	1/125	143_{16}	1/125	1/125
196_{16}	1/100	1/100	149_{16}	1/120	1/120

2. Low-speed shutter (Valid during field accumulation mode only)

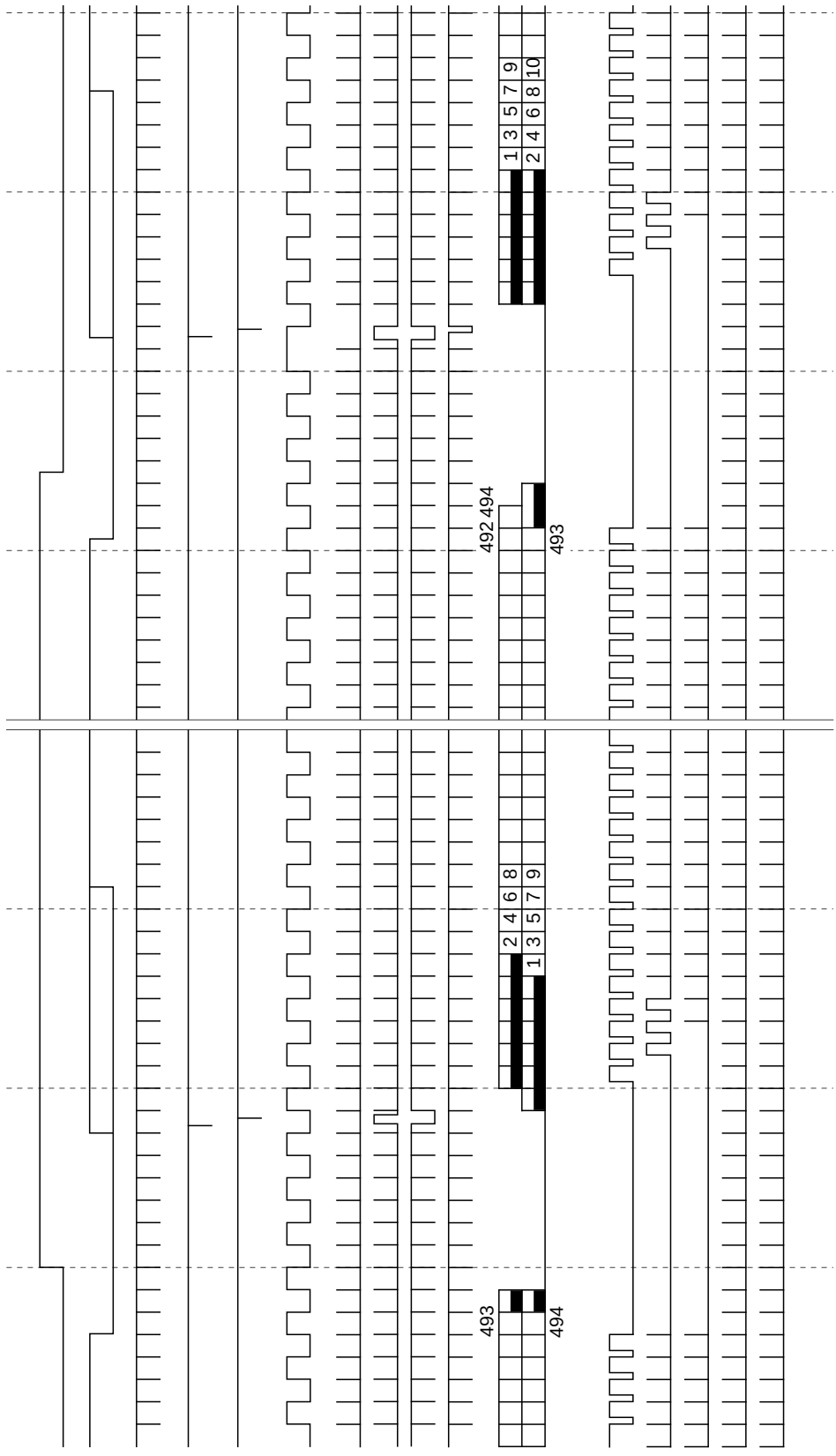
Shutter speed calculation formula

$N = 2 \times (1FF_{16} – L_{16})$ FLD

However, "FF" cannot be used as the load value.

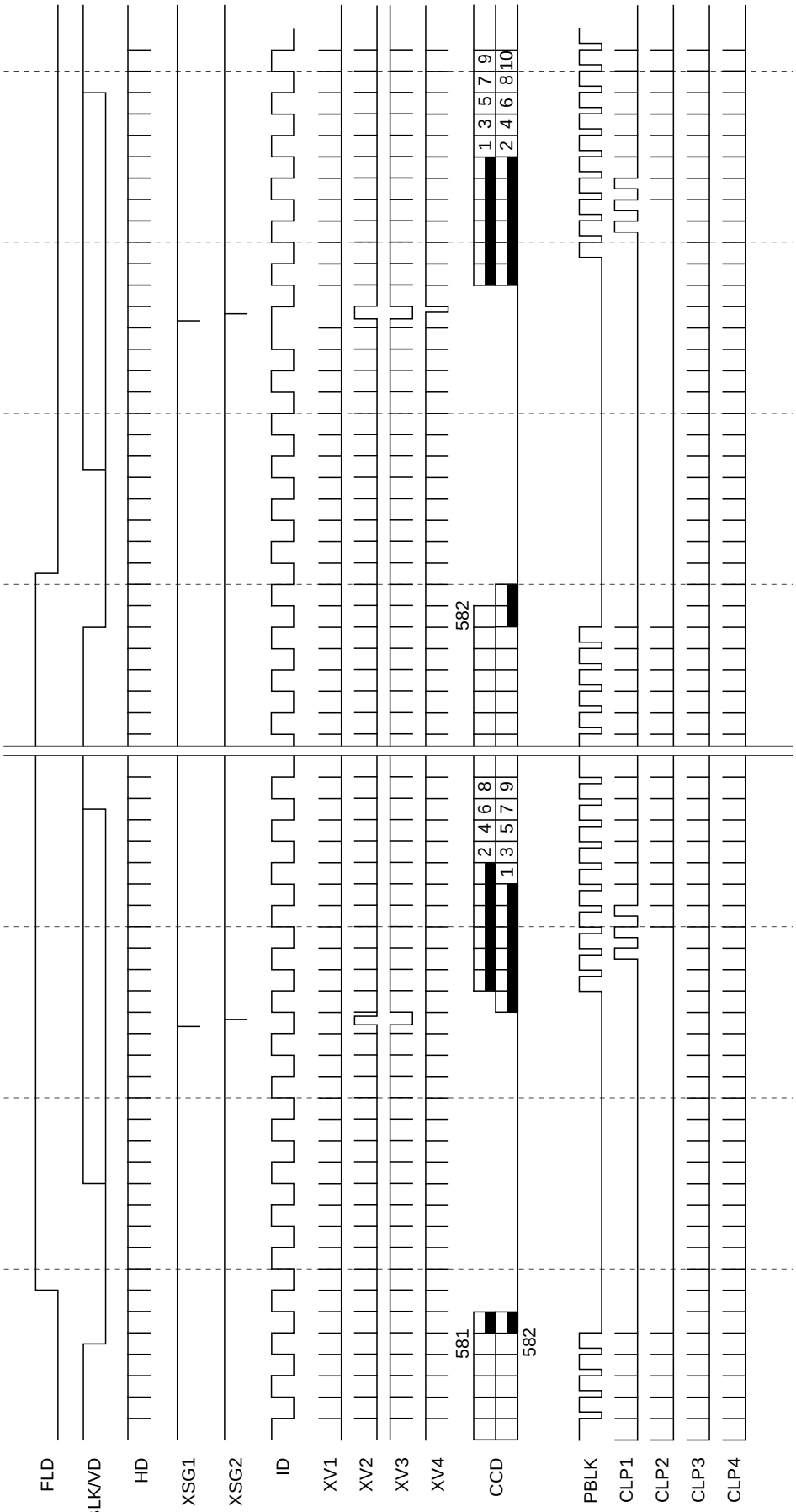
Load value	Shutter speed (FLD)
$1FE_{16}$	2
$1FD_{16}$	4
: :	: :
101_{16}	508
100_{16}	510

Timing Chart (1)
NTSC vertical direction



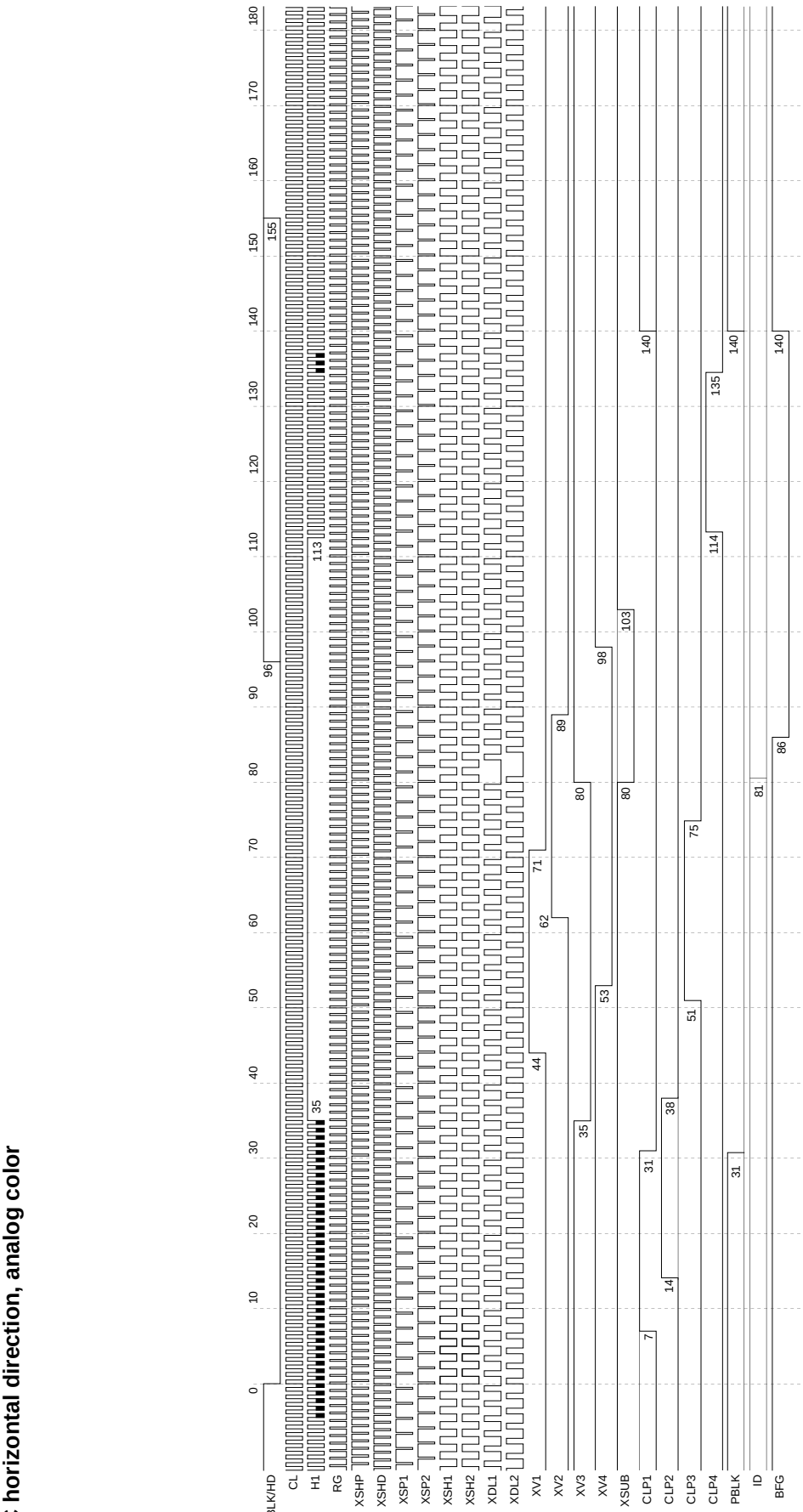
However, ID is halted for black-and-white mode

Timing Chart (2)
PAL vertical direction



However, ID is halted for black-and-white mode

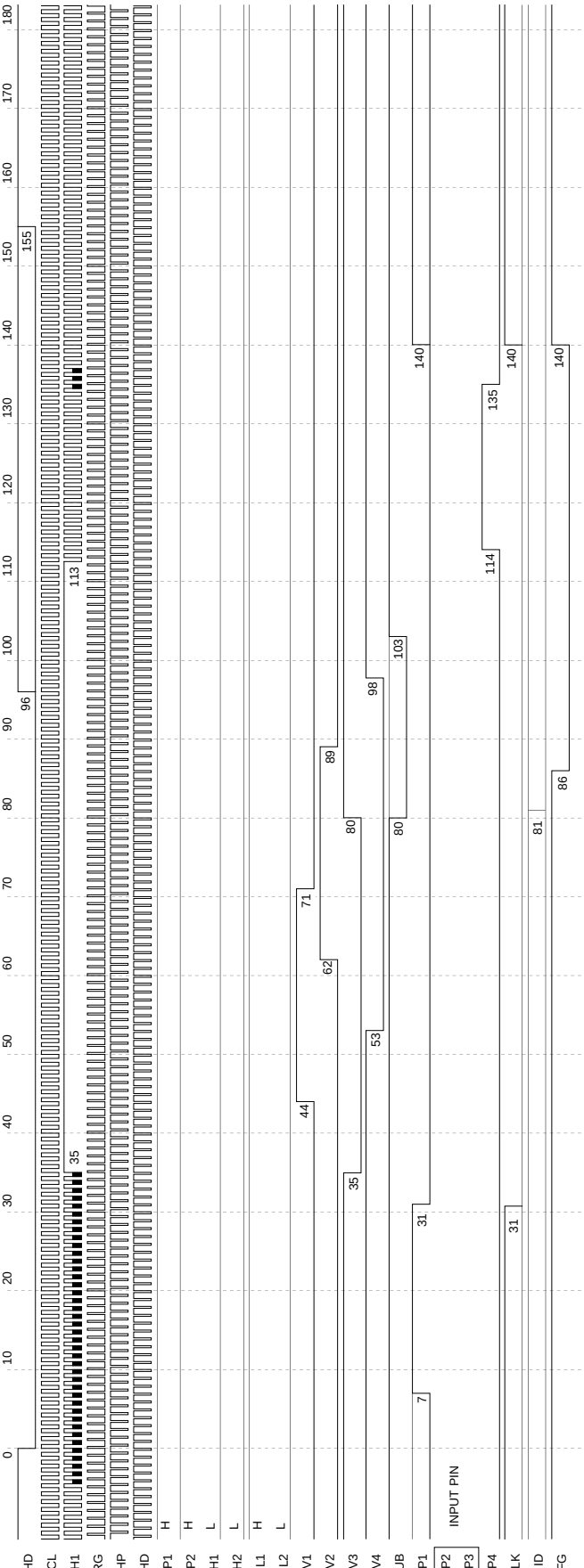
Timing Chart (3)
NTSC horizontal direction, analog color



Black painted portions indicate the optical black output timing of CCD.

(GM = L, D2=L, TEST2 = L)

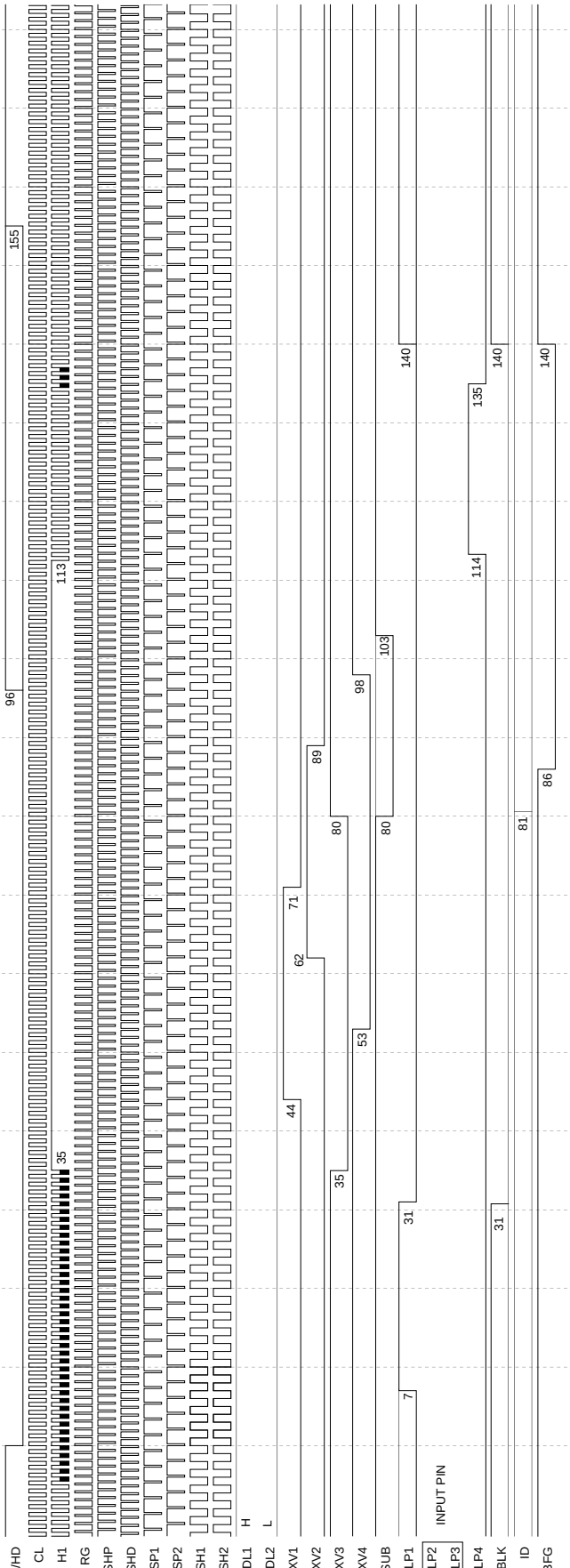
Timing Chart (4)
NTSC horizontal direction, digital color 1



Black painted portions indicate the optical black output timing of CCD.

(GM = H, D2 = L, TEST2 = L)

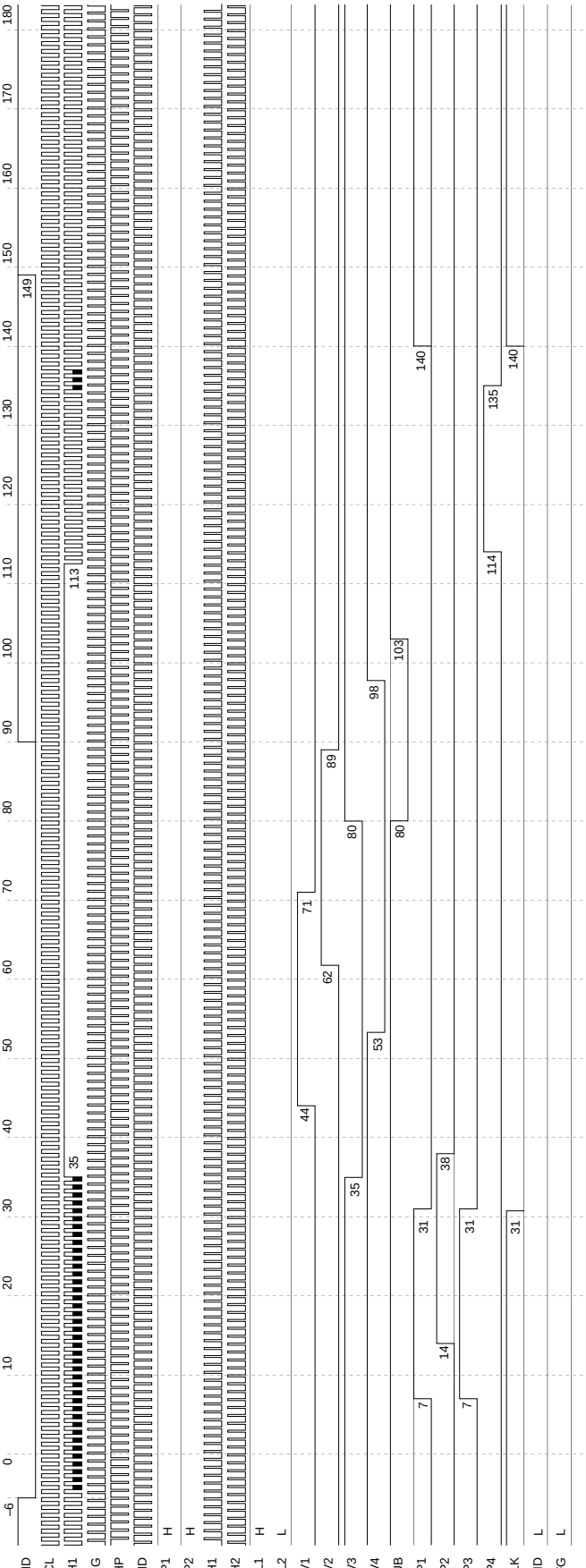
Timing Chart (5)
NTSC horizontal direction, digital color 2



Black painted portions indicate the optical black output timing of CCD.

(GM = H, D2 = L, TEST2 = H)

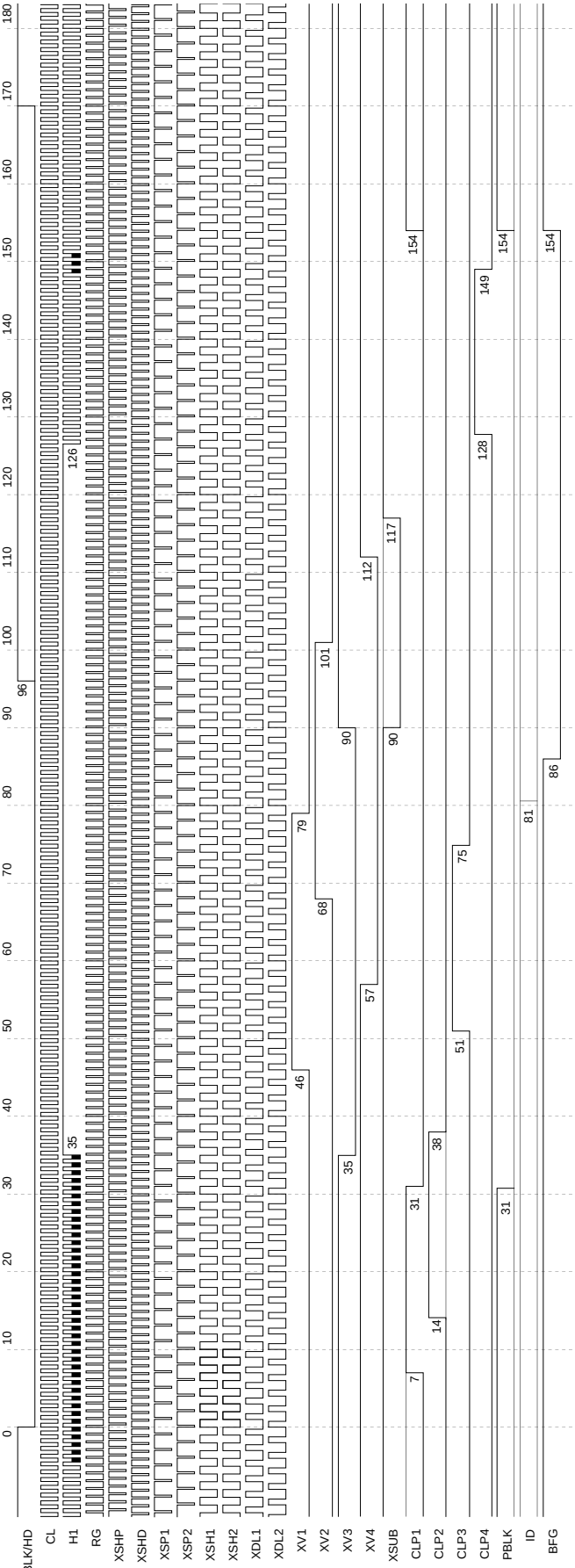
Timing Chart (6)
EIA horizontal direction, analog black-and-white



Black painted portions indicate the optical black output timing of CCD.

(GM = L, D2 = H, TEST2 = L)

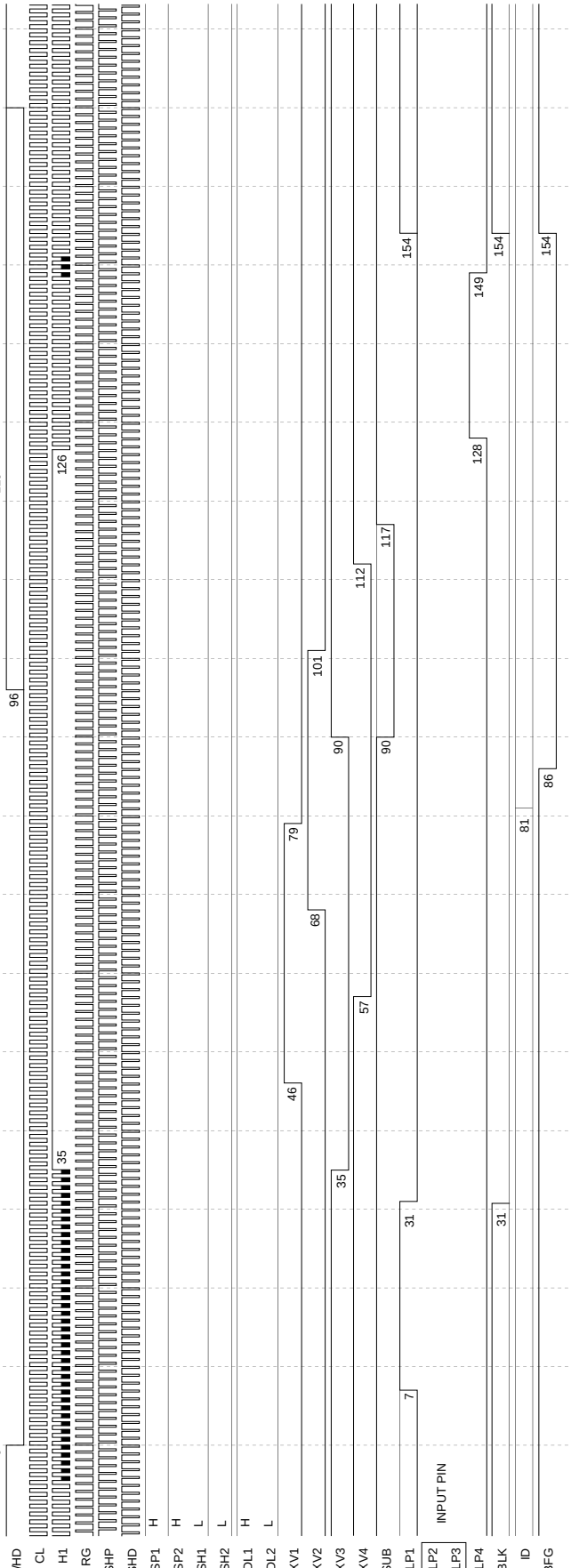
Timing Chart (7)
PAL horizontal direction, analog color



Black painted portions indicate the optical black output timing of CCD.

(GM = L, D2 = L, TEST2 = L)

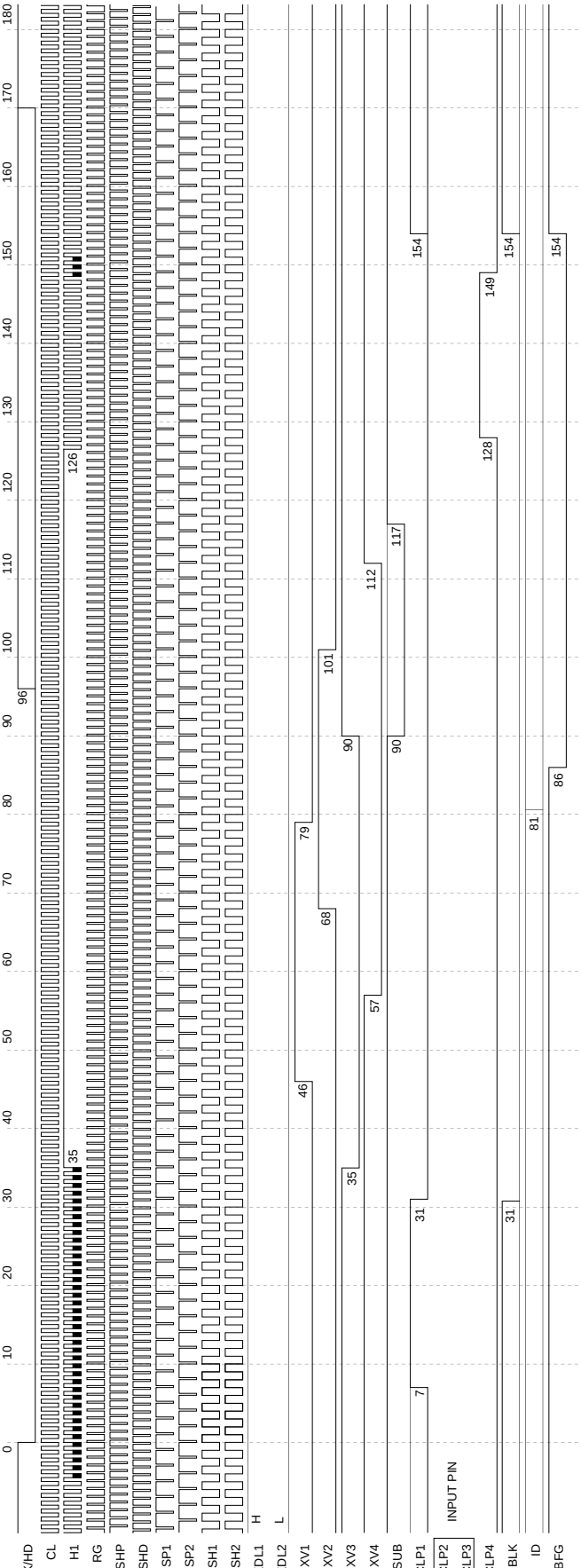
Timing Chart (8)
PAL horizontal direction, digital color 1



Black painted portions indicate the optical black output timing of CCD.

(GM = H, D2 = L, TEST2 = L)

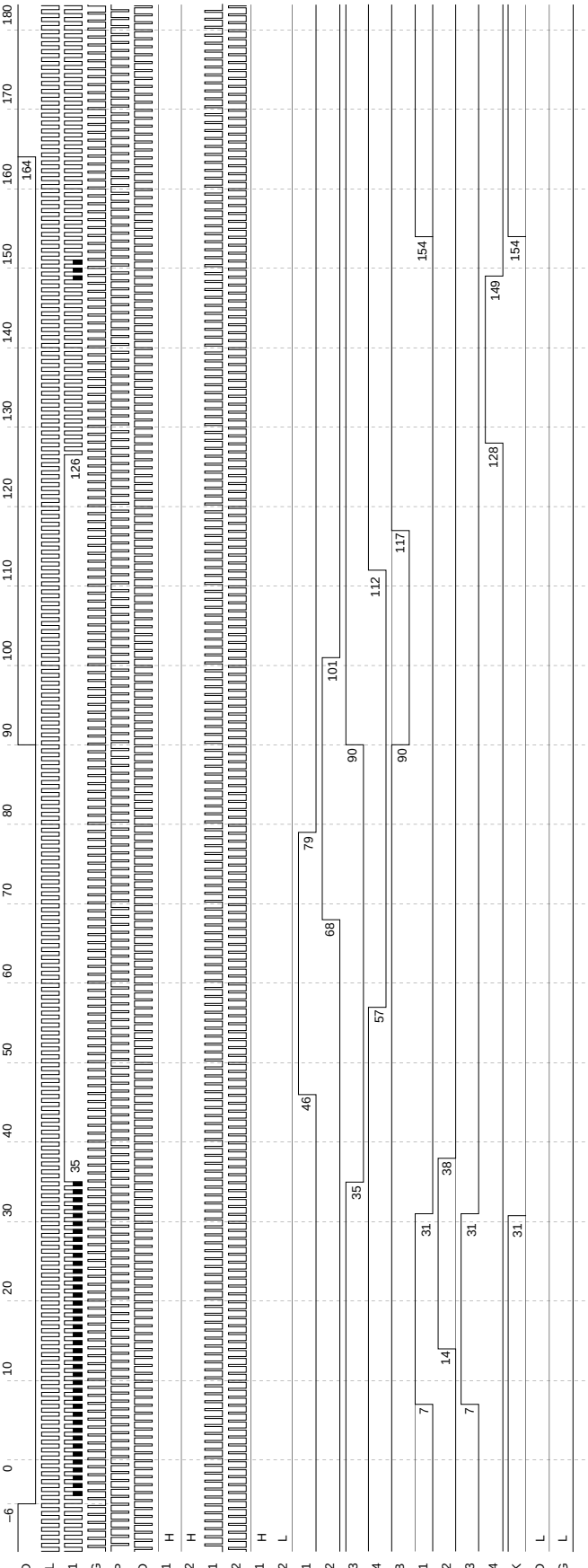
Timing Chart (9)
PAL horizontal direction, digital color 2



Black painted portions indicate the optical black output timing of CCD.

(GM = H, D2 = L, TEST2 = H)

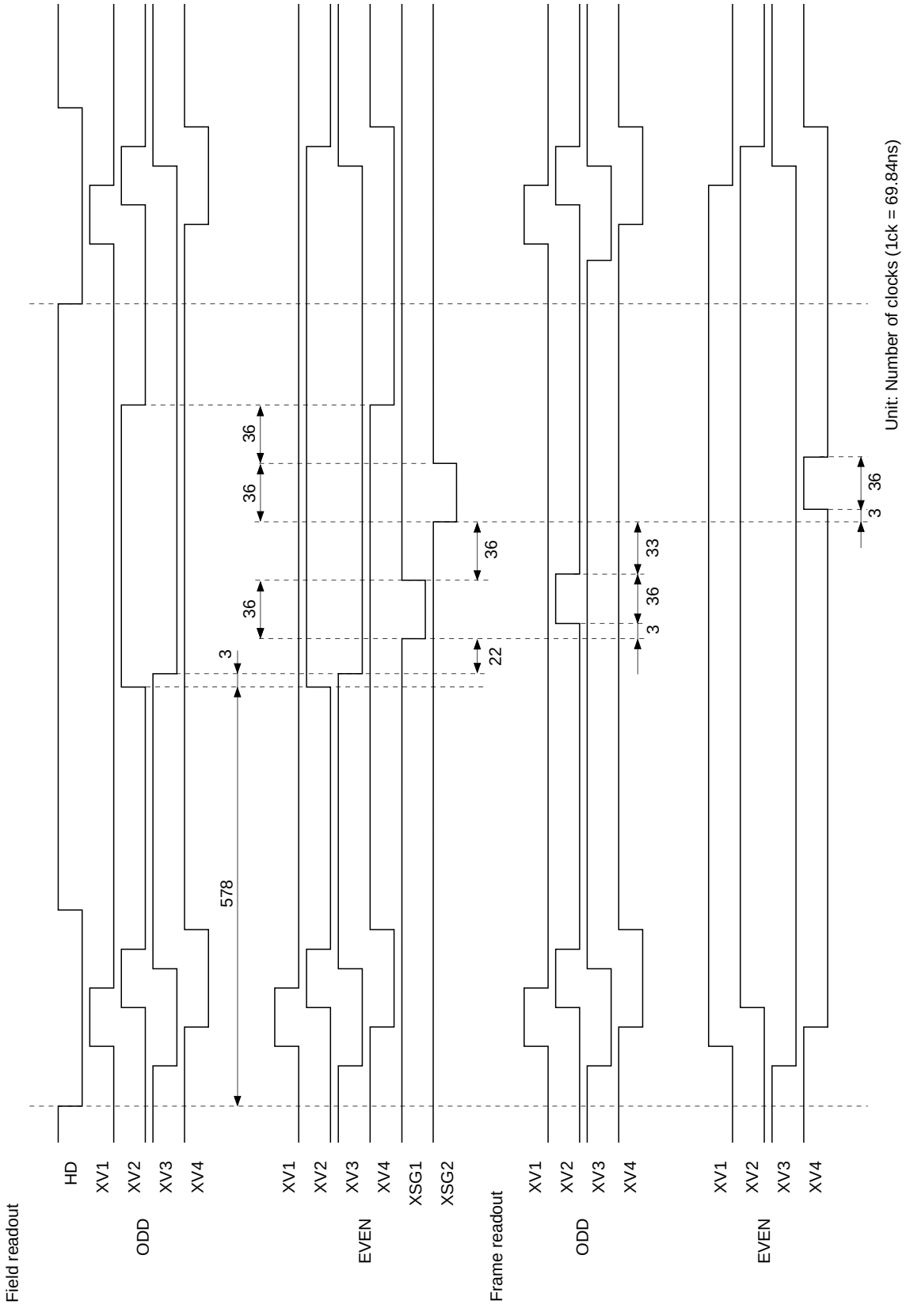
Timing Chart (10)
CCIR horizontal direction, analog black-and-white



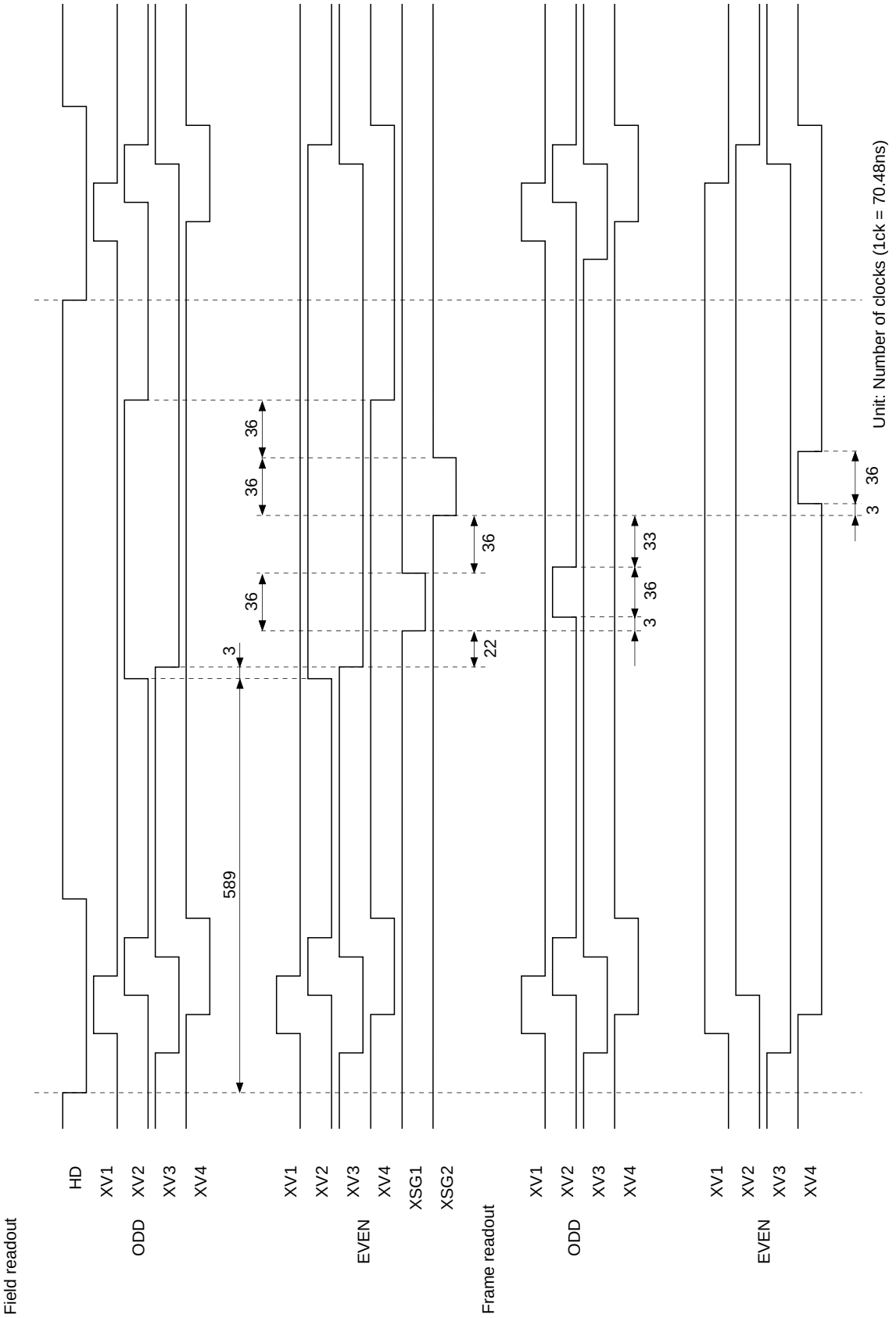
Black painted portions indicate the optical black output timing of CCD.

(GM = L, D2 = H, TEST2 = L)

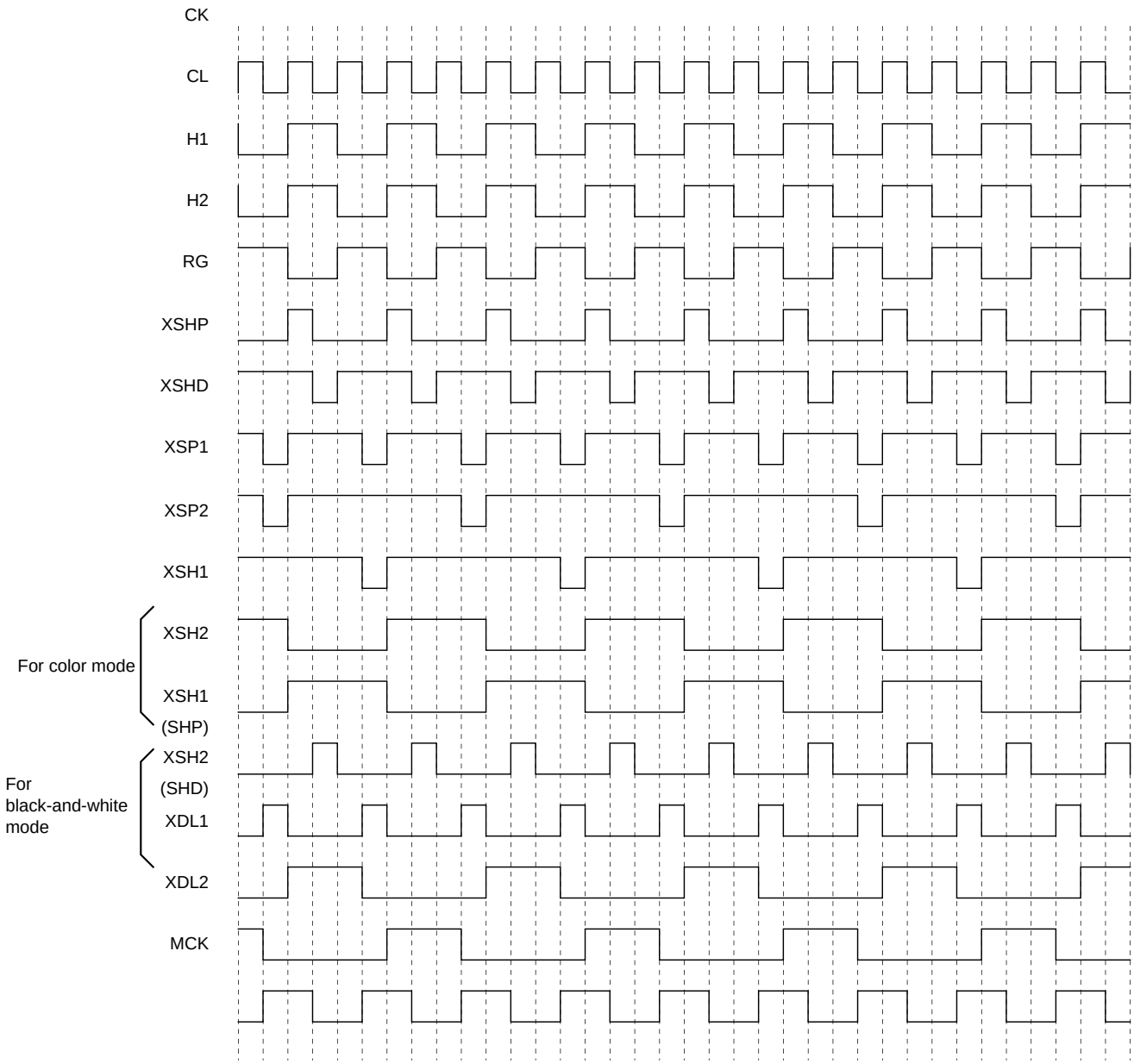
4-1. Timing Chart of Readout (NTSC/EIA)



4-2. Timing Chart of Readout (PAL/CCIR)



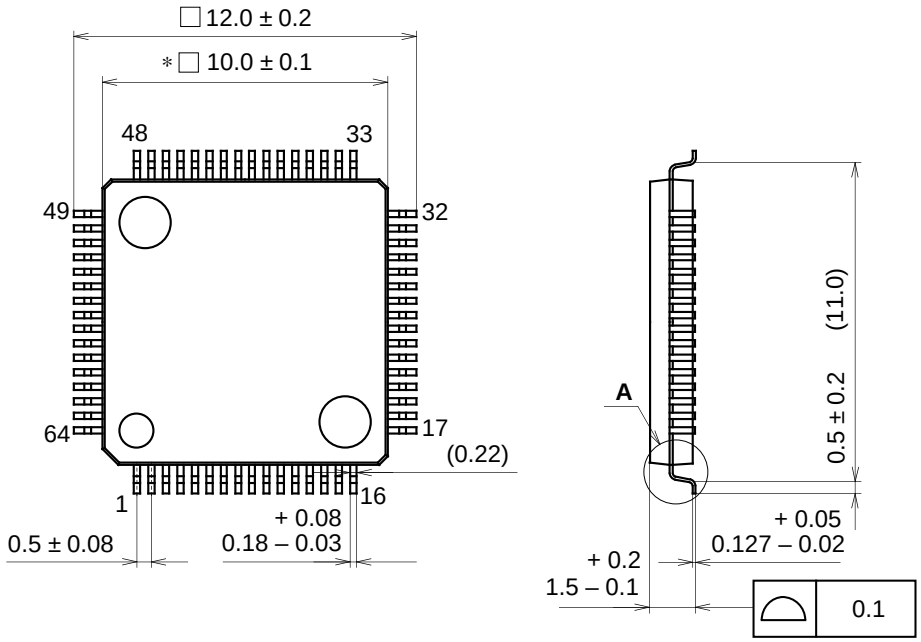
5. High-speed Clock Timing Chart

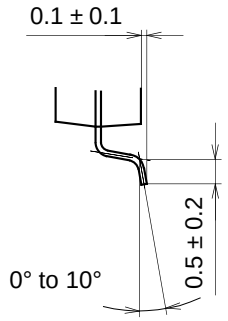


* For black and white mode, XSP1, XSP2, XDL1, and XDL2 are halted.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	∗QFP064-P-1010-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g