SONY

CXD1273R

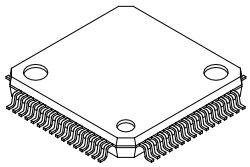
Cellular Phone Filter LSI with On-Chip Compandor

Description

The CXD1273R is a filter LSI for cellular phones. The successor to the CXD1272Q/R, this device enables low voltage (3V) operation, and the addition of an attenuator for digital control provides for easy adjustment.

When used with the control signal processor CXD1270Q/R IC, a modem can be implemented.

64 pin LQFP (Plastic)



Features

- On-chip compandor
- Ultra-low current consumption
  Operating current: 5.6mA,
  Power standby: 0.7mA (For standard 3V operation)
- Power save function
- 4-bit attenuation controller facilitates gain adjustment over required range.
- Supports 4 standards.
- AMPS, DOC, TACS, and N-TACS
- Adoption of SCF technology provides stable characteristics.
- On-chip 8-level, 3 dB-step electronic volume

Functions

- Compandor
- Filtering of received data
- PLL lock detection for received SAT
- Filtering and addition performed on transmitted data
- Audio signal filtering for received/transmitted signals
- Gain controlled through serial data input
- Volume controller (Dual system)

Absolute Maximum Ratings

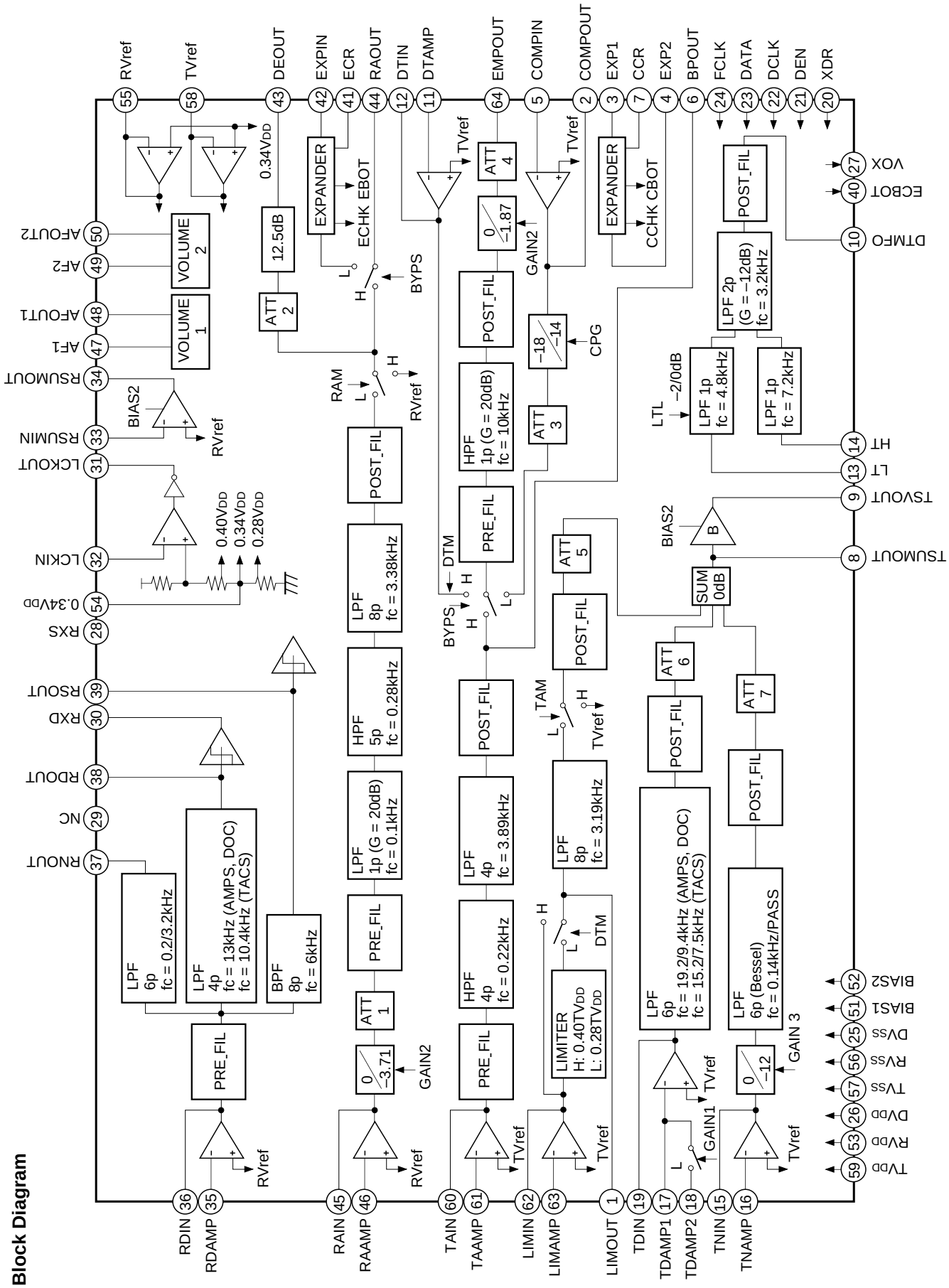
• Supply voltage	V_{DD}	–0.5 to +7.0	V
• Input voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V
• Output voltage	V_{OUT}	–0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	2.85 to 3.15	V
		4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

E94845-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	LIMOUT	O	TX audio limiter output.
2	COMPOUT	O	Output from compressor.
3	EXP1	I	Expander input for compressor structure.
4	EXP2	O	Expander output for compressor structure.
5	COMPIN	I	Gain control amplifier input for compressor input.
6	BPOUT	O	TX audio band-pass filter output.
7	CCR	O	Attack recovery time setting of compressor. Satisfy each standard by connecting a 0.1µF capacitor between this pin and TV_{SS}.
8	TSUMOUT	O	TX system summing amplifier output.
9	TSVOUT	O	Bufferd output for TX system summing amplifier.
10	DTMFO	O	DTMF filter output.
11	DTAMP	I	Gain control amplifier input for DTMF input.
12	DTIN	O	Gain control amplifier output for DTMF input.
13	LT	I	DTMF Low tone input.
14	HT	I	DTMF High tone input.
15	TNIN	O	Gain control amplifier output for inputting TX data (N-TACS standard).
16	TNAMP	I	Gain control amplifier input for inputting TX data (N-TACS standard).
17	TDAMP1	I	Input for TX SAT.
18	TDAMP2	I	Input for TX Wide Band Data and ST. Gain is controlled by control data "GAIN1".
19	TDIN	O	Summing amplifier output for inputting TX Wide Band Data, ST, and SAT.
20	XDR	I	Control data reset. Active at Low.
21	DEN	I	Load signal input for inputting serial data to data buffer.
22	DCLK	I	Clock signal input for serial data input.
23	DATA	I	8-bit serial data input.
24	FCLK	I	Clock input for filter.
25	DV_{SS}	—	Exclusive GND for digital circuits.
26	DV_{DD}	—	Exclusive power supply for digital circuits.
27	VOX	O	TX audio signal detection output. (Output with no signal: High)
28	RXS	O	Comparator output for RX SAT.
29	NC	—	Don't connect.
30	RXD	O	Comparator output for RX Wide Band Data.
31	LCKOUT	O	Comparator output for PLL lock detection of RX SAT.
32	LCKIN	I	Comparator input for PLL lock detection of RX SAT.
33	RSUMIN	I	Summing amplifier input for RX system.
34	RSUMOUT	O	Summing amplifier output for RX system.
35	RDAMP	I	Gain controller amplifier input for inputting RX Wide Band Data and SAT.

Pin No.	Symbol	I/O	Description
36	RDIN	O	Gain controller amplifier output for inputting RX Wide Band Data and SAT.
37	RNOUT	O	Filter output for RX data (N-TACS standard).
38	RDOUT	O	Filter output for RX Wide Band Data. Used as a prefilter for RX audio data.
39	RSOUT	O	Filter output for RX SAT.
40	ECBOT	O	Compandor reference voltage output. (Test pin)
41	ECR	O	Attack/recovery time setting of expander. Satisfy each standard by connecting a 0.1µF capacitor between this pin and RVss.
42	EXPIN	I	Expander input.
43	DEOUT	O	RX audio filter output.
44	RAOUT	O	RX audio filter output. (BYPS: High) Internal expander output. (BYPS: Low)
45	RAIN	O	Gain control amplifier output for RX audio input.
46	RAAMP	I	Gain control amplifier input for RX audio input.
47	AF1	I	Volume 1 input.
48	AFOUT1	O	Volume 1 output.
49	AF2	I	Volume 2 input.
50	AFOUT2	O	Volume 2 output.
51	BIAS1	I	Determines bias current of internal operation amplifier. Normally, connects a 100kΩ resistor between this pin and RV_{DD}.
52	BIAS2	I	Determines bias current of RX summing amplifier, TSVOUT buffering amplifier. Normally, connects a 51kΩ between this pin and RV_{DD}.
53	RV_{DD}	—	Exclusive power supply for RX system.
54	$0.34V_{DD}$	I	Reference voltage input for operational amplifier. (0.34 times supply voltage) Normally, connects a 1µF capacitor between this pin and RVss.
55	RVref	O	Reference voltage output for RX processing system operational amplifier. (0.34 times supply voltage) Normally, connects a 1µF capacitor between this pin and RVss.
56	RV_{SS}	—	Exclusive GND for RX system.
57	TV_{SS}	—	Exclusive GND for TX system.
58	TVref	O	Reference voltage output for TX processing system operational amplifier. (0.34 times supply voltage) Normally, a 1µF capacitor is connected between this pin and TVss.
59	TV_{DD}	—	Exclusive power supply for TX system.
60	TAIN	O	Gain control amplifier output for TX audio input.
61	TAAMP	I	Gain control amplifier input for TX audio input.
62	LIMIN	O	Gain control amplifier output for limiter input.
63	LIMAMP	I	Gain control amplifier input for limiter input.
64	EMPOUT	O	Emphasis output for TX audio.

Electrical Characteristics (V_{DD} = 3V ± 5%, Ta = –20 to +75°C)

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Supply current 1 (N-TACS standard)	I_{DD1}	RV_{DD} TV_{DD} DV_{DD} Total	STD = "L" STN = "L" V1ST = V2ST = "L" BIAS1 = 100kΩ BIAS2 = 51kΩ	—	5.6	7.3	mA
Supply current 2 (Standards other than N-TACS)	I_{DD2}	RV_{DD} TV_{DD} DV_{DD} Total	STD = "L" STN = "H" V1ST = V2ST = "L" BIAS1 = 100kΩ BIAS2 = 51kΩ	—	5.5	7.2	mA
Supply current 3 (In standby status, excluding volume)	I_{STB1}	RV_{DD} TV_{DD} DV_{DD} Total	STD = "H" STN = "H" V1ST = V2ST = "L" BIAS1 = 100kΩ BIAS2 = 51kΩ	—	1.1	1.5	mA
Supply current 4 (All in standby status)	I_{STB2}	RV_{DD} TV_{DD} DV_{DD} Total	STD = "H" STN = "H" V1ST = V2ST = "H" BIAS1 = 100kΩ BIAS2 = 51kΩ	—	0.7	1.0	mA
Digital Low input voltage	V_{IL}	FCLK, DATA, DCLK, DEN, XDR	—	—	—	$0.3V_{DD}$	V
Digital High input voltage	V_{IH}	FCLK, DATA, DCLK, DEN, XDR	—	$0.7V_{DD}$	—	—	V
Digital Low input current	I_{IL}	FCLK, DATA, DCLK, DEN, XDR	V_{IN} = GND	–10	—	10	µA
Digital High input current	I_{IH}	FCLK, DATA, DCLK, DEN, XDR	$V_{IN} = V_{DD}$	–10	—	10	µA
Digital Low output voltage	V_{OL}	RXD, RXS, ECBOT, LCKOUT	I_{OL} = 0.3mA	—	—	0.4	V
Digital High output voltage	V_{OH}	RXD, RXS, ECBOT, LCKOUT	I_{OH} = –0.3mA	V_{DD} – 0.8	—	—	V
Analog input voltage range	V_{LA}	RDAMP, RAAMP, TAAMP, LIMAMP, TDAMP1, TDAMP2, TNAMP, DTMFI, RSUMIN, AF1, AF2	BIAS1 = 100kΩ	—	—	1	Vp-p
Analog input resistance	R_I	AF1, AF2	Input pin – $0.34V_{DD}$	60	100	140	kΩ
Analog switch ON resistance	R_{SW}	TDAMP2, BPOUT, RAOUT	Input pin – $0.34V_{DD}$	—	0.8	2	kΩ
Analog output load resistance 1	R_{L1}	TSVOUT, RSUMOUT	Output pin – $0.34V_{DD}$ BIAS2 = 51kΩ	2	—	—	kΩ
Analog output load resistance 2	R_{L2}	DTMFO, BPOUT, EMPOUT, RAOUT, DEOUT, AFOUT1, AFOUT2	Output pin – $0.34V_{DD}$ BIAS1 = 100kΩ	10	—	—	kΩ
Analog output load resistance 3	R_{L3}	RDIN, RAIN, TAIN, LIMIN, TDIN, TNIN, DTIN	Output pin – $0.34V_{DD}$ BIAS1 = 100kΩ	100	—	—	kΩ

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Analog output voltage range 1	V_{OA1}	TSVOUT, RSUMOUT	BIAS2 = 51kΩ Load resistance = 2kΩ	—	—	0.6	Vp-p
Analog output voltage range 2	V_{OA2}	DTMF, BPOUT, EMPOUT, RAOUT, DEOUT	BIAS1 = 100kΩ Load resistance = 10kΩ	—	—	0.4	Vp-p
Analog output voltage range 3	V_{OA3}	AFOUT1, AFOUT2	BIAS1 = 100kΩ Load resistance = 10kΩ	—	—	1	Vp-p
Limiter Low voltage	V_{LL}	LIMOUT	DTM = "L"	$0.34V_{DD}$ – 0.066 V_{DD}	$0.34V_{DD}$ – 0.06 V_{DD}	$0.34V_{DD}$ – 0.054 V_{DD}	V
Limiter High voltage	V_{LH}	LIMOUT	DTM = "L"	$0.34V_{DD}$ + 0.054 V_{DD}	$0.34V_{DD}$ + 0.06 V_{DD}	$0.34V_{DD}$ + 0.066 V_{DD}	V
Electronicvolume step	V_{STEP}	AF1 – AFOUT1 AF2 – AFOUT2	—	2.5	3	3.5	dB
Attenuator step	A_{STEP}	—	ATT1 to 7	0.1	0.2	0.3	dB
RX DATA filter gain 1 (AMPS)	G_{RD1}	RDAMP – RDOUT	Input: –18dBV 13kHz AT = "H"	–5	–3	–1	dB
RX DATA filter gain 2 (TACS)	G_{RD2}	RDAMP – RDOUT	Input: –18dBV 10.4kHz AT = "L"	–4	–3	–2	dB
RX DATA filter gain 1 (N-TACS)	G_{RN1}	RDAMP – RNOUT	Input: –18dBV 0.2kHz NTF = "L"	–4	–3	–2	dB
RX DATA filter gain 2 (N-TACS)	G_{RN2}	RDAMP – RNOUT	Input: –18dBV 3.2kHz NTF = "H"	–4	–3	–2	dB
RX SAT filter gain	G_{SAT}	RDAMP – RSOUT	Input: –18dBV 6kHz	–1	0	1	dB
TX DATA filter gain 1 (AMPS)	G_{TD1}	TDAMP1 – TSVOUT	Input: –18dBV 19.2kHz AT = "H", DS = "H" ATT6 = 0dB	–5	–3	–1	dB
TX DATA filter gain 2 (AMPS)	G_{TD2}	TDAMP1 – TSVOUT	Input: –18dBV 9.4kHz AT = "H", DS = "L" ATT6 = 0dB	–4	–3	–2	dB
TX DATA filter gain 3 (TACS)	G_{TD3}	TDAMP1 – TSVOUT	Input: –18dBV 15.2kHz AT = "L", DS = "H" ATT6 = 0dB	–5	–3	–1	dB
TX DATA filter gain 4 (TACS)	G_{TD4}	TDAMP1 – TSVOUT	Input: –18dBV 7.5kHz AT = "L", DS = "L" ATT6 = 0dB	–4	–3	–2	dB
TX DATA filter gain 1 (N-TACS)	G_{TN}	TNAMP – TSVOUT	Input: –18dBV 0.14kHz NTF = "L" ATT7 = 0dB	–4	–3	–2	dB
RX audio filter gain	G_{RA}	RAAMP – RAOUT	Input: –18dBV 1kHz RAM = "L" BYPS = "H" ATT1 = 0dB	–1	–0.3	1	dB

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
RX audio mute	G_{RAM}	RAAMP – RAOUT	Input: –18dBV 1kHz RAM = "H" BYPS = "H" ATT1 = 0dB	50	—	—	dB
RX audio S/N ratio	SN_R	RAAMP – RAOUT	Input: –18dBV 1kHz RAM = "L" BYPS = "H" ATT1 = 0dB Band: 50Hz to 30kHz	50	—	—	dB
RX audio distortion	THD_R	RAAMP – RAOUT	Input: –18dBV 1kHz RAM = "L" BYPS = "H" ATT1 = 0dB Band: 50Hz to 30kHz	—	—	–50	dB
TX audio filter gain	G_{RA}	TAAMP – TSVOUT	Input: –18dBV 1kHz TAM = "L" BYPS = "H" DTM = "L" ATT5 = 0dB	–1	–0.3	1	dB
TX audio mute	G_{RAM}	TAAMP – TSVOUT	Input: –18dBV 1kHz TAM = "H" BYPS = "H" DTM = "L" ATT5 = 0dB	50	—	—	dB
TX audio S/N ratio	SN_R	TAAMP – TSVOUT	Input: –18dBV 1kHz TAM = "L" BYPS = "H" DTM = "L" ATT5 = 0dB Band: 50Hz to 30kHz	45	—	—	dB
TX audio distortion	THD_R	TAAMP – TSVOUT	Input: –18dBV 1kHz TAM = "L" BYPS = "H" DTM = "L" ATT5 = 0dB Band: 50Hz to 30kHz	—	—	–45	dB

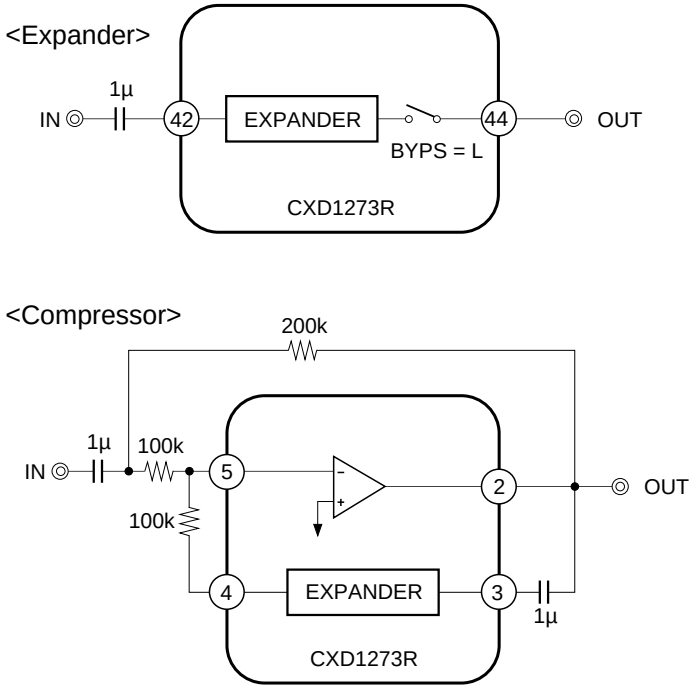
Compandor Characteristics

	Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Compressor	Input reference level	Acr	CONPIN – COMPOUT	—	α – 0.5	α	α – 0.5	dBV
	Output level	Aco	CONPIN – COMPOUT	Input: α – 30dBV Input: α – 50dBV	α – 16 α – 27	α – 15 α – 25	α – 14 α – 23	dBV
	Attack time	Tca	CONPIN – COMPOUT	12dB-step input	2.4	3.0	3.6	ms
	Recovery time	Tcr	CONPIN – COMPOUT	12dB-step input	10.8	13.5	16.2	ms
	Distortion + noise	THNc	CONPIN – COMPOUT	Input: α – 10dBV (1kHz)	—	–40	–30	dB
	Noise level	Ne	CONPIN – COMPOUT	Input: No signal	—	–40	–35	dBV
Expander	Input reference level	Aer	EXPIN – RAOUT	—	α – 1	α	α + 1	dBV
	Output level	Aeo	EXPIN – RAOUT	Input: α – 15dBV Input: α – 30dBV	α – 32 α – 66	α – 30 α – 60	α – 28 α – 54	dBV
	Attack time	Tea	EXPIN – RAOUT	6dB-step input	2.4	3.0	3.6	ms
	Recovery time	Ter	EXPIN – RAOUT	6dB-step input	2.4	3.0	3.6	ms
	Distortion + noise	THNe	EXPIN – RAOUT	Input: α – 5dBV (1kHz)	—	–45	–35	dB
	Noise level	Ne	EXPIN – RAOUT	Input: No signal	—	–88	–75	dBV

Notes)

1. 0dBV = 1Vrms
2. Definition of attack/recovery time based on AMPS standard.
3. Distortion + noise and noise level measurement range: 50Hz to 30kHz.
4. Output level expressed in value obtained after automatic correction of linearity. (Supply voltage and temperature variations after correction not included.)
5. Measurement circuit shown below.
6. In case 3V power supply is used: α = –4.4, 5V is used: α = 0.

Compandor Measurement Circuit



Description of Operation

This IC is a filter IC which is designed for use in cellular car telephones. It conforms to the AMPS (North America), TACS (United Kingdom), DOC (Canada), and N-TACS standards. When this filter IC is combined with the CXD1270Q/R control signal processing LSI chip, a modem is implemented with the following functions:

(1) Received Wide Band Data filtering
(2) Received SAT filtering
(3) Received SAT PLL lock detection
(4) Received N-TACS data filtering
(5) Transmitted Wide Band Data, ST, and SAT summing
(6) Transmitted Wide Band Data, ST, and SAT filtering
(7) Transmitted N-TACS data filtering
(8) Received audio filtering
(9) Transmitted audio filtering
(10) Attenuator and volume control
(11) Serial data input
(12) Compandor

These functions are detailed below:

1. Received Wide Band Data filtering

In a cellular car telephone system, data is exchanged in the line connection and hand-off processes between land stations (base stations) and mobile stations (mobile switching offices) for channel setup and other purposes. The data consists of Manchester code which is called Wide Band Data. The data transmission rate is 20kbaud for the AMPS/DOC standard, and is 16kbaud for the TACS standard. The received Wide Band Data is passed through the gain control amplifier and prefilter, and fed to the fourth-order Butterworth low-pass filter which functions as a Data demodulation roll-off filter. The low-pass filter cut-off frequency varies with the cellular standard standard and is controlled according to serial data. In the AMPS or DOC cellular system, a low-pass filter cut-off frequency of 13kHz (typical value) is obtained when AT = High. In the TACS or N-TACS system, a low-pass filter cut-off frequency of 10.4kHz (typical value) is obtained when AT = Low. Bandwidth limiting is provided in this manner so as to minimize the error rate.

After the filter output is waveform-shaped to CMOS logic levels by a comparator, it is transmitted to the CXD1270Q/R.

2. Received SAT filtering

While the cellular car telephone line is connected (during mobile telephone conversation), the land and mobile stations exchange a sine wave signal called SAT (supervisory audio tone) to acknowledge one another. Each cellular system standard provides three different SAT frequencies: 5.97kHz, 6.00kHz, and 6.03kHz. In the line connection and hand-off processes, one of these three frequencies is chosen. The land station sends 2-bit data called SCC (SAT color code) to the mobile station to notify which frequency is used. While the line is connected, the mobile and land stations receive the SAT from one another to recognize each other.

As is the case with the Wide Band Data, the SAT transmitted from the land station passes through the gain control amplifier and prefilter and then goes through the 6kHz eighth-order Butterworth band-pass filter which is provided to protect the SAT from the audio components (300Hz to 3kHz) and to reduce high-frequency noise (6kHz to 13kHz) in a weak electric field. As a band-pass filter having a center frequency of 6kHz is formed, SAT detection is accomplished with high efficiency. The 6kHz band-pass filter output is waveform-shaped to CMOS logic levels by a comparator and then transmitted to the CXD1270Q/R.

3. Received SAT PLL lock detection

When the SAT having a frequency designated by the SCC is received by the CXD1270Q/R, the DPLL is locked. The CXD1273R incorporates a lock/unlock judgment comparator. The output of this comparator switches from the Low to the High level when the CXD1270Q/R SAT lock detection output (SDET) exceeds the reference voltage ($0.75V_{DD}$).

4. Received N-TACS data filtering

When the CXD1273R is intended for use in the non-N-TACS standard, it can be used as an audio filter by changing control data NTF to High to change the cut-off frequency to 3.2kHz. To obtain 100Hz data to be used in the N-TACS standard, the received N-TACS data is passed through the sixth-order Butterworth low-pass filter having a cut-off frequency of 200Hz.

5. Transmitted Wide Band Data, ST, and SAT summing

In a cellular car telephone system, the mobile station sends the Wide Band Data or ST and SAT to the land station. The ST is a signal transmitted for telephone conversation termination or bell ringing purposes. Its frequency is 10kHz (AMPS/DOC standard) or 8kHz (TACS/N-TACS standard). Wide Band Data, ST, and SAT input from the CXD1270Q/R to CXD1273R is accomplished via an attenuation pad.

The CXD1273R incorporates an inverting summing amplifier which is used to sum up the Wide Band Data, ST, and SAT signals before transmission. As the transmission filter subsequent to the summing amplifier, the sixth-order Butterworth low-pass filter having a cut-off frequency of 19.2kHz (AMPS/DOC standard) or 15.2kHz (TACS/N-TACS standard) is selected at the time of Wide Band Data transmission, or the sixth-order Butterworth low-pass filter having a cut-off frequency of 9.4kHz (AMPS/DOC standard) or 7.5kHz (TACS/N-TACS standard) is chosen at the time of ST transmission.

To compensate for the amplitude characteristics difference between the 19.2kHz (15.2kHz) and 9.4kHz (7.5kHz) low-pass filters at a ST frequency of 10kHz, two different summing amplifiers gains can be selected. For ST transmission, the gain control data (GAIN1) is set to Low to obtain a gain of + (plus) several dB or set to High to obtain a gain of – (minus) several dB. An external resistor is to be adjusted to obtain the optimum gain.

6. Transmitted Wide Band Data, ST, and SAT filtering

A low-pass filter is provided subsequently to the summing amplifier to eliminate the high-order harmonic component of the summing amplifier output. The AMPS/DOC prescribes that a 20kHz ±10% fourth-order Butterworth low-pass filter be used as the transmitted Wide Band Data roll-off filter. Therefore, the CXD1273R employs a 19.2kHz sixth-order Butterworth low-pass filter to meet the AMPS 60kHz attenuation requirement (38dB min.). Further, the cut-off frequency of this transmission filter needs to be lower than 19.2kHz (typical value) because the ST and SAT transmission frequencies are 10kHz and 6kHz, respectively. The CXD1273R provides control according to serial data. When AT = High and DS = High, a cut-off frequency of 19.2kHz (typical value) is obtained. When AT = High and DS = Low, the obtained cut-off frequency is 9.4kHz (typical value).

As for the TACS/N-TACS standard, the transmission speed difference is compensated for by obtaining a cut-off frequency of 15.2kHz (typical value) when AT = Low and DS = High , or a cut-off frequency of 7.5kHz (typical value) when AT = Low and DS = Low.

7. Transmitted N-TACS data filtering

For the N-TACS standard, the sixth-order Bessel low-pass filter having a cut-off frequency of 140Hz is employed as the transmitted data roll-off filter.

8. Received audio filtering

Three Butterworth filters are employed to meet each cellular standard.

The input stage is equipped with a gain control amplifier and a loopback distortion elimination prefilter. The output stage is provided with a carrier elimination postfilter.

The RDOUT output is fed into the gain control amplifier, passed through the prefilter, de-emphasized by the first-order Butterworth low-pass filter, band-limited by the fifth-order and eighth-order Butterworth low-pass filters, and transferred out via the postfilter.

RAM provides muting control. Expander by-pass control is exercised with the BYPS control data.

9. Transmitted audio filtering

In the transmitter system, the audio signal is passed through the gain control amplifier and prefilter, band-limited by the fourth-order Butterworth high-pass filter and low-pass filter, passed through the postfilter prefilter, emphasized by the first-order Butterworth high-pass filter, and transferred out via the postfilter.

Further, the output is entered into the limiter via the gain control amplifier, clipped at 1.02 ± 0.18V (V_{DD} = 3V typ.), passed through the eighth-order Butterworth low-pass filter which serves as an abrupt splatter filter, and transferred out via the postfilter.

TAM exercises muting control, and the BYPS control data provides by-pass control of compressor.

DTM is normally at Low, however, when it is set to High, the splatter filter characteristics can be observed without being affected by the limiter.

10. Attenuator and volume control

Attenuators (ATT1 to ATT7) are provided at places where the audio signal level needs to be fine turned.
Further, two 3-bit control electronic volumes are incorporated to adjust the loudness of the speaker and exercise linking and other volume control.

C4	C3	C2	C1	C0	GAIN	
					ATT1, 5 to 7	ATT2 to 4
1	1	1	1	1	–3.0	–1.4
1	1	1	1	0	–2.8	–1.2
1	1	1	0	1	–2.6	–1.0
1	1	1	0	0	–2.4	–0.8
1	1	0	1	1	–2.2	–0.6
1	1	0	1	0	–2.0	–0.4
1	1	0	0	1	–1.8	–0.2
1	1	0	0	0	–1.6	0
1	0	1	1	1	–1.4	0.2
1	0	1	1	0	–1.2	0.4
1	0	1	0	1	–1.0	0.6
1	0	1	0	0	–0.8	0.8
1	0	0	1	1	–0.6	1.0
1	0	0	1	0	–0.4	1.2
1	0	0	0	1	–0.2	1.4
1	0	0	0	0	0	1.6
0	1	1	1	1	0.2	—
0	1	1	1	0	0.4	—
0	1	1	0	1	0.6	—
0	1	1	0	0	0.8	—
0	1	0	1	1	1.0	—
0	1	0	1	0	1.2	—
0	1	0	0	1	1.4	—
0	1	0	0	0	1.6	—
0	0	1	1	1	1.8	—
0	0	1	1	0	2.0	—
0	0	1	0	1	2.2	—
0	0	1	0	0	2.4	—
0	0	0	1	1	2.6	—
0	0	0	1	0	2.8	—
0	0	0	0	1	3.0	—
0	0	0	0	0	3.2	—

* VOLUME1, 2

C2	C1	C0	GAIN
1	1	1	–21
1	1	0	–18
1	0	1	–15
1	0	0	–12
0	1	1	–9
0	1	0	–6
0	0	1	–3
0	0	0	0

dB

11. Serial data input

The CXD1273R IC receives internal control data input in the form of 8-bit serial data. The four high-order bits are used for address indication, whereas the remaining four low-order bits are handled as data.

In the input process, 8-bit serial data is entered into the internal shift register when the DCLK clock pulse rises, and put into the internal buffer designated by the address upon receipt of the DEN load signal.

When the XDR reset signal is received, the internal buffer data is initialized.

Serial data structure descriptions, timing chart, and switching characteristics descriptions are presented below.

Serial Data Format (8-bit serial)

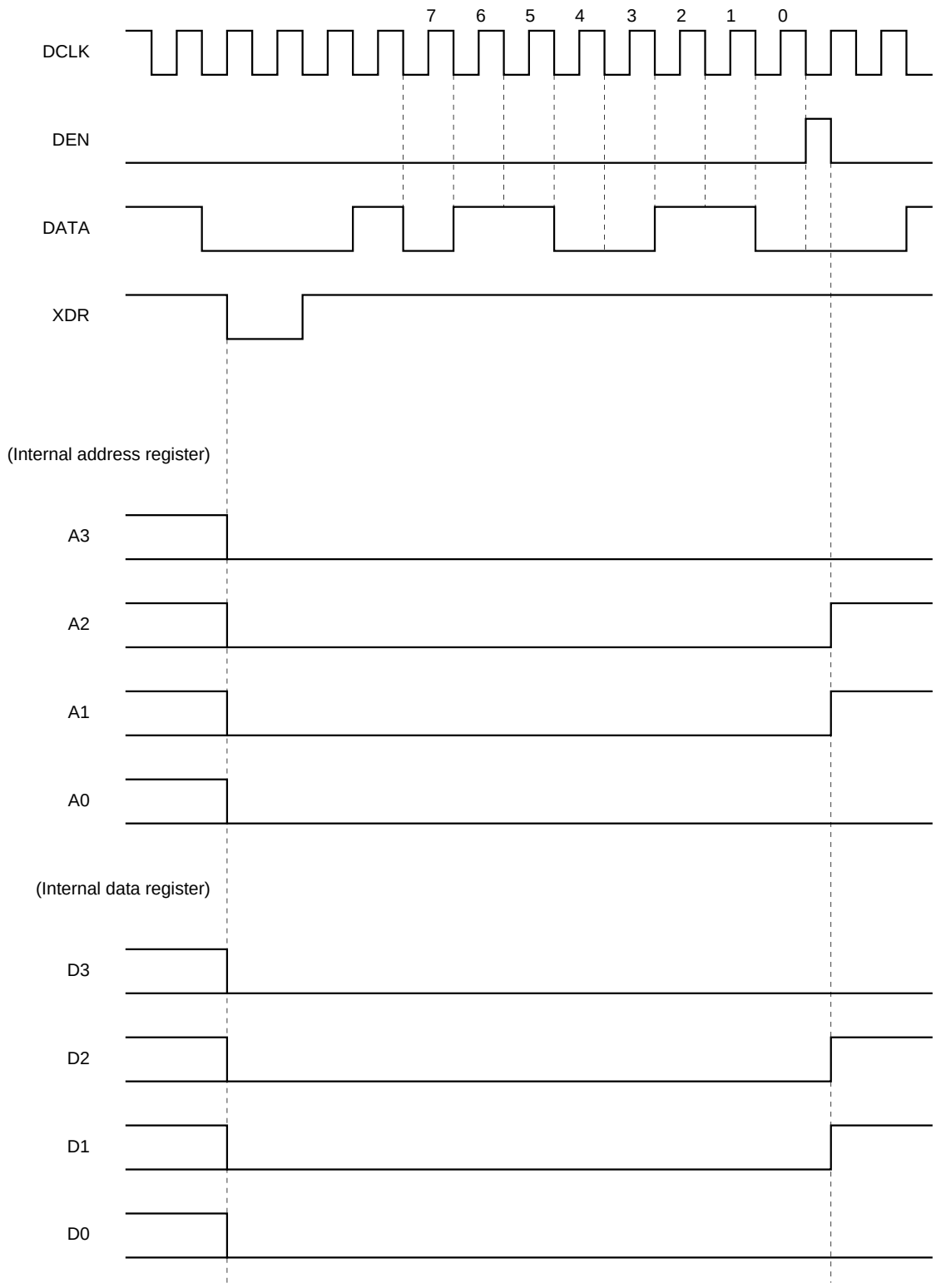
7	6	5	4	3	2	1	0	
0	0	0	0	AT 0	DS 1	STN 1	STD 1	
0	0	0	1	RAM 1	TAM 1	BYPS 0	DTM 0	
0	0	1	0	GAIN1 0	GAIN2 0	GAIN3 0	NTF 0	
0	0	1	1	CAL 1	LTL 0		CPG 0	
0	1	0	0			A8C5 1	A8C4 1	
0	1	0	1	A8C3 1	A8C2 1	A8C1 1	A8C0 1	
0	1	1	0	V1C2 1	V1C1 1	V1C0 1	V1ST 1	VOLUME1
0	1	1	1	V2C2 1	V2C1 1	V2C0 1	V2ST 1	VOLUME2
1	0	0	0	A1C3 0	A1C2 0	A1C1 0	A1C0 0	ATT1
1	0	0	1	A2C3 1	A2C2 0	A2C1 0	A2C0 0	ATT2
1	0	1	0	A3C3 1	A3C2 0	A3C1 0	A3C0 0	ATT3
1	0	1	1	A4C3 1	A4C2 0	A4C1 0	A4C0 0	ATT4
1	1	0	0	A5C3 0	A5C2 0	A5C1 0	A5C0 0	ATT5
1	1	0	1	A6C3 0	A6C2 0	A6C1 0	A6C0 0	ATT6
1	1	1	0	A7C3 0	A7C2 0	A7C1 0	A7C0 0	ATT7
1	1	1	1	A1C4 1	A5C4 1	A6C4 1	A7C4 1	ATT1, 5 to 7 Most significant bit
Address				Data				

Note) The state (“0” or “1”) prevailing upon data reset (XDR = Low) is indicated at the lower right-hand corner of above table columns.

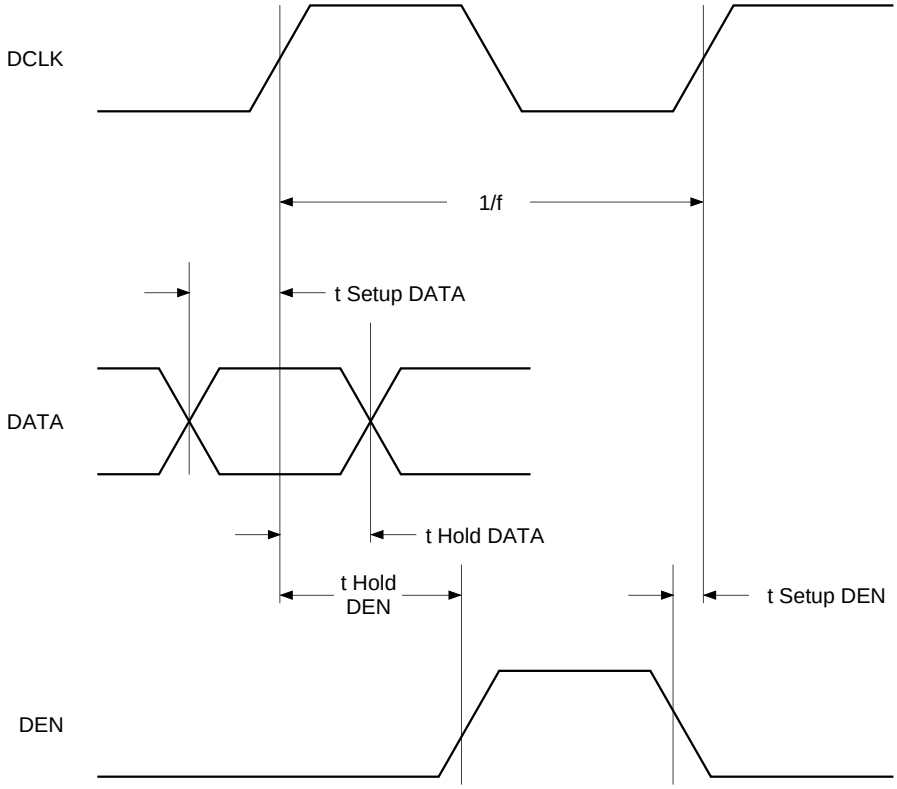
Control Data

Data name	Description
AT	AMPS/DOC standard is used at High; TACS/N-TACS standard is used at Low.
DS	WBD transmitted at High; SAT transmitted at Low.
STN	N-TACS data processing block in standby mode at High.
STD	Power save mode at High. (However, the data reception block operates at all times.)
RAM	Received audio is muted at High.
TAM	Transmitted audio is muted at High.
BYPS	Compandor is by-passed at High.
DTM	Audio signal transmitted at Low; DTMF signal transmitted at High.
GAIN1	Gain control of transmitted data summing input. TDAMP2 input switching is left open at High.
GAIN2	Gain control of transmitted and received audio. Transmission: –1.87dB, reception: –3.71dB at High.
GAIN3	Gain control of transmitted N-TACS input. –12dB at High.
NTF	Switchover of the filter fc for transmitted and received N-TACS. Transmission (Low: 0.14kHz, High: PASS); Reception (Low: 0.2kHz, High: 3.2kHz)
CAL	Automatic correction mode of compandor linearity at High. Not used when CAL = Low.
LTL	Gain control of DTMF Low tone signal (Low: –2dB, High: 0dB).
CPG	Gain control of compressor output (Low: –18dB, High: –14dB).
V1C2 to V1C0	VOLUME1 gain control (3-bit control; MSB: V1C2).
V1ST	VOLUME1 in standby mode at High.
V2C2 to V2C0	VOLUME2 gain control (3-bit control; MSB: V2C2).
V2ST	VOLUME2 in standby mode at High.
A1C4 to A1C0	ATT1 gain control (5-bit control; MSB: A1C4).
A2C3 to A2C0	ATT2 gain control (4-bit control; MSB: A2C3).
A3C3 to A3C0	ATT3 gain control (4-bit control; MSB: A3C3).
A4C3 to A4C0	ATT4 gain control (4-bit control; MSB: A4C3).
A5C4 to A5C0	ATT5 gain control (5-bit control; MSB: A5C4).
A6C4 to A6C0	ATT6 gain control (5-bit control; MSB: A6C4).
A7C4 to A7C0	ATT7 gain control (5-bit control; MSB: A7C4).
A8C5 to A8C0	Don't use. All of the bits must be set to High.

Serial Data Timing Chart



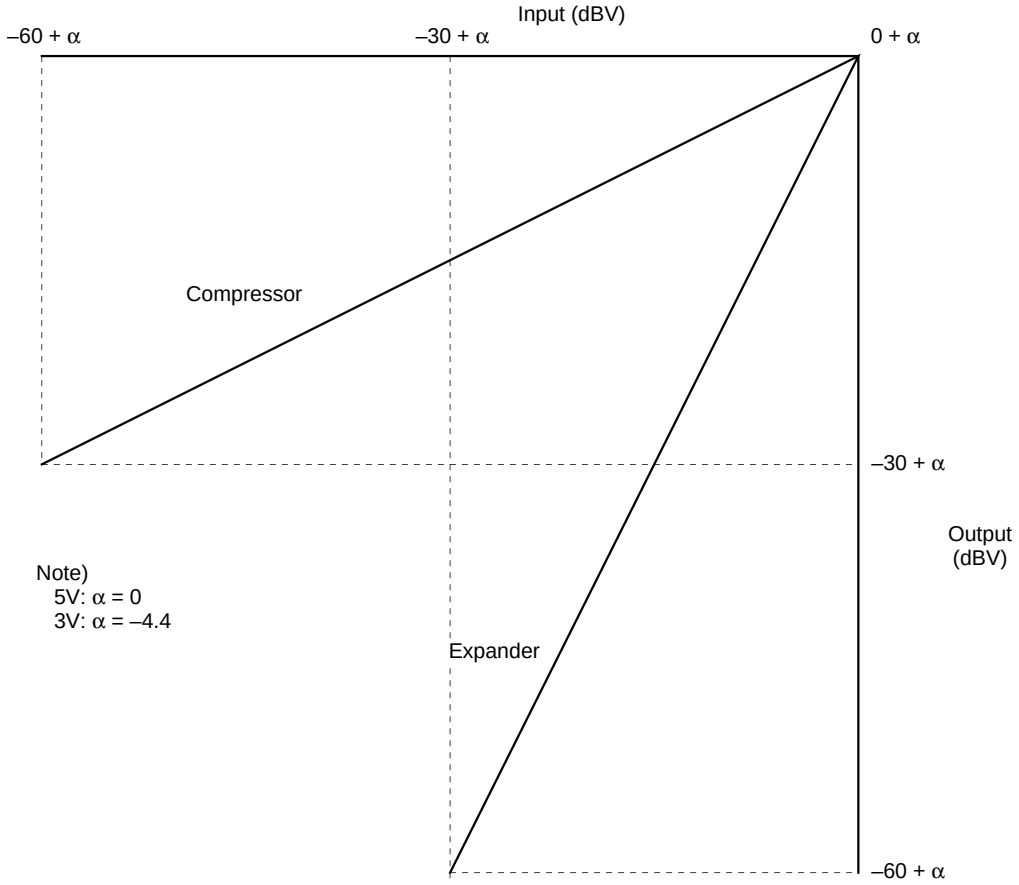
Serial Data Switching Characteristics



Item	Symbol	Min.	Typ.	Max.	Unit
DATA Set up Time	t Setup DATA	500	—	—	ns
DATA Hold Time	t Hold DATA	500	—	—	ns
DEN Set up Time	t Setup DEN	100	—	—	ns
DEN Hold Time	t Hold DEN	500	—	—	ns
DCLK frequency	f	—	—	1.2	MHz

Compandor

A feature of the expander is that, as shown in the graph below, the expander has 0dBV cross point (reference level) which is also its maximum input level, and acts only in the direction where the signal is attenuated. A compressor is configured by applying negative feedback to the expander through an operational amplifier. Therefore, the compressor, like the expander, has 0dBV reference level and its maximum input level. (In case 5V power supply is used)

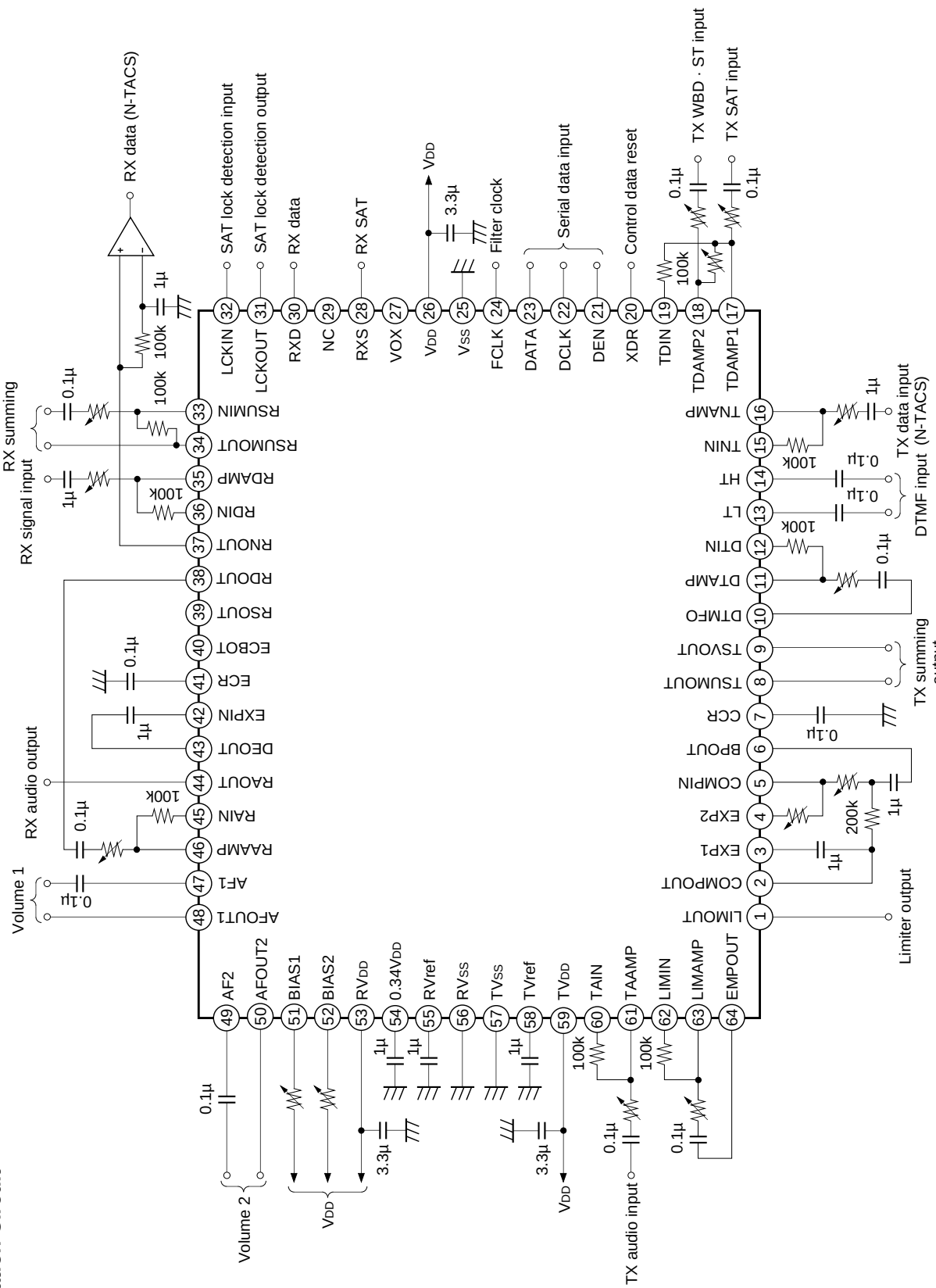


I/O Characteristics of Compandor

Automatic correction of linearity

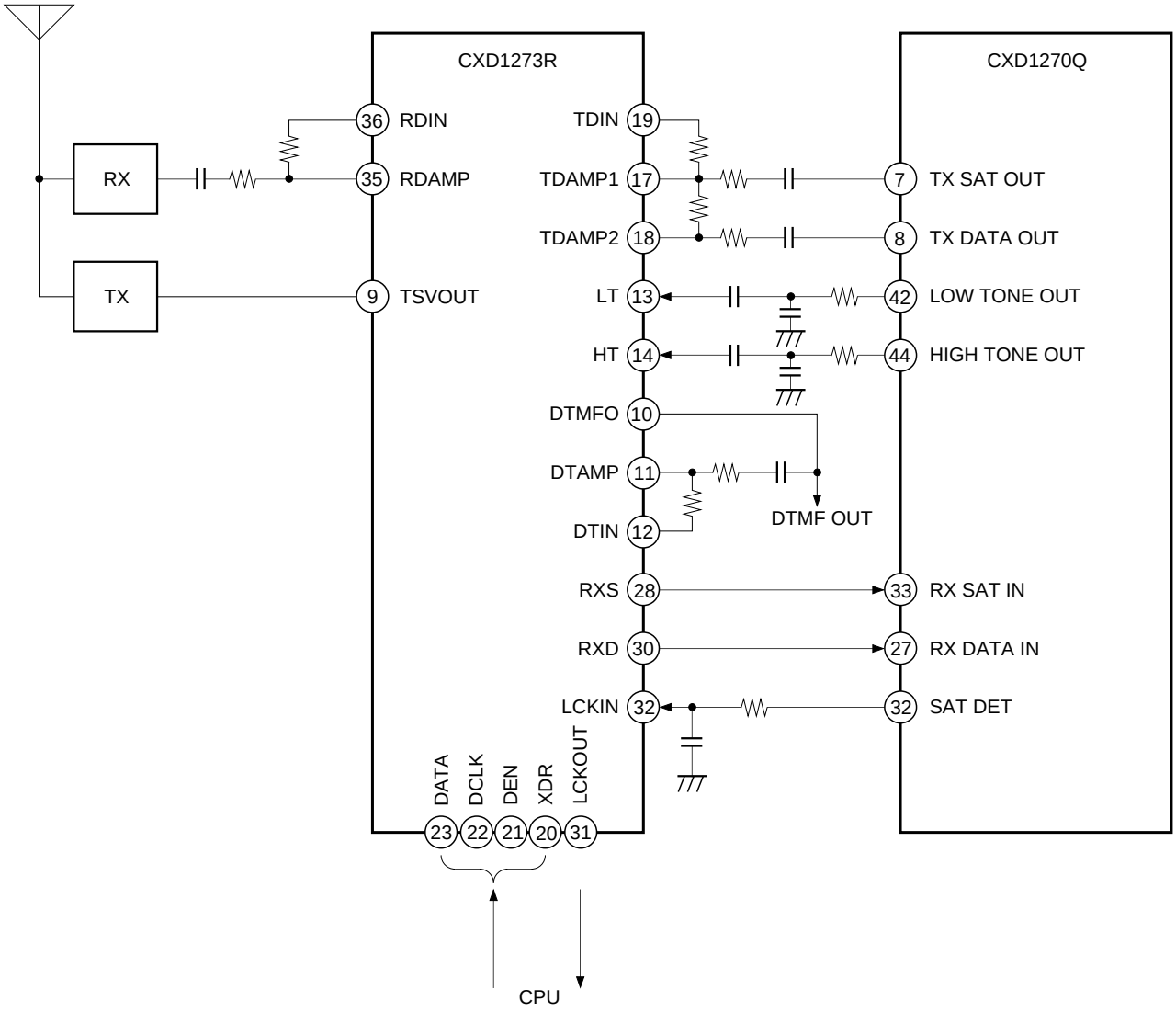
To maintain good linearity, the compandor executes automatic correction of linearity when it switches from the standby state to the active state (STD switches from High to Low). More precisely, the compandor starts automatic correction when recognition of control data CAL being High causes STD to fall from High to Low. Note that forced muting is done at that time. Forced muting is released when correction is completed. The time required for correction is 31ms maximum.

Application Circuit



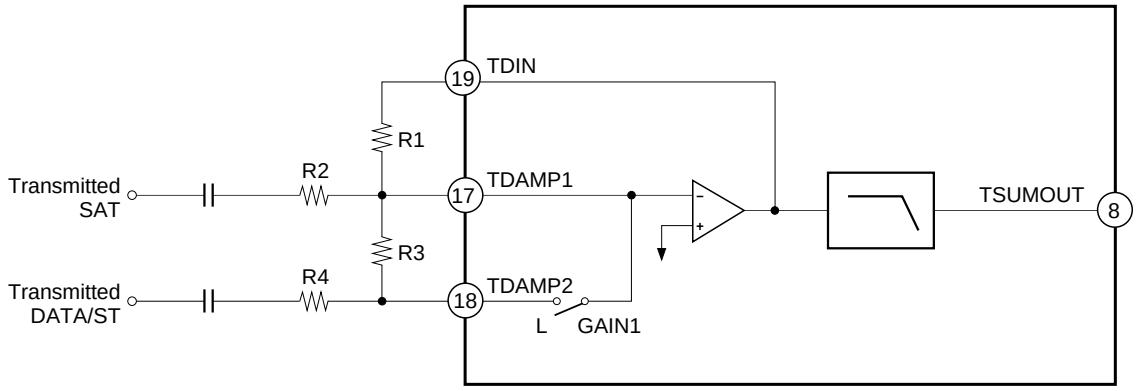
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Connection Example of CXD1273R and CXD1270Q



Notes on Operation

1. Gain Adjustment of Transmitted Data Summing Amplifier



Resistors R2 and R1 in the above circuit adjust the transmitted SAT attenuation, whereas resistors R4, R3, and R1 adjust the transmitted DATA/ST attenuation. The recommended amount of attenuation is –20dB.
Further the transmitted output level difference between the DATA and ST is compensated for by the resistor R3.
For ST transmission, the GAIN1 data is set to Low to raise the gain. For DATA transmission, the GAIN1 data is set to High to lower the gain.

2. Cellular System Setup and Transmitted Data Changeover

The data filter cut-off frequency is controlled to match the employed cellular system and transmitted data. For this control, the "AT" and "DS" control data are used.

Transmitted data / Cellular system	WBD	ST, SAT
AMPS, DOC	AT = H DS = H	AT = H DS = L
TACS, N-TACS	AT = L DS = H	AT = L DS = L

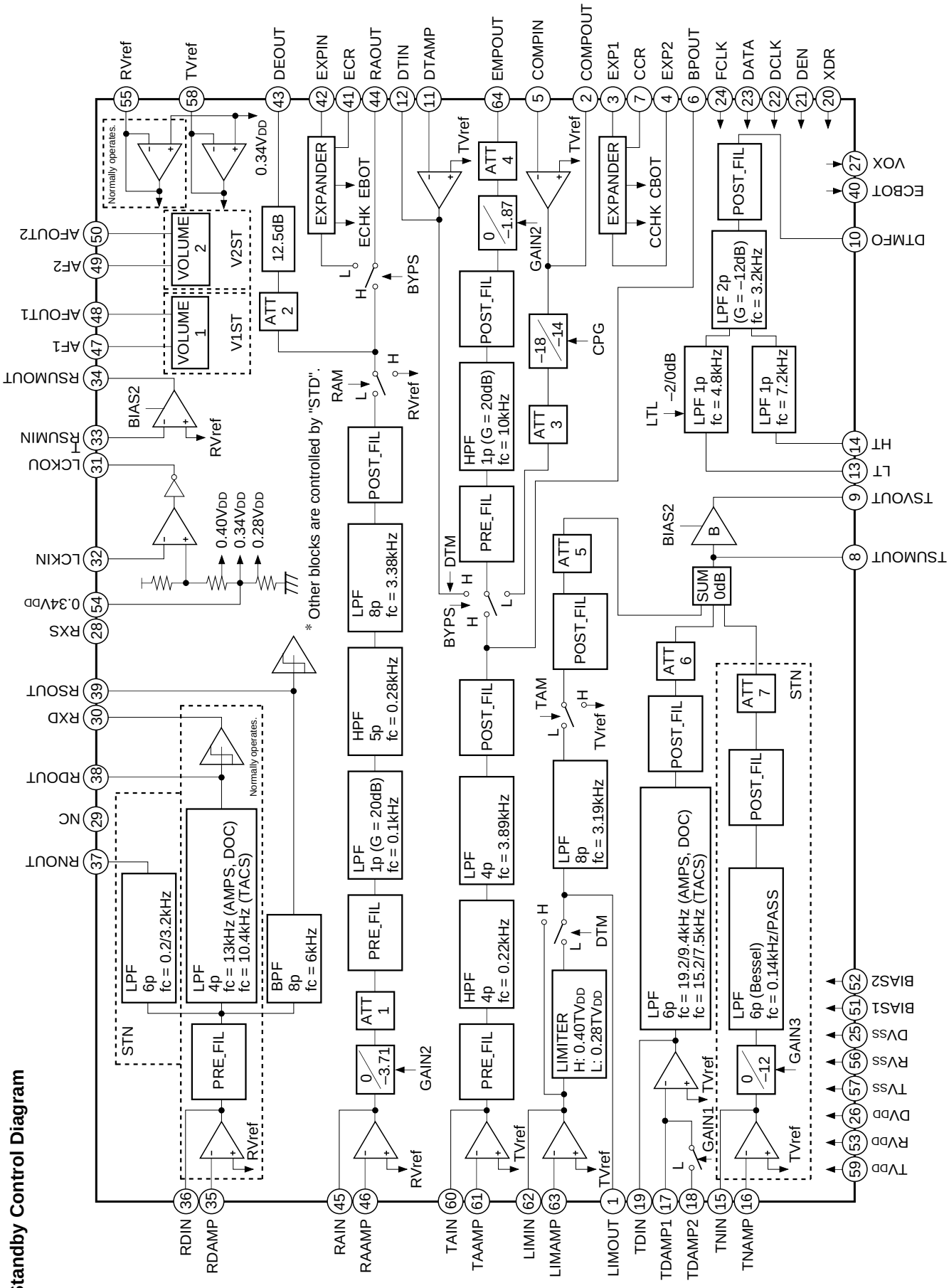
3. Standby Control

Standby control is exercised independently by the "STD", "STN", "V1ST", "V2ST" control data.

Control data	Control block	High	Low
STD	Blocks other than VOLUME1, VOLUME2, and N-TACS data processing blocks	Only block up to RDAMP-RXD, and the RVref generator circuit are active	Active
STN	N-TACS data processing block	Standby	Active
V1ST	VOLUME1	Standby	Active
V2ST	VOLUME2	Standby	Active

Note) Operation with STD = H and STN = L cannot be used.

Standby Control Diagram



4. Output Voltage Range and Supply Current Adjustment

The CXD1273R varies its output level range and supply current depending on the BIAS resistor (resistor connected between the BIAS1 and RV_{DD} pins).

The data presented under Electrical Characteristics are obtained at a BIAS resistance of 100kΩ with 10kΩ output load.

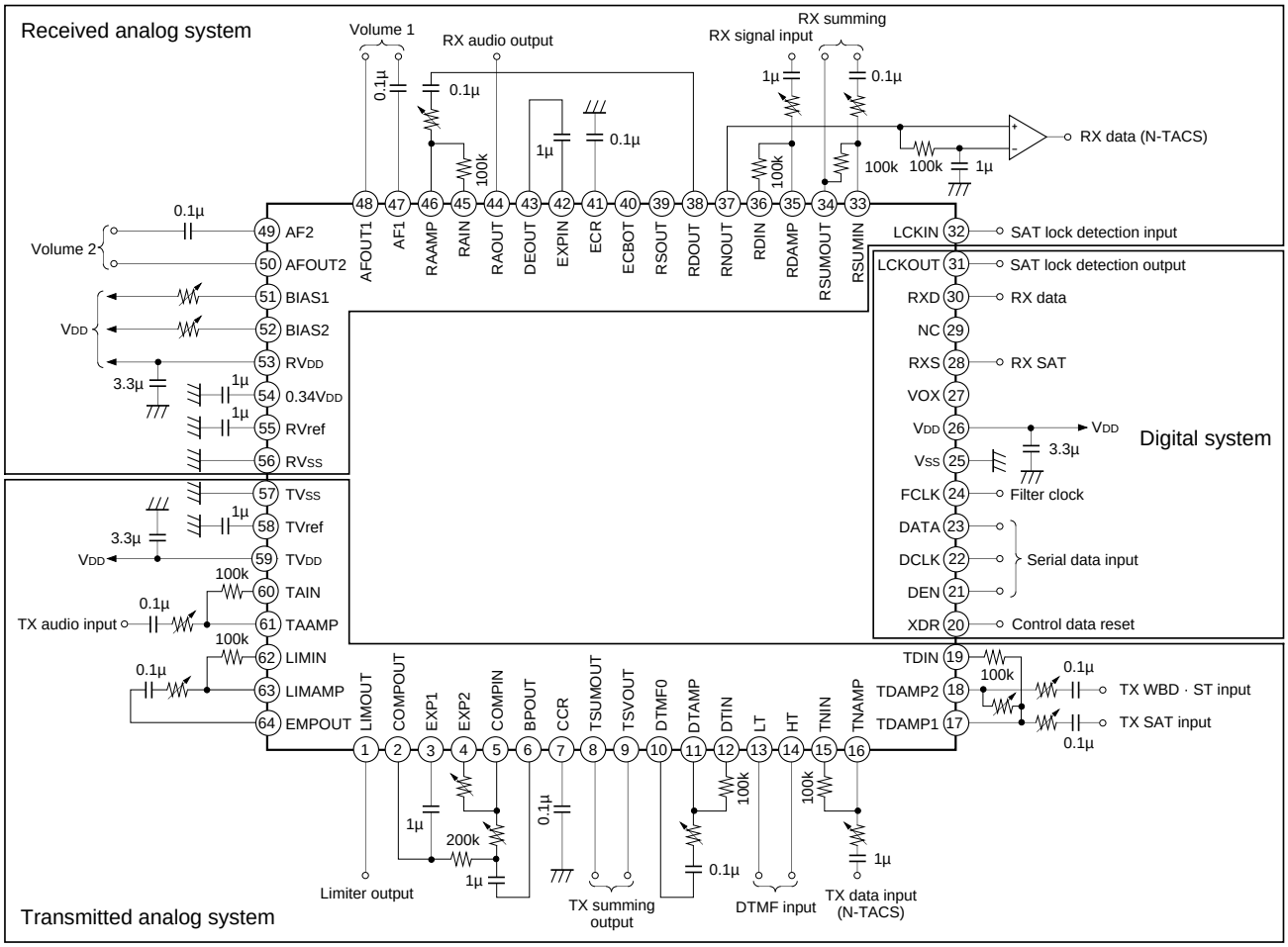
As the BIAS resistance determines the internal operational amplifier bias current, decreasing the BIAS resistance enlarges the output level range and supply current, and increasing the BIAS resistance reduces the output level range and supply current.

Therefore, the output voltage range and supply current can be adjusted as desired by varying the BIAS resistance.

5. Output Voltage Range Adjustment of High-load Operational Amplifier

As stated in the preceding section, the output voltage range can be adjusted by varying the BIAS resistance. However, the output voltage range of the receiver system summing amplifier (RSUMIN-RSUMOUT) and the TSVOUT can be independently varied by adjusting the other BIAS resistance (connected between the BIAS2 and RV_{DD} pins). This feature is convenient in driving a heavy load without significantly affecting the supply current.

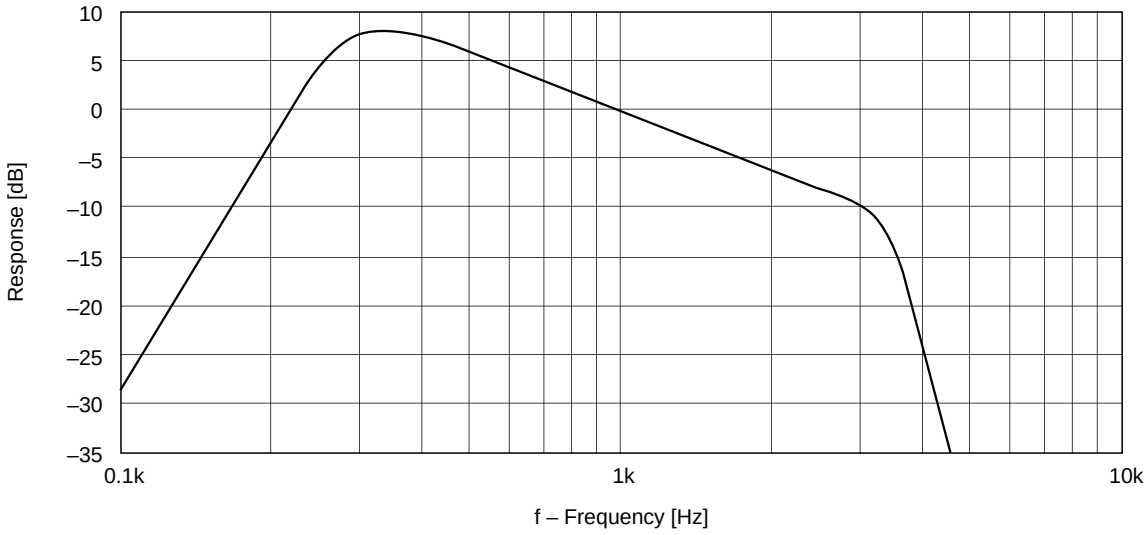
6. Notes for Board Layout



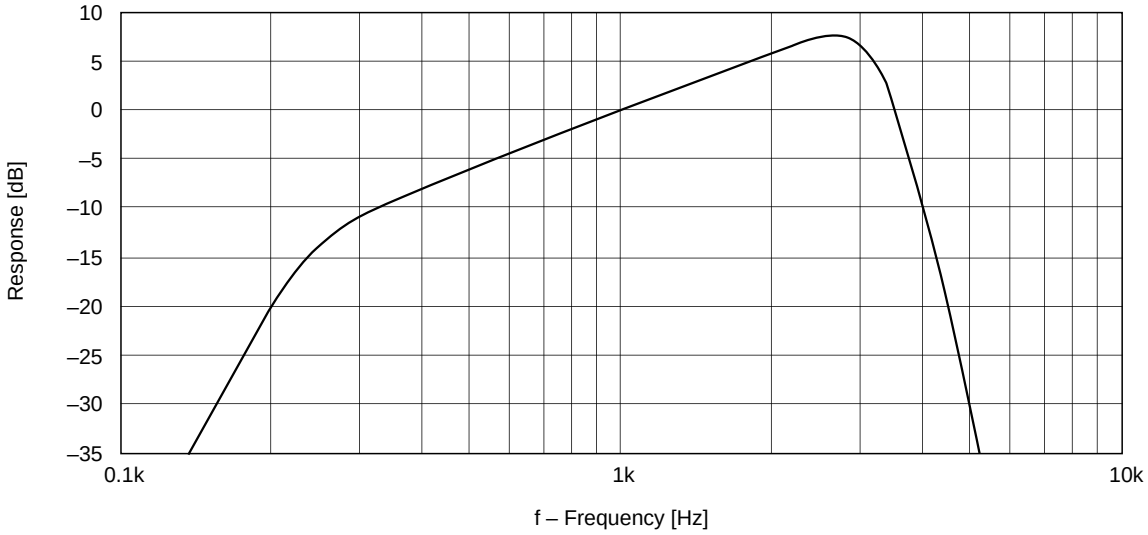
1) The power supply and GND are divided into three systems; received analog, transmitted analog, and digital systems as shown above. For protection against latch-up, put the power supply and GND wires of the three systems together near the set power supply.
2) Make sure that the wires of the three systems do not cross one another whenever possible.
3) A by-pass capacitor should be connected directly near the pins.
4) Compandor smoothing capacitors (Pins 41 and 7) should be directly connected near the pins.
5) A compressor configuration circuit (Pins 2 to 6) should be compactly arranged at a position as close to the pins as possible.

Filter Characteristics

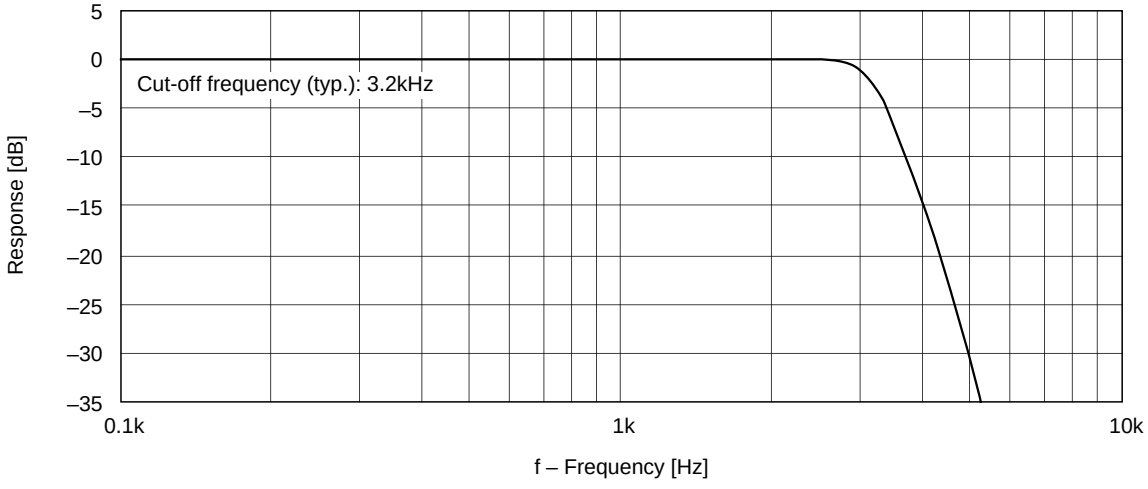
Received audio filter amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



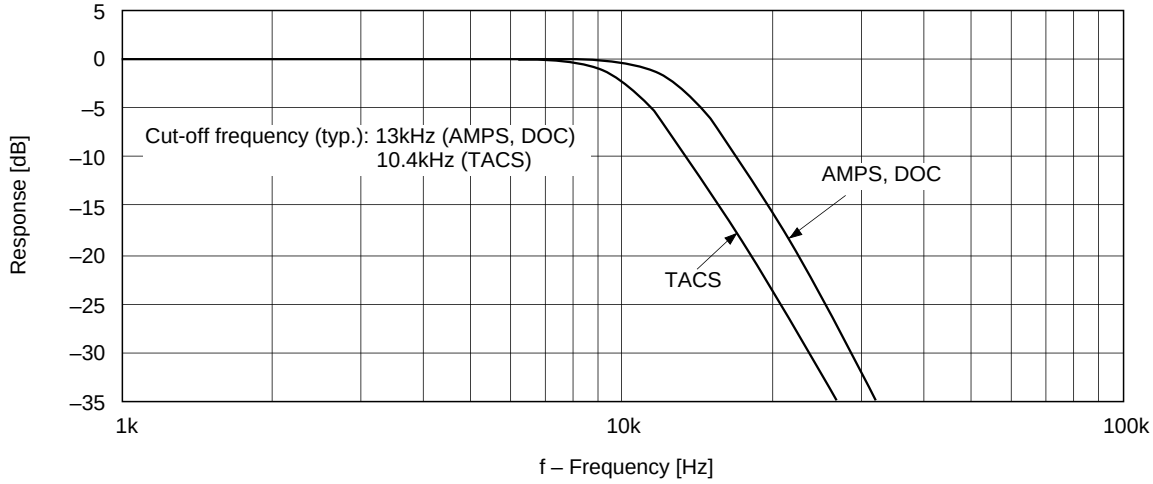
Transmitted audio filter (splatter filter included) amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



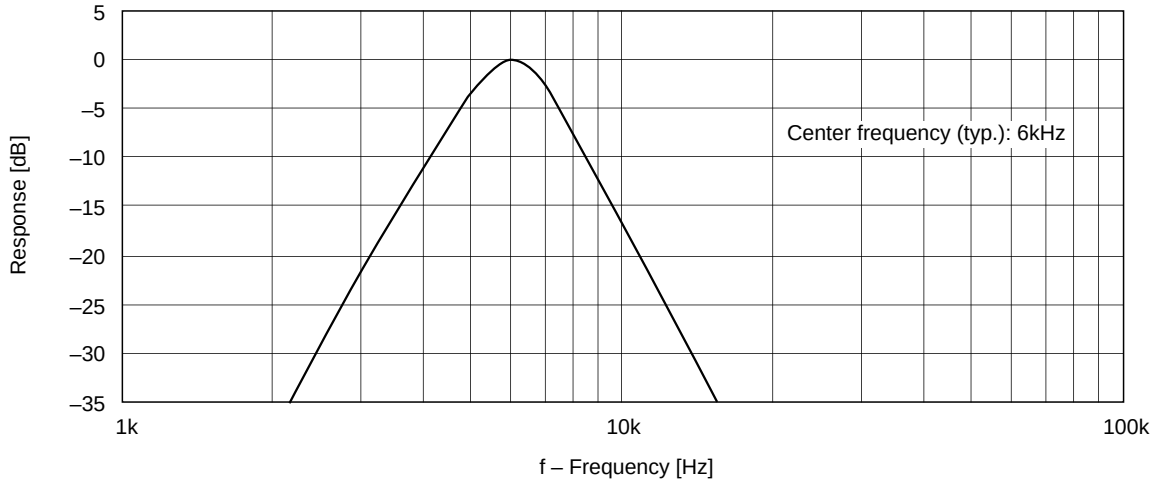
Splatter filter amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



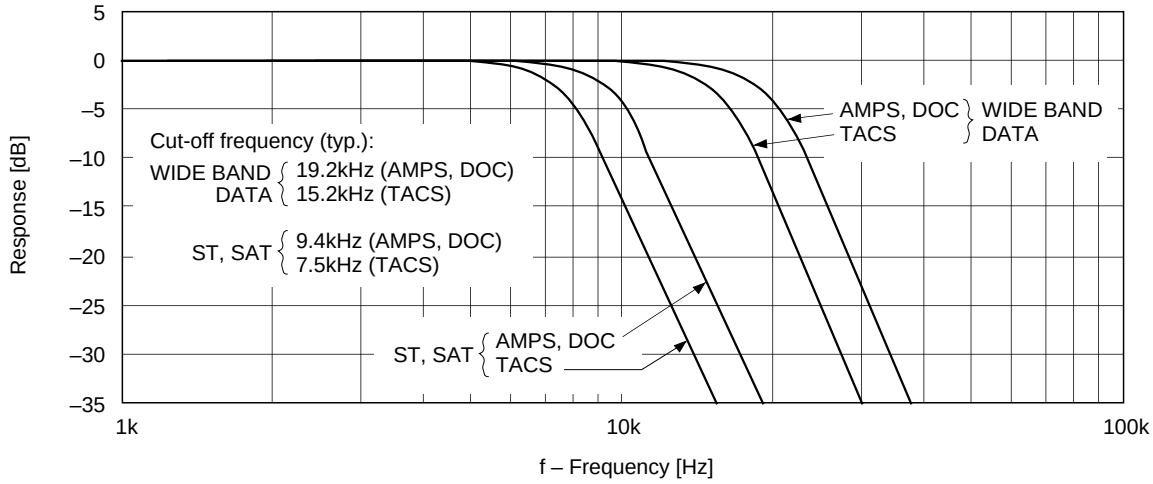
Received Wide Band Data LPF amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



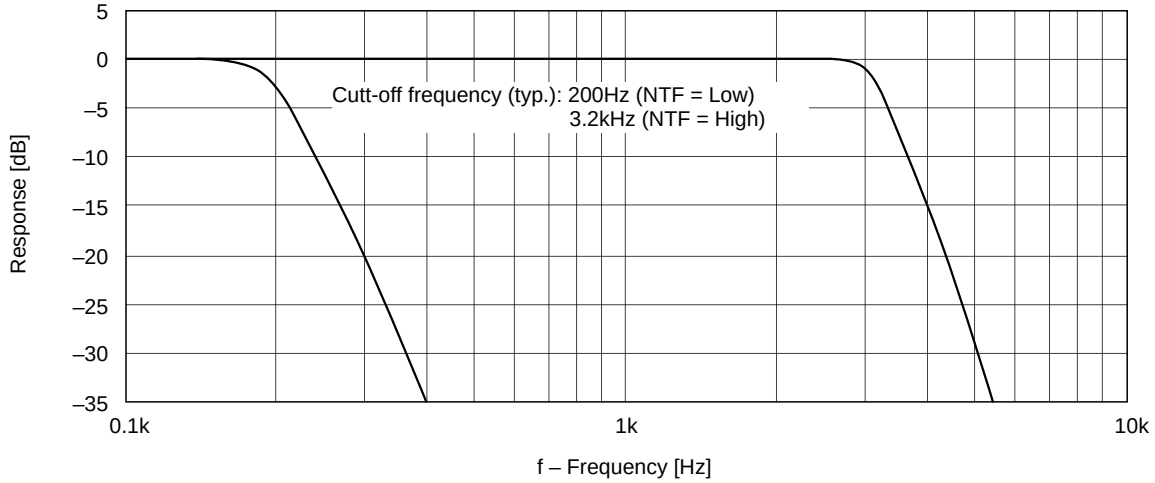
Received SAT BPF amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



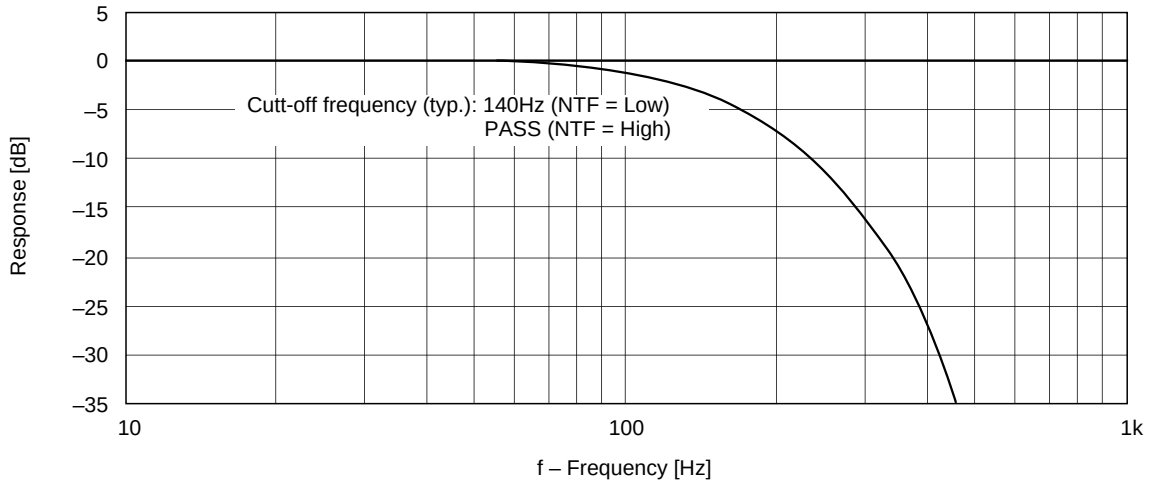
Transmitted Wide Band Data, ST, SAT LPF amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



Received N-TACS data LPF amplitude characteristics (V_{DD} = 3V, Ta = 25°C)

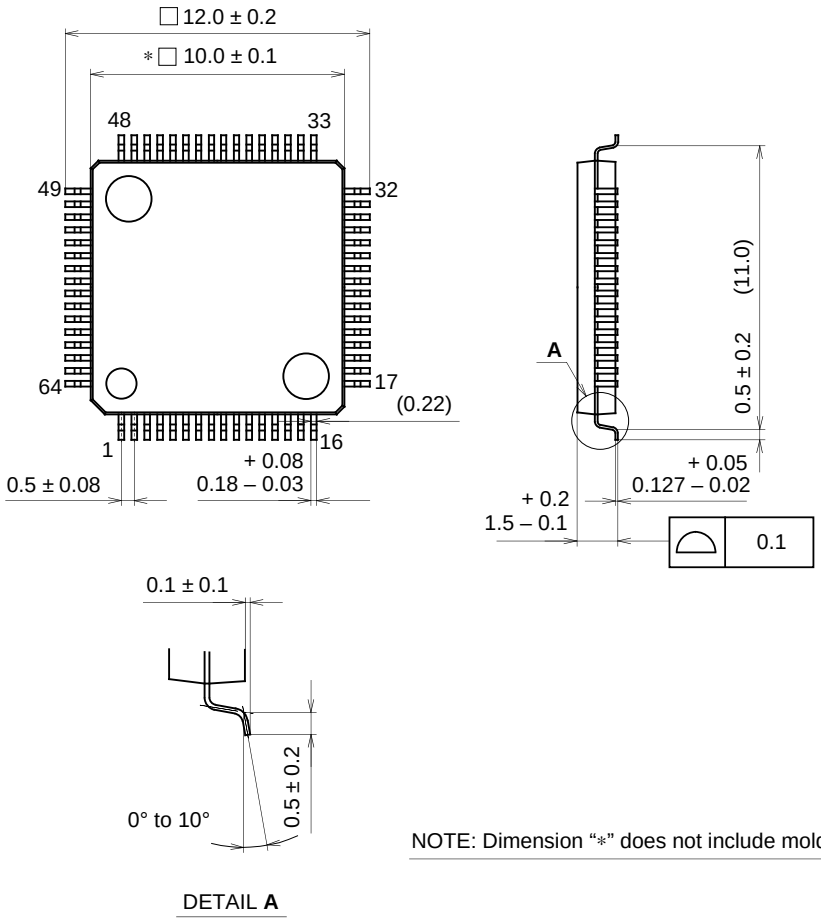


Transmitted N-TACS data LPF amplitude characteristics (V_{DD} = 3V, Ta = 25°C)



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	∗QFP064-P-1010-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g