SONY

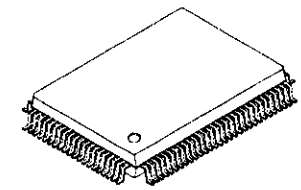
CXD1806AQ

CD-ROM DECODER

Description

CXD1806AQ is a CD-ROM decoder LSI.

100 pin QFP (Plastic)



Features

- Compatible with CD-ROM, CD-I and CD-ROM XA formats
- Real time error correction
- Capable of handling up to quadruple speed playback
- Multiblock auto-transfer function
- Can read subcode-Q data for each byte from the sub CPU
- Serial transfer of commands to CD DSP
- Maximum transfer speed to host of 5.6MB/s when decoding is on (when clock frequency is 33.8688MHz and playback speed is 2.4x or slower)
- Maximum transfer speed to host of 6.7MB/s when decoding is off (when clock frequency is 33.8688MHz)
- Connectable with standard SRAM of up to 1M-bit (128K-byte)
- Connectable with standard DRAM of up to 4M-bit (512K-byte)
- Connectable with standard pseudo-SRAM of up to 1M-bit (128K-byte)
- Connectable directly with Sony's SCSI controller CXD1185CQ.

Applications

CD-ROM drives

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

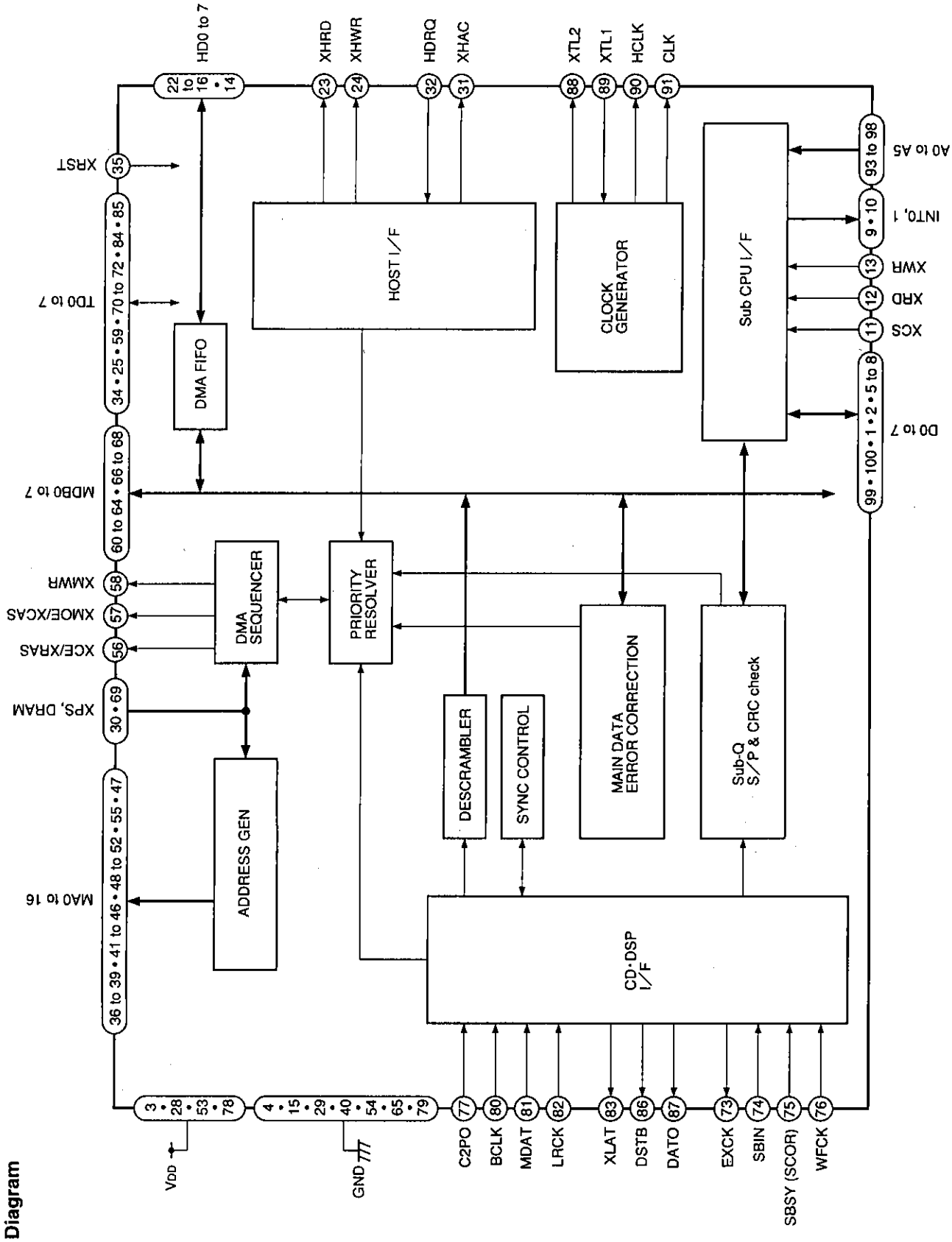
• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V
• Output voltage	V_O	−0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 typ.)	V
• Operating temperature	Topr	−20 to +75	°C

E95211A58—ST

Block Diagram



Pin Description

Pin No.	Sumbol	I/O	Description
1	D2	I/O	Sub CPU data bus
2	D3	I/O	Sub CPU data bus
3	V_{DD}	—	Power supply (+5V)
4	GND	—	Ground
5	D4	I/O	Sub CPU data bus
6	D5	I/O	Sub CPU data bus
7	D6	I/O	Sub CPU data bus
8	D7	I/O	Sub CPU data bus
9	INT0	O	Interrupt request signal from IC to sub CPU
10	INT1	O	Interrupt request signal from IC to sub CPU
11	XCS	I	Chip select negative logic signal from sub CPU
12	XWR	I	Strobe negative logic signal to write this IC internal register from sub CPU
13	XRD	I	Strobe negative logic signal to read this IC internal register from sub CPU
14	HD7	I/O	Host data bus
15	GND	—	Ground
16	HD6	I/O	Host data bus
17	HD5	I/O	Host data bus
18	HD4	I/O	Host data bus
19	HD3	I/O	Host data bus
20	HD2	I/O	Host data bus
21	HD1	I/O	Host data bus
22	HD0	I/O	Host data bus
23	XHRD	O	Data write strobe signal to SCSI controller IC
24	XHWR	O	Data read strobe signal to SCSI controller IC
25	TD1	I/O	Test input/output
26	N.C.	—	
27	N.C.	—	
28	V_{DD}	—	Power supply (+5V)
29	GND	—	Ground
30	XPS	I	PSRAM selection negative logic signal
31	XHAC	O	DMA acknowledge negative logic signal to SCSI controller IC
32	HDRQ	I	DMA data request positive logic signal from SCSI controller IC
33	N.C.	—	

Pin No.	Symbol	I/O	Description
34	TD0	I/O	Test input/output
35	XRST	I	Reset negative logic signal
36	MA0	O	Buffer memory address (LSB)
37	MA1	O	Buffer memory address
38	MA2	O	Buffer memory address
39	MA3	O	Buffer memory address
40	GND	–	Ground
41	MA4	O	Buffer memory address
42	MA5	O	Buffer memory address
43	MA6	O	Buffer memory address
44	MA7	O	Buffer memory address
45	MA8	O	Buffer memory address
46	MA9	O	Buffer memory address
47	MA16	O	Buffer memory address
48	MA10	O	Buffer memory address
49	MA11	O	Buffer memory address
50	MA12	O	Buffer memory address
51	MA13	O	Buffer memory address
52	MA14	O	Buffer memory address
53	V_{DD}	–	Power supply (+5V)
54	GND	–	Ground
55	MA15	O	Buffer memory address
56	XCE XRAS	O	Buffer memory chip enable, or row address strobe signal
57	XMOE XCAS	O	Buffer memory output enable negative logic signal, or column address strobe signal
58	XMWR	O	Buffer memory write enable negative logic signal
59	TD2	I/O	Test input
60	MDB0	I/O	Buffer memory data bus
61	MDB1	I/O	Buffer memory data bus
62	MDB2	I/O	Buffer memory data bus
63	MDB3	I/O	Buffer memory data bus
64	MDB4	I/O	Buffer memory data bus
65	GND	–	Ground
66	MDB5	I/O	Buffer memory data bus
67	MDB6	I/O	Buffer memory data bus
68	MDB7	I/O	Buffer memory data bus

Pin No.	Symbol	I/O	Description
69	DRAM	I	DRAM/SRAM switch input
70	TD3	I/O	Test input
71	TD4	I/O	Test input
72	TD5	I/O	Test input
73	EXCK	O	SBIN signal strobe clock signal
74	SBIN	I	Subcode data serial input signal
75	SCOR	I	Subcode sync signal
76	WFCK	I	Write frame clock input signal
77	C2PO	I	Error flag (C2 pointer) positive logic signal from CD DSP
78	V_{DD}	—	Power supply (+5V)
79	GND	—	Ground
80	BCLK	I	DATA signal strobe clock signal (bit clock)
81	DATA	I	Data signal from CD DSP
82	LRCK	I	LR clock signal from CD DSP (for discriminating L, R channels)
83	XLAT	O	DATO signal latch signal
84	TD6	I/O	Test input
85	TD7	I/O	Test input
86	DSTB	O	DATO signal transfer clock output
87	DATO	O	Serial data output to CD DSP
88	XTL2	O	Crystal oscillation circuit output
89	XTL1	I	Crystal oscillation circuit input
90	GND	—	Ground
91	HCLK	O	Clock output with 1/2 the frequency of the XTL1 pin
92	CLK	O	Clock output with the same frequency as that of the XTL1 pin
93	A0	I	Sub CPU address
94	A1	I	Sub CPU address
95	A2	I	Sub CPU address
96	A3	I	Sub CPU address
97	A4	I	Sub CPU address
98	A5	I	Sub CPU address
99	D0	I/O	Sub CPU data bus
100	D1	I/O	Sub CPU data bus

Note: The CXD1806AQ is not pin-compatible with the CXD1808AQ.

Electrical Characteristics

DC Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input level pin *1 High level input voltage	V_{IH1}		2.2			V
TTL input level pin *1 Low level input voltage	V_{IL1}				0.8	V
CMOS input level pin *2 High level input voltage	V_{IH2}		0.7V_{DD}			V
CMOS input level pin *2 Low level input voltage	V_{IL2}				0.3V_{DD}	V
CMOS Schmitt input level pin *3 High level input voltage	V_{IH4}		0.8V_{DD}			V
CMOS Schmitt input level pin *3 Low level input voltage	V_{IL4}				0.2V_{DD}	V
CMOS Schmitt input level pin *3 Input voltage hysteresis	$V_{IH4} - V_{IL4}$			0.6		V
TTL Schmitt input level pin *4 High level input voltage	V_{IH5}		2.2			V
TTL Schmitt input level pin *4 Low level input voltage	V_{IL5}				0.8	V
TTL Schmitt input level pin *4 Input voltage hysteresis	$V_{IH5} - V_{IL4}$			0.4		V
Bidirectional pin with pull-up resistor*5 Input current	I_{IL3}	V_{IN} = 0V	–90	–200	–440	µA
Input pin with pull-up resistor *6 Input current	I_{IL4}	V_{IN} = 0V	–40	–100	–240	µA
High level output voltage *7	V_{OH1}	I_{OH} = –2mA	V_{DD} –0.8			V
Low level output voltage *7	V_{OL1}	I_{OL} = 4mA			0.4	V
Input leakage current *8	I_{I1}	V_{IN} = Vss or V_{DD}	–10		10	µA
Output leakage current *9	I_{OZ}	High-impedance state	–40		40	µA
Oscillation cell *10 high level input voltage	V_{IH4}		0.7V_{DD}			V
Oscillation cell low level input voltage	V_{IL4}				0.3V_{DD}	V
Oscillation cell logic threshold value	LV_{TH}			0.5V_{DD}		V
Oscillation cell feedback resistance value	R_{FB}	V_{IN} = Vss or V_{DD}	250K	1M	2.5M	Ω
Oscillation cell High level output voltage	V_{OH2}	I_{OH} = –3mA	0.5V_{DD}			V
Oscillation cell Low level output voltage	V_{OL2}	I_{OL} = 3mA			0.5V_{DD}	V

*1 D7 to 0, HD7 to 0, MDB7 to 0, TD1, TD0
*2 MDAT, LRCK, C2PO, EMP, RMCK, SBIN, SBSY, WFCK, XPS
*3 BCLK, XRST
*4 A5 to 0, XWR, XRD, XCS, XPS
*5 D7 to 0, MDB7 to 0, HD7 to 0, TD1, TD0
*6 HA1, HA0, XHAC
*7 All output pins except XTL2
*8 All input pins except *5, *6 and XTL1
*9 HINT
*10 Input: XTL1, Output: XTL2

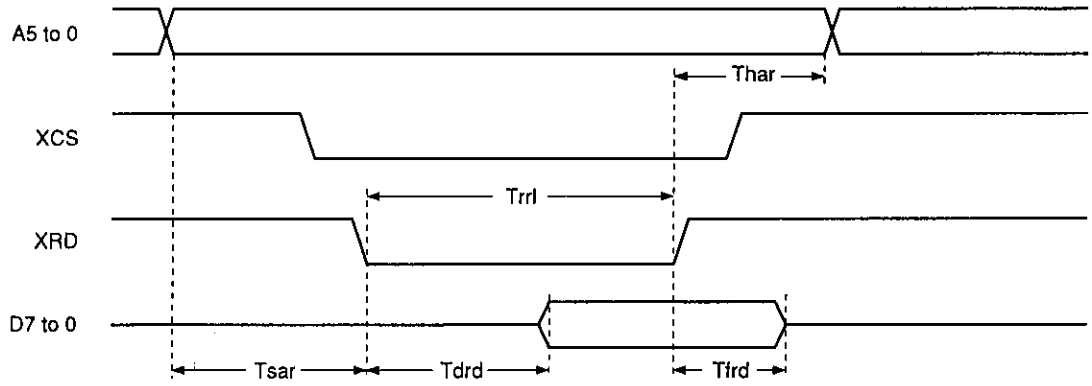
I/O Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}			9	pF
Output capacitance	C_{OUT}			11	pF
I/O capacitance	$C_{I/O}$			11	pF

AC Characteristics (V_{DD} = 5V ±10%, Vss = 0V, Topr = −20 to +75°C)

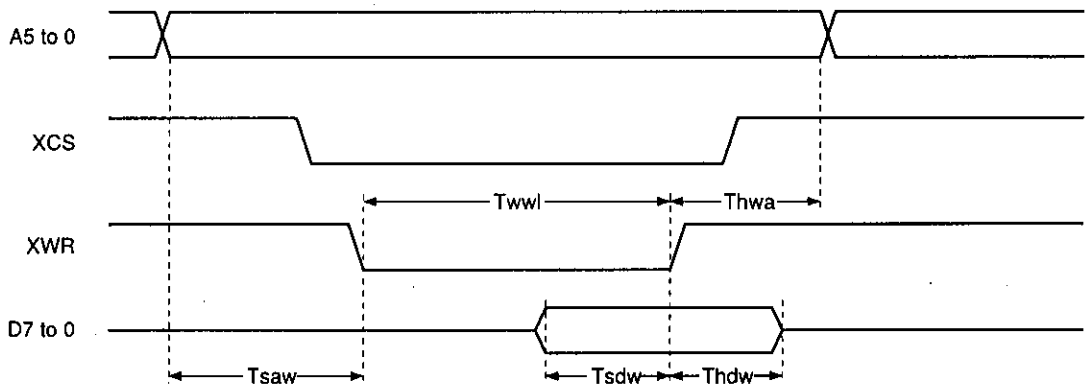
1. Sub CPU Interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XRD ↓)	Tsar	10			ns
Address hold time (for XCS & XRD ↑)	Thar	10			ns
Data delay time (for XCS & XRD ↓)	Tdrd			35	ns
Data float time (for XCS & XRD ↑)	Tfrd	0		15	ns

(2) Write

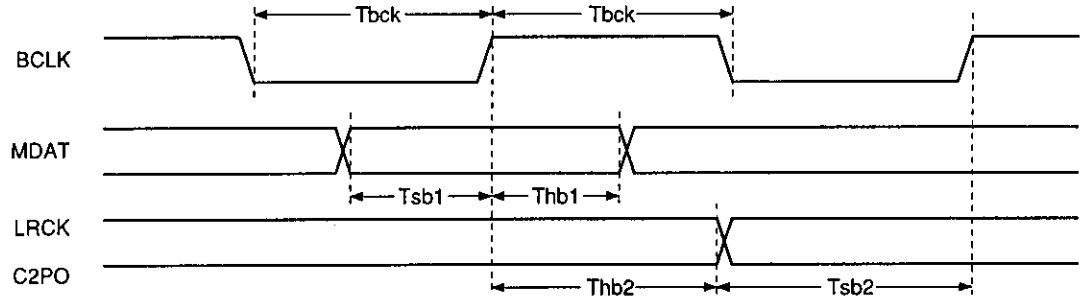


Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XWR ↓)	Tsaw	20			ns
Address hold time (for XCS & XWR ↑)	Thaw	10			ns
Data setup time (for XCS & XWR ↓)	Tsdw	20			ns
Data hold time (for XCS & XWR ↑)	Thdw	10			ns
Low level XWR pulse width	Twwl	30			ns

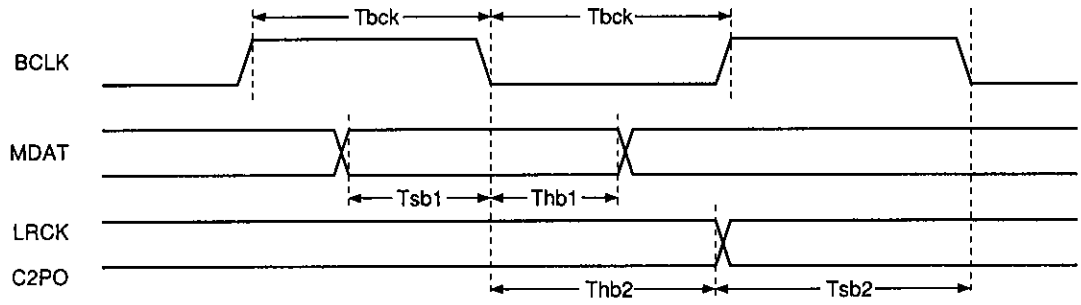
Note) "&" indicates "AND".

2. CD DSP Interface

BCKRED = "H"



BCKRED = "L"

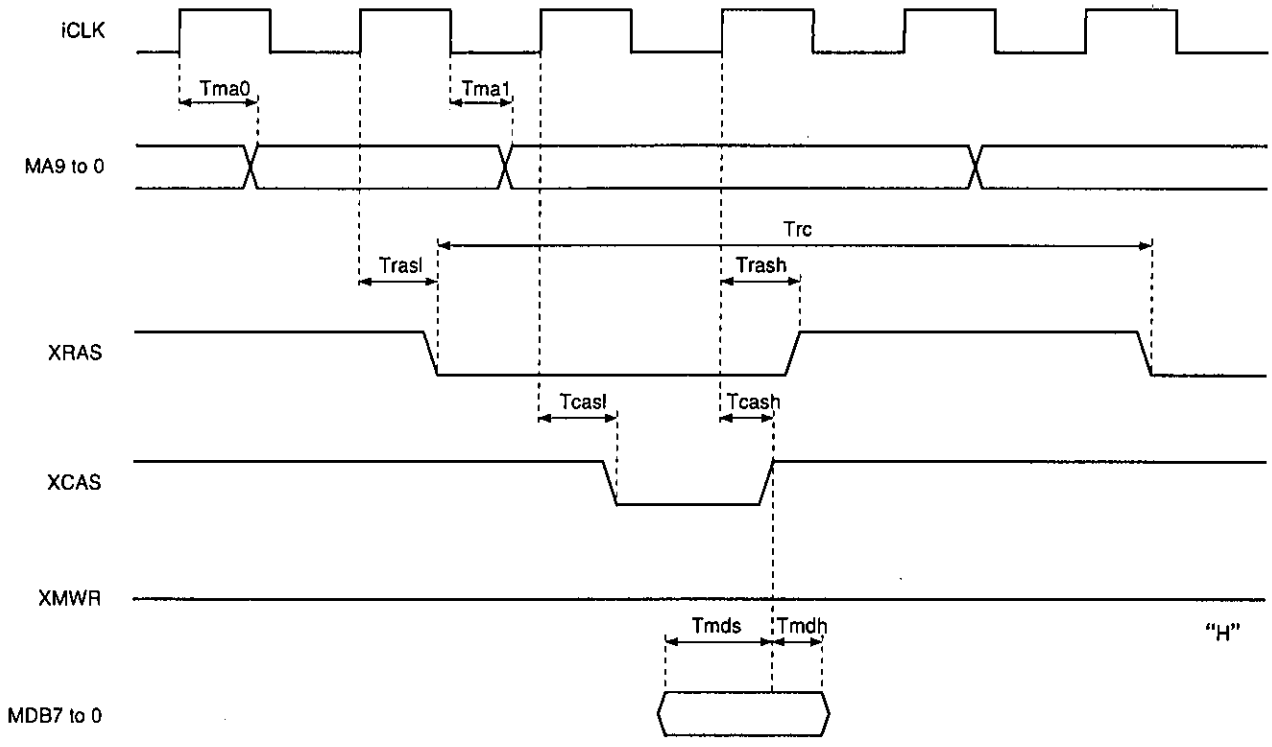


Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			26	MHz
BCLK pulse width	Tbck	19			ns
DATA setup time (for BCLK)	Tsb1	12			ns
DATA hold time (for BCLK)	Thb1	12			ns
LRCK, C2PO setup time (for BCLK)	Tsb2	12			ns
LRCK, C2PO hold time (for BCLK)	Thb2	12			ns

3. DRAM interface (Output Load = 30pF)

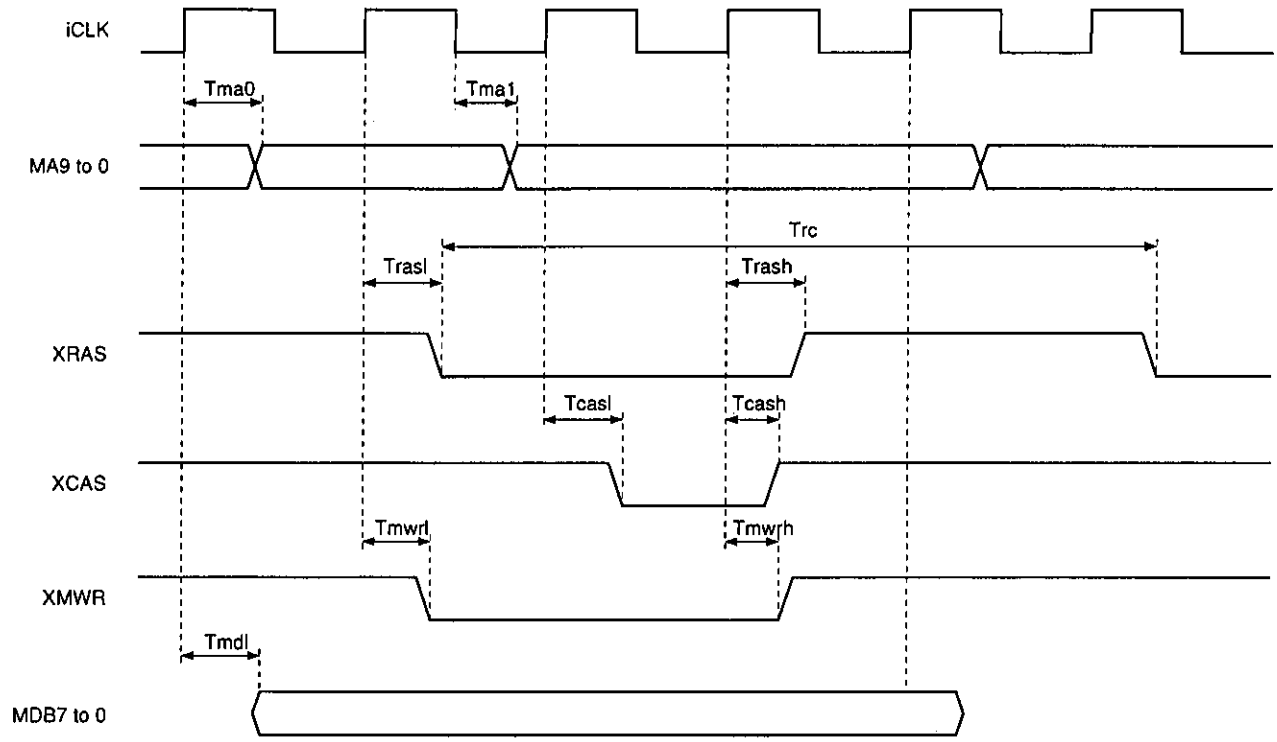
In the timing charts that follow, "iCLK" represents the IC's internal clock.

(1) Read



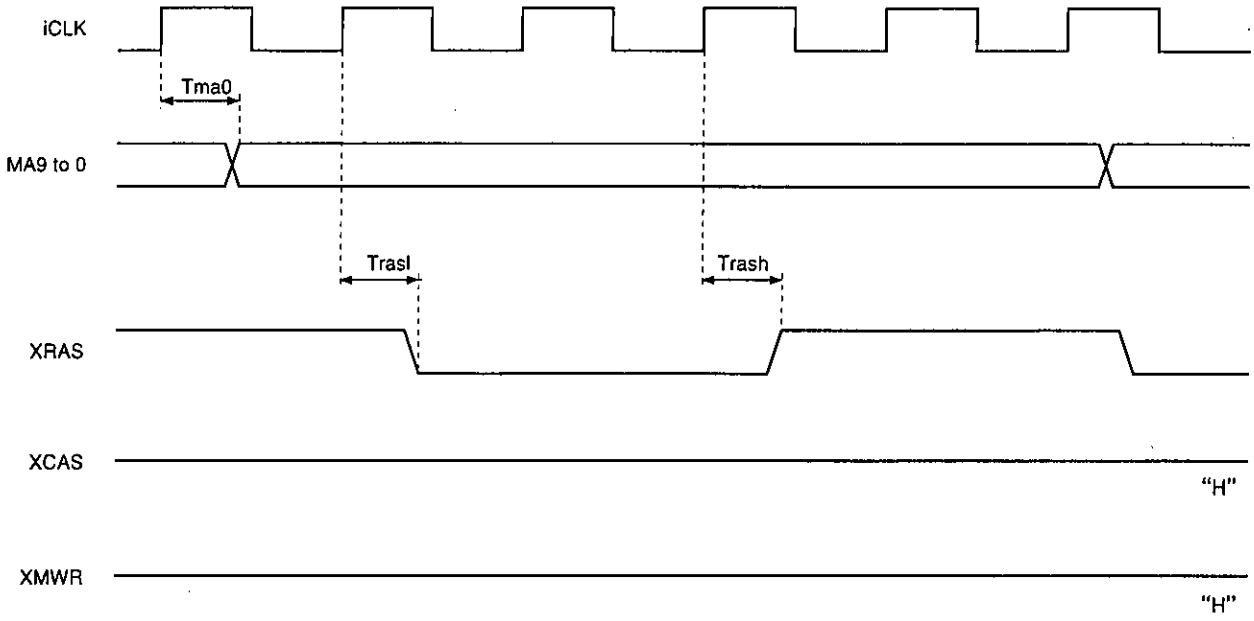
Item	Symbol	Min.	Typ.	Max.	Item
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for iCLK ↑)	Tma0		18	31	ns
Address delay time (for iCLK ↓)	Tma1		16	28	ns
XRAS ↓ delay time (for iCLK ↑)	Trasl		11	19	ns
XRAS ↑ delay time (for iCLK ↑)	Trash		15	26	ns
XCAS ↓ delay time (for iCLK ↑)	Tcasl		10	17	ns
XCAS ↑ delay time (for iCLK ↑)	Tcash		15	26	ns
Data setup time (for XCAS ↑)	Tmds		15	24	ns
Data hold time (for XCAS ↓)	Tmdh	0			ns

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for iCLK ↑)	Tma0		18	31	ns
Address delay time (for iCLK ↓)	Tma1		16	28	ns
XRAS ↓ delay time (for iCLK ↑)	Trasl		11	19	ns
XRAS ↑ delay time (for iCLK ↑)	Trash		15	26	ns
XCAS ↓ delay time (for iCLK ↑)	Tcasl		10	17	ns
XCAS ↑ delay time (for iCLK ↑)	Tcash		15	26	ns
XMWR ↓ delay time (for iCLK ↑)	Tmwrl		11	19	ns
XMWR ↑ delay time (for iCLK ↑)	Tmwrh		15	33	ns
Data delay time (for iCLK ↑)	Tmds		19	33	ns

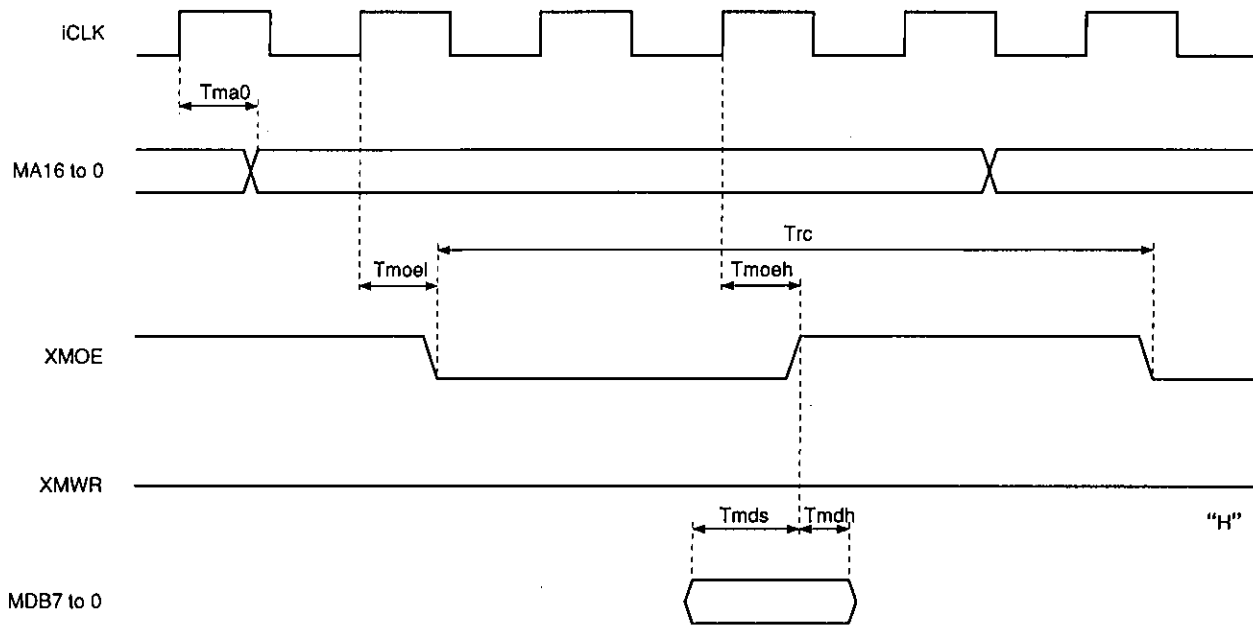
(3) Refresh (RAS only refresh)



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for iCLK ↑)	Tma0		17	29	ns
XRAS ↓ delay time (for iCLK ↑)	Trasl		10	17	ns
XRAS ↑ delay time (for iCLK ↑)	Trash		14	24	ns

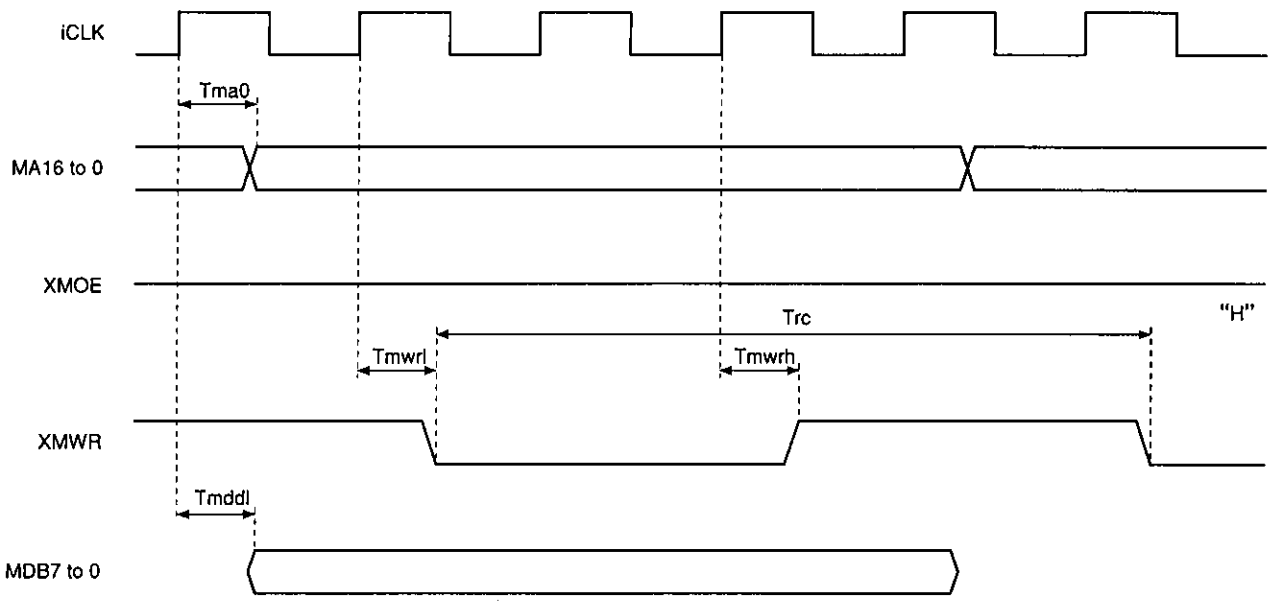
4. SRAM Interface (output Load = 30pF)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for iCLK ↑)	Tma0		18	31	ns
XMOE ↓ delay time (for iCLK ↑)	Tmoel		12	21	ns
XMOE ↑ delay time (for iCLK ↑)	Tmoeh		16	28	ns
Data setup time (for iCLK ↑)	Tmds		15	25	ns
Data hold time (for iCLK ↓)	Tmdh	0			ns

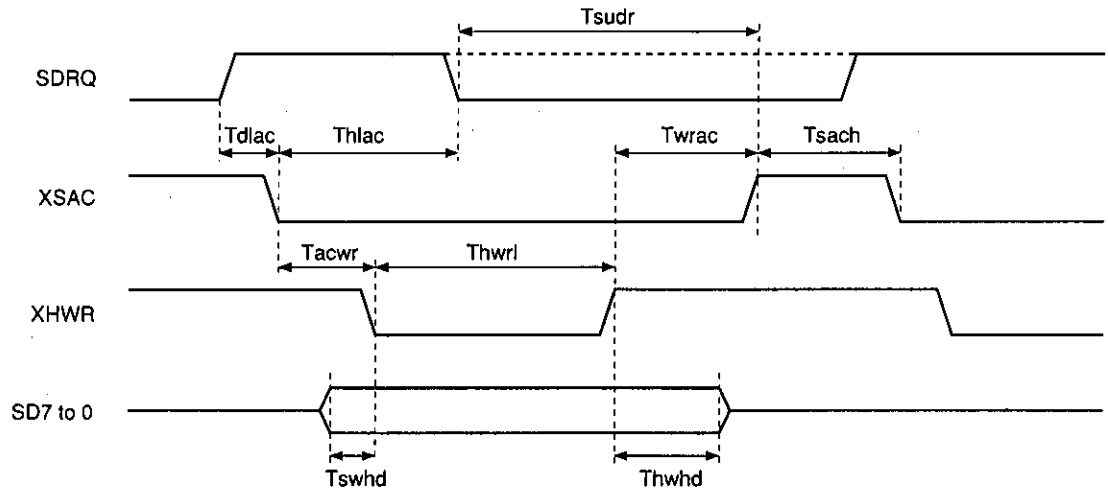
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for iCLK ↑)	Tma0		18	31	ns
XMWR ↓ delay time (for iCLK ↑)	Tmwrl		11	19	ns
XMWR ↑ delay time (for iCLK ↑)	Tmwrh		15	26	ns
Data delay time (for iCLK ↑)	Tmddl		19	33	ns

5. SCSI controller IC Interface (output Load = 30pF)

(1) To SCSI controller IC



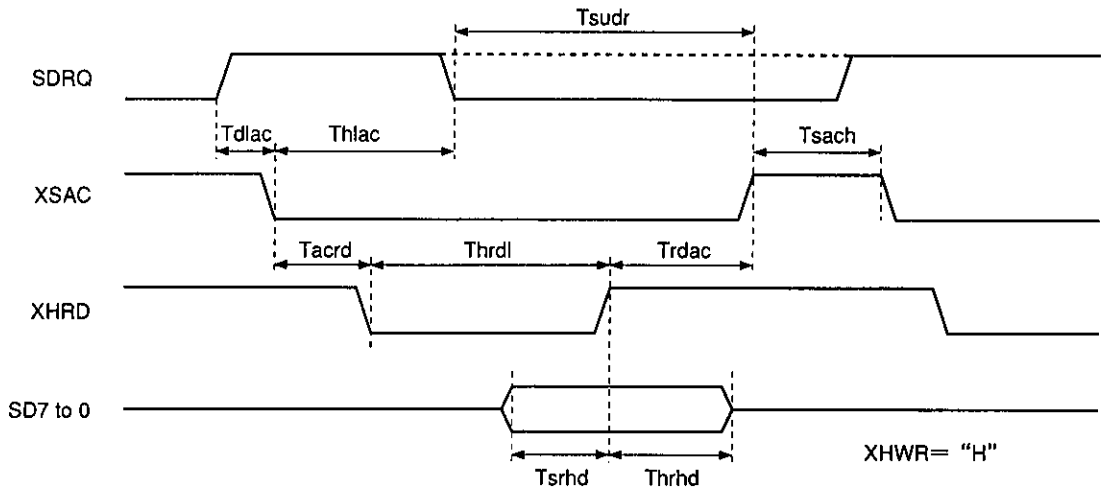
Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall delay time (for SDRQ ↑)	Tdlac	0			ns
XSAC setup time (for XSWR ↓)	Tacwr	Tw –5			ns
XSAC hold time (for XSWR ↑)	Twrac	Tw –10			ns
Data setup time (for XSWR ↓)	Tswhd	Tw –15			ns
Data hold time (for XSWR ↑)	Thwhd	Tw –15			ns
XHWR low pulse width	Thwrl	(m – 2) x Tw			ns
XSAC high pulse width	Tsach	T_1 –1			ns
SDRQ fall hold time (for XSAC ↑)	Thlac	0			ns
SDRQ fall setup time (for XSAC ↑)	Tsudr	0			ns

$$T_1 = \begin{cases} Tw\ (XFRRATE1, 0 = "L", "L") \\ (n - m) \times Tw \end{cases}$$

m: Number of cycles determined by SXFRCYC1, 0

n: Number of cycles determined by XFRRATE1, 0

(2) From SCSI controller IC



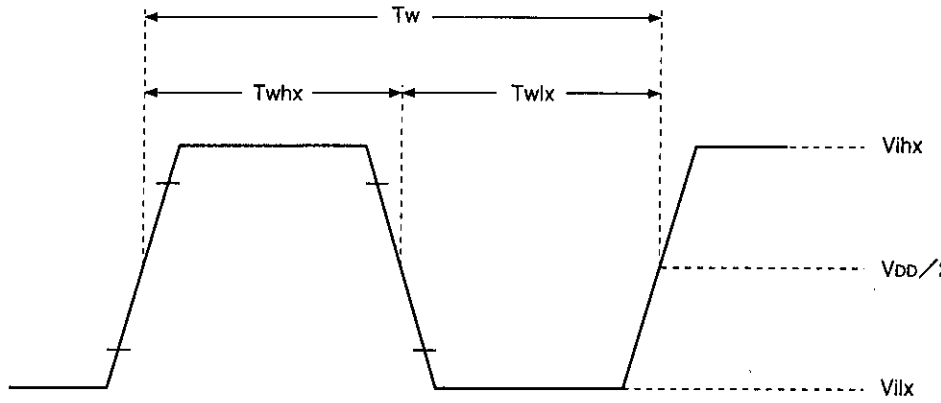
Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall delay time (for SDRQ ↑)	Tdlac	0			ns
XSAC setup time (for XHRD ↓)	Tacrd	0			ns
XSAC hold time (for XHRD ↑)	Trdac	Tw –10			ns
Data setup time (for XHRD ↑)	Tsrhd	20			ns
Data hold time (for XHRD ↑)	Thrhd	0			ns
XHRD low pulse width	Thwrl	(m –1) x Tw			ns
XSAC high pulse width	Thwrh	T_1 –1			ns
SDRQ fall hold time (for XSAC ↓)	Thlac	0			ns
SDRQ fall setup time (for XSAC ↑)	Tsudr	0			ns

7. XTL1 and XTL2 Pins

(1) When using self-excited oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	Fmax			40.0	MHz

(2) When inputting a pulse to the XTL1 pin



Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	Twhx	10			ns
Low level pulse width	Twlx	10			ns
Pulse cycle	Tw	25			ns

1. Pin Description

The pin description by function is given below.

1-1. CD player interface (11 pins)

This enables direct connection with the Sony's digital signal processor LSI for CD players. Digital signal processor LSI for CD applications are hereafter called "CD DSP".

(1) MDAT (medium DATA: input)
Serial data stream from CD DSP.

(2) BCLK (bit clock: input)
Bit clock signal; DATA signal strobe.

(3) LRCK (LR clock: input)
LR clock signal; indicates left and right channels of MDAT signals.

(4) C2PO (C2 pointer: input)
C2 pointer signal; indicates that an error is contained in MDAT input.

(5) WFCK (write frame clock: input)
Write frame clock input signal; connect to the WFCK pin (Pin 62) of the CXD2500.

(6) SCOR (subcode sync OR: input)
Subcode sync signal; connect to the SCOR pin (Pin 63) of the CXD2500.

(7) SBIN (subcode serial input: input)
Subcode serial signal; connect to the SBSO pin (Pin 64) of the CXD2500.

(8) EXCK (external clock: output)
Clock output used for reading the SBIN signal, connect to the EXCK pin (Pin 65) of the CXD2500.

(9) DATO (DATA output: output)
Serial data output to the CD DSP from the sub CPU.

(10) DSTB (data strobe: output)
DATO transfer clock output.

(11) XLAT (latch: output)
DATO latch signal. DATO is latched at the falling edge.

1-2. Buffer memory interface (28 pins)

The types of buffer memory that can be connected to this IC are shown in the table below.

Size	SRAM	DRAM	PSRAM
32KB (256Kbit)	$32K^{w} \times 8^{b}$	Not permitted	$32K^{w} \times 8^{b}$
64KB (512Kbit)	Not permitted	Not permitted	$64K^{w} \times 8^{b}$
128KB (1Mbit)	$128K^{w} \times 8^{b}$	$128K^{w} \times 8^{b}$ *1	$128K^{w} \times 8^{b}$
256KB (2Mbit)	Not permitted	$256K^{w} \times 4^{b} \times 2$ or $256K^{w} \times 8^{b}$	Not permitted
512KB (4Mbit)	Not permitted	$512K^{w} \times 8^{b}$	Not permitted

*1 CXD1806AQ can be connected to $128K^{w} \times 8^{b}$ DRAM which has 8 row addresses and 9 column addresses.

(1) DRAM (buffer memory DRAM: input)
Low is input when SRAM or PSRAM is connected as buffer memory.
High is input when DRAM is connected as buffer memory.

(2) XPS (buffer memory PSRAM: input)
High is input or leave this pin open when SRAM or DRAM is connected as buffer memory.
Low is input when PSRAM is connected as buffer memory.

(3) XMWR (buffer memory write: output)
Data write strobe negative logic output signal to buffer memory.
(4) XMOE/XCAS (buffer memory output enable/column address strobe: output)
When connected to SRAM or PSRAM, data read strobe negative logic output signal to buffer memory.
When connected to DRAM, XCAS (column address strobe negative logic) signal.
(5) MA0 to 16 (buffer memory address: output)
Address signals to buffer memory. When connected to DRAM, MA0 to 9 are valid.
(6) XRAS/XCE (row address strobe/chip enable: output)
When connected to DRAM, XRAS (row address strobe negative logic signal). When connected to PSRAM, chip enable negative logic signal.
(7) MDB0 to 7 (buffer memory data bus: input/output)
Data bus signals to buffer memory; pulled up by standard 25kΩ resistor.

1-3. Sub CPU interface (19 pins)

(1) XWR (sub CPU write: input)
Strobe negative logic signal for writing IC internal register.
(2) XRD (sub CPU read: input)
Strobe negative logic signal for reading IC internal register status.
(3) D0 to 7 (sub CPU data bus: input/output)
8-bit data bus.
(4) A0 to 5 (sub CPU address: input)
Address signal for selecting IC internal register from sub CPU.
(5) INT0 ,1 (sub CPU interrupt: output)
Interrupt request signal to sub CPU. Open drain signal. The polarity is controlled by the sub CPU.
(6) XCS (chip select: input)
Chip select negative logic signal form sub CPU.

1-4. Host interface (12 pins)

(1) XSAC (SCSI DMA acknowledge: output)
DMA acknowledge negative logic signal to SCSI controller IC.
(2) SDRQ (SCSI data request: input)
DMA data request positive logic signal from SCSI controller IC.
(3) XHWR (host write: output)
Data write strobe output to SCSI controller IC.
(4) XHRD (host read: output)
Data read strobe output to SCSI controller IC.
(5) HD0 to 7 (host data bus: input/output)
Host data bus signal.

1-5. Others (5 pins)

(1) XRST (reset: input)
Chip reset negative logic input signal.

(2) XTL1 (crystal 1: input)

(3) XTL2 (crystal 2: output)
A crystal oscillator is connected between XTL1 and XTL2. (The capacitor value depends on the crystal oscillator.)
Alternatively, a clock signal is input to the XTL1 pin.

(4) CLK (clock: output)
Outputs a clock signal with the same frequency as that of XTL1.
The output can be fixed low when this signal is not used.

(5) HCLK (half clock: output)
Outputs a clock signal with 1/2 the frequency of XTL1.
The output can be fixed low when this signal is not used.

1-6. Test pins (8 pins)

(1) TD0 to 7
Test pins for use during the manufacture of the IC. Normally, these pins are left open.

2. Sub CPU Write Registers

2-1. CONFIG0 (configuration 0) resister (address: 00HEX)

bit 7: CINTPOL (sub CPU interrupt polarity)

High: The INT0 and 1 pins become active high. When the register is inactive, they go low.

Low: The INT0 and 1 pins become active low. When the register is inactive, they go to high impedance.

bit 6: RESERVED

Normally, set low.

bits 5, 4: SXFRCYC1, 0

These bits determine the number of cycles required for data transfers between this IC and the SCSI controller IC. The sub CPU should set these bits according to the clock frequency and the AC characteristics of the SCSI controller IC.

SXFRSCY1	SXFRCY0	Number of transfer cycles
"L"	"L"	3
"L"	"H"	4
"H"	"L"	5
"H"	"H"	RESERVED

bit 3: EXCKSL (EXCK select)

This bit determines the frequency of the EXCK clock that is used to get the subcode from the CD DSP. This bit is set by the sub CPU on the basis of the clock frequency on the XTL1 pin and the playback speed. (The maximum frequency for EXCK is 1MHz.)

High: The EXCK frequency is 1/48 the frequency of the XTL1 pin. Set this bit high when the XTL1 pin frequency is greater than 32MHz.

Low: The EXCK frequency is 1/32 the frequency of the XTL1 pin. Set this bit low when the XTL1 pin frequency is 32MHz or less.

bit 2: DISCLK (disable CLK output)

High: The CLK pin is fixed low.

Low: A clock signal with the same frequency as that of the XTL1 pin is output from the CLK pin.

bit 1: DISHCLK (disable HCLK output)

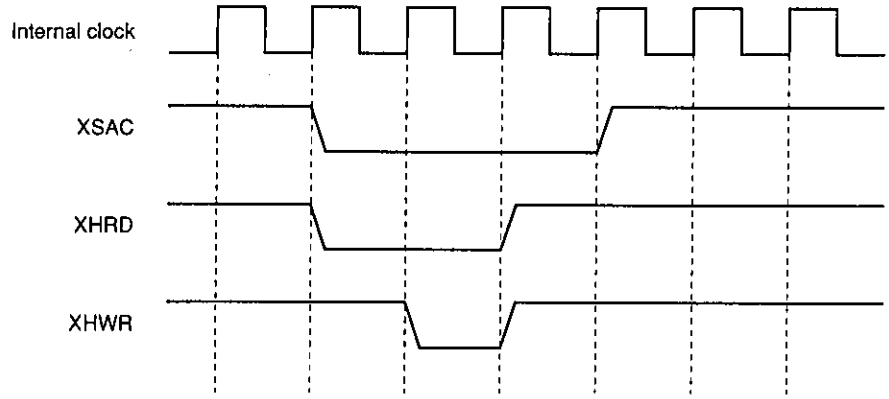
High: The HCLK pin is fixed low.

Low: A clock signal with 1/2 the frequency as that of the XTL1 pin is output from the HCLK pin.

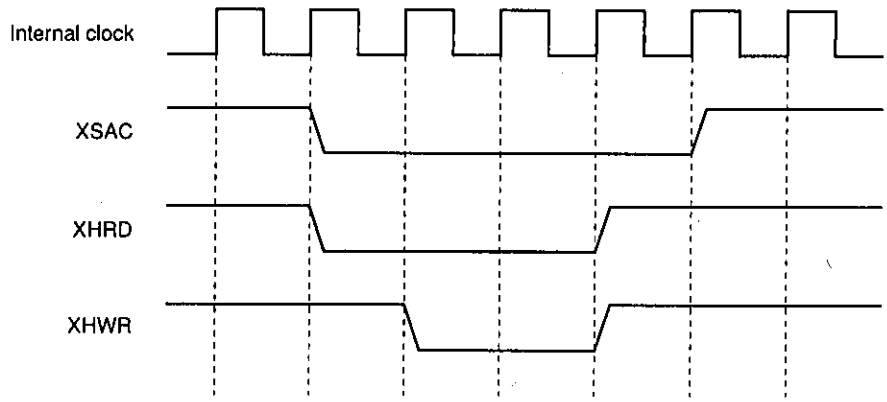
bit 0: RAMSIZE (RAM size)

Set this pin as shown in the table below according to the type of buffer memory connected.

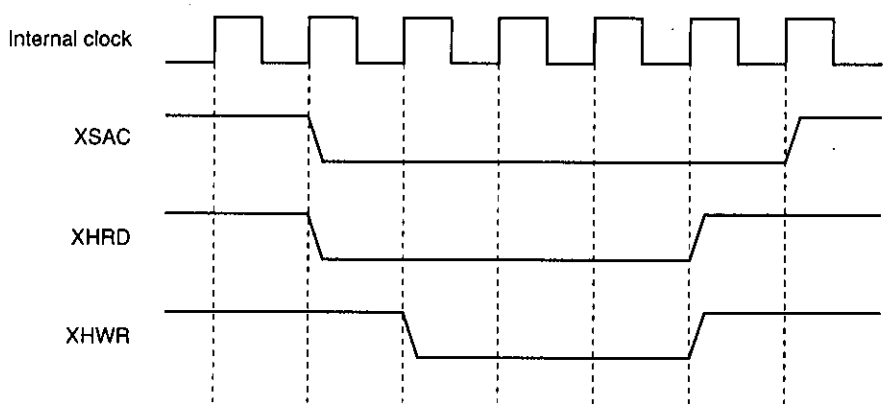
Size	Type	DRAM pin	RAMSIZE
32KB (256Kbit)	SRAM	"L'	"L"
64KB (512Kbit)	SRAM	"L"	"L"
128KB (1Mbit)	SRAM	"L"	"L"
256KB (2Mbit)	DRAM	"H"	"L"
512KB (4Mbit)	DRAM	"H"	"H"



Three-cycle mode transfer SXFRCYC [1:0] = 0



Four-cycle mode transfer SXFRCYC [1:0] = 1



Five-cycle mode transfer SXFRCYC [1:0] = 2

2-2. CONFIG1 (configuration 1) register (address: 01HEX)

bit 7: SWOPEN (sync window open)

High: The Sync mark detection window opens.

In this case, the IC's internal Sync protection circuit is disabled.

Low: The Sync mark detection window is controlled by the IC's internal Sync protection circuit.

bits 6 to 4: SYCNGC2 to 0 (SYNC NG count 2 to 0)

The Sync mark detection window opens once the number of Sync marks specified by these bits is inserted. Setting a value of 1HEX or less for these bits is prohibited. (After a reset, these bits are set to 2HEX.)

bits 3, 0: RESERVED

Normally set low.

2-3. LSTARA (last area)/LHADR (last HADRC) register (address: 02HEX)

This register specifies the last order area.

Otherwise, when host automatic transfer mode is disabled, this register specifies the upper limit for HADRC (the upper eight bits); for the subcode buffering command, this register specifies the upper limit for the address (upper eight bits).

The lower 11 bits are 7FFHEX.

When the buffer memory is used in full, the LSTARA setting values are as shown in the table below.

BFBYTEF	RAM size	LSTARAHEX
"L"	32KB	0C
"H"		0A
"L"	64KB	19
"H"		16
"L"	128KB	34
"H"		2E
"L"	256KB	69
"H"		5E
"L"	512KB	D3
"H"		BD

2-4. DRVIF (drive interface) register (address: 03HEX)

This register controls the connection mode with the CD DSP. After the IC is reset, the sub CPU sets this register according to the CD DSP to be connected.

bit 7: C2PL1ST (C2PO lower byte first)

High: When two bytes of data are input, C2PO inputs the lower byte first followed by the upper byte.

Low: When two bytes of data are input, C2PO inputs the upper byte first followed by the lower byte.

Here, "upper byte" means the upper 8 bits including MSB from the CD DSP and "lower byte" means the lower 8 bits including LSB from the CD DSP. For example, the Header minute byte is the lower byte and the second byte, the upper byte.

bit 6: LCHLOW (Lch low)

High: When LRCK is low, determined to be the left channel data.

Low: When LRCK is high, determined to be the left channel data.

bit 5: BCKRED (BCLK rising edge)

High: Data is strobed at the rising edge of BCLK.

Low: Data is strobed at the falling edge of BCLK.

bits 4, 3: BCKMD1, 0 (BCLK mode 1, 0)

These bits are set according to the number of clocks output for BCLK during one WCLK cycle by the CD digital signal processing LSI (CD DSP).

BCKMD1	BCKMD0	
"L"	"L"	Reserved
"L"	"H"	24BCLKs/WCLK
"H"	"X"	32BCLKs/WCLK

bit 2: LSB1ST (LSB first)

High: Connected with the CD DSP which outputs data with LSB first.

Low: Connected with the CD DSP which outputs data with MSB first.

bit 1: SONY 30 (SONY CDL30 Series)

High: A Sony 30 Series CD DSP is connected.

Low: A CD DSP other than a Sony 30 Series CD DSP is connected.

bit 0: RESERVED

Normally set low.

Any change of each bit in this register must be made in the decoder disable status. (After the IC is reset, the address is 28HEX.)

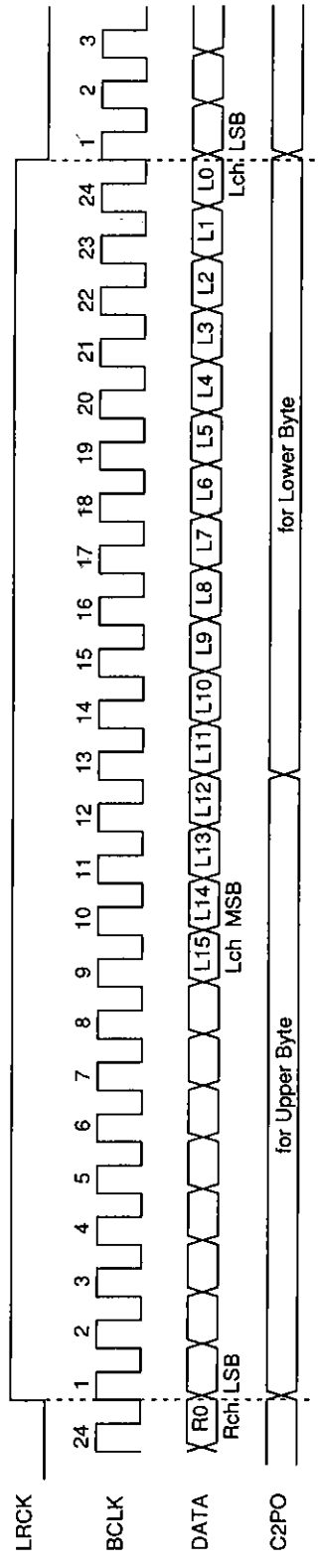


Fig. 2-4-1 (1). CDL30 and 35 Series Timing Chart

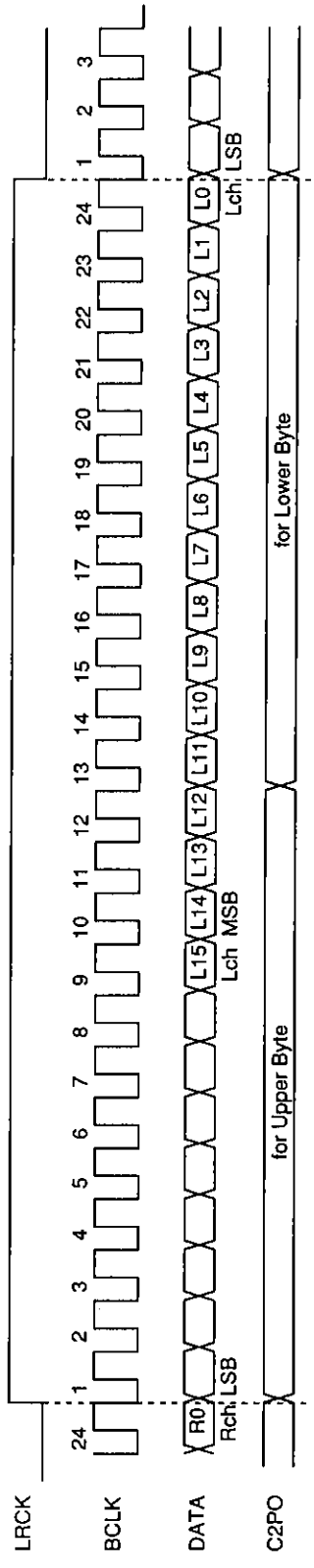


Fig. 2-4-1 (2). CDL40 Series Timing Chart (48-bit slot mode)

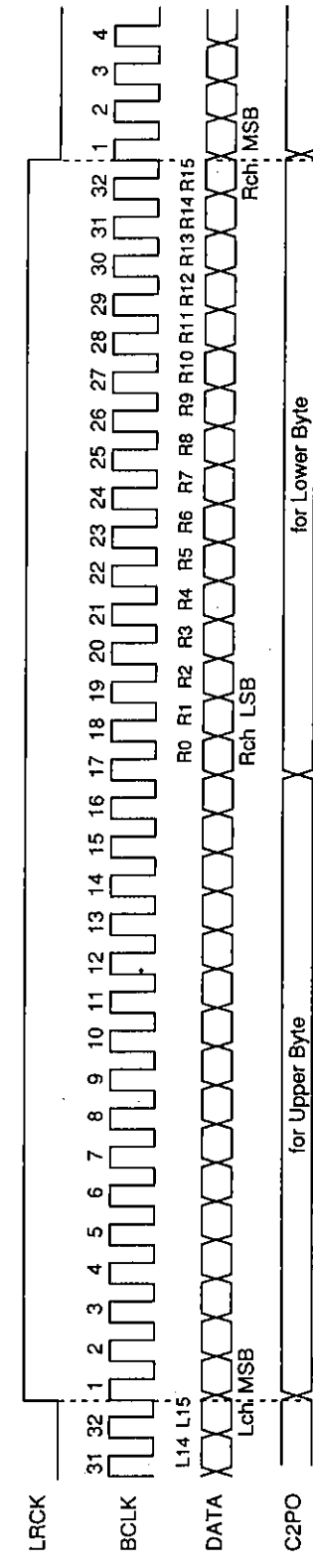


Fig. 2-4-1 (3). CDL40 Series Timing Chart (64-bit slot mode)

2-5. XFRFMT0 (transfer format 0) register (address: 04HEX)

The transfer format for automatic data transfer is determined by this register. Before starting to transfer each sector, this IC reads the value of the SCTINF register written in buffer memory. The buffer memory data is transferred to the host according to the values in the XFRFMT1 and 0 registers. The Mode/Form of bits 3 to 1 depends on the values of bits 2 and 1 in the SCTINF register. Regarding Mode2 in Yellow Book, don't care the Form2 (bit 2) of the SCTINF register. Set bits 3 to 1 of the XFRFMT0 register high to transfer 2336 bytes of user data.

bit 7: 1024XFR

When this bit is set high, the user data (2048 bytes) is divided into 1024-byte blocks for transmission. In this case, the values of bits 5 to 1 in the XFRFMT0 register and the value of the XFRFMT1 register are invalid. In other words, the Sync mark, Header, Sub Header, Parity byte, block error flag, byte error flag, and subcode cannot be sent to the host. This transfer mode is not supported for Mode2/Form2 sectors.

bit 6: 512XFR (512 bytes transfer mode)

When this bit is set high, the user data (2048 bytes) is divided into 512-byte blocks for transmission. In this case, the values of bits 5 to 1 in the XFRFMT0 register and the value of the XFRFMT1 register are invalid. In other words, the Sync mark, Header, Sub Header, and Parity bytes, as well as the block error flag, byte error flag, and subcode, cannot be sent to the host. This transfer mode is not supported for Mode2/Form2 sectors.

1024XFR and 512XFR cannot both be set high simultaneously.

bit 5: SYNC

High: Sync marks are transferred to the host.

Low: Sync marks are not transferred to the host.

bit 4: HEADER

High: The four Header bytes are transferred to the host.

Low: The four Header bytes are not transferred to the host.

bit 3: SUBHEADER

High: Mode1: This bit has no meaning.
Mode2: The eight Sub Header bytes are transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 2: USERDATA (user data)

High: Mode1 and Mode2/Form1: User data (2048 bytes) is transferred to the host.
Mode2/Form2: User data (2324 bytes) is transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 1: PARITY

High: Mode1: The EDC, ECC parity bytes and the eight 00HEX bytes, for a total of 288 bytes, are transferred to the host.
Mode2/Form1: The 280 EDC and ECC parity bytes are transferred to the host.
Mode2/Form2: The four reserved bytes (at the end of the sector) are transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 0: RESERVED

Normally set low.

Note that bits 5 to 1 should be set high for CD-DA data.

2-6. XFRFMT1 (transfer format 1) register (address: 05HEX)

bit 7: ENBLKEFL (enable block error flag)

High: The block error flag (1 byte) is transferred to the host.

Low: The byte indicated above is not transferred to the host.

bit 6: BLKEFLSL (block error flag select)

This bit is valid only when ENBLKEFL is high.

High: The value (one byte) written in the BLEFLG register by the sub CPU is transferred to the host as the block error flag.

Low: The OR value of each bit in the byte error flag is transferred to the host as the block error flag.

bit 5: ENBYTFBT (enable byte error flag buffering & transfer)

If this bit is set high, the operations described below are performed. If this bit is set low, the operations described below are not performed.

(1) The byte error flag is buffered during execution of a write-only, real-time error correction, and CD-DA command.

(2) When host automatic transfer mode is enabled (the AUTOXFR bit (bit 7) of the XFRCTL register is high), the byte error flag is transferred to the host.

The ENBYTFBT and BYTEFLSL bits are valid only when the USERDATA bit (bit 2) of the XFRFMT0 register is high.

bit 4: BYTEFLSL (byte error flag select)

This bit is valid only when ENBYTFBT is high. When this bit is set high, the value of BYTERSTS (the byte error status register, described later) is written in the byte error flag area of buffer memory. Setting the BLKEFLSL bit low and the BYTEFLSL bit high at the same time is prohibited.

If this bit is set low, either C2PO from the CD DSP or the result after error correction is written in the byte error flag area.

bit 3: ENSBQBT (enable subcode-Q buffering & transfer)

If this bit is set high, the operations described below are performed. If this bit is set low, the operations described below are not performed.

(1) The serial-parallel converted subcode-Q is buffered while the decoder executes CD-DA commands.

(2) When host automatic transfer mode is enabled (the AUTOXFR bit (bit 7) of the XFRCTL register is high), subcode-Q is transferred to the host.

bit 2: RESERVED

Normally set low.

bit 1: SBCESTS (sub code error status)

This bit is valid only when ENSBQBT is high.

High: The value (one byte) written in the SBCESTS register by the sub CPU is transferred to the host.

Low: The byte indicated above is not transferred to the host.

bit 0: ZASQEF (zero after sub-Q error flag)

This bit is valid only when ENSBQBT and SBCESTS are both high. (This bit is valid only when subcode-Q and the subcode error flag are transferred to the host.)

High: Five 00HEX bytes in addition to the sub-Q error flag are transferred to the host.

Low: Five 00HEX bytes are not added to the sub-Q error flag.

2-7. DECCTL (decoder control) register

bit 7: AUTODIST (auto distinction)

High: Errors are corrected according to the Mode byte and Form bit read from the drive.

Low: Errors are corrected according to the MODESEL and FORMSEL bits (bits 6 and 5).

bit 6: MODESEL (mode select)

bit 5: FORMSEL (form select)

When AUTODIST is low, the sector is corrected in the Mode or Form indicated below.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit 4: RESERVED

Normally set low.

bit 3: ENFM2EDC (enable Form2 EDC check)

High: EDC check for Form2 is enabled.

Low: EDC check for Form2 is disabled. The EDCNG bit of the DECSTS0 register goes low.

bit 2: MDBYTCTL (mode byte control)

High: Even if there are data other than "0" in the upper six bits of the Mode byte in the Header, an error does not result. Set this bit high when playing back discs such as CD-ROM.

Low: If the upper six bits of the Mode byte in the Header are not "000000", an error results.

bit 1: ENDLA (enable drive last area (address))

High: DLAR (Drive Last Area) is enabled. While the decoder is executing a write-only command, a real-time error correction command, or a CD-DA command, if buffering of the AREA in buffer memory specified by DLAR is completed, the DRVOVRN (Drive Overrun) status results. Buffer-write of subsequent sectors is then interrupted.

Low: DLAR (drive last area) is disabled when this is set low.

bit 0: ATDLRNEW (auto DLARA renewal)

High: When the data transfer to the host is completed for one sector, DLARA is renewed in the written area of the sector.

Low: DLARA is updated by the sub CPU.

2-8. DECCTL1 (decoder control 1) register (address: 07HEX)

bit 7: ENSBQRD (enable subcode-Q read)

The subcode is fetched from the DSP and the subcode Q CRC check is performed. The sub CPU can read the subcode Q from the SUBQ register.

bit 6: RESERVED

Set the same value as is set for the ENSBQRD bit.

bits 5 to 3: DECCMD2 to 0 (decoder command 2 to 0)

DECCMD2	DECCMD1	DECCMD0	Decoder command
"L"	"L"	"L"	Decoder disable
"L"	"L"	"H"	Monitor-only
"L"	"H"	"L"	Write-only
"L"	"H"	"H"	Real-time-correction
"H"	"L"	"H"	RESERVED
"H"	"H"	"H"	CD-DA

bit 2 to 0: RESERVED

Normally set low.

2-9. XFRCLT0 (transfer control 0) register (address: 08HEX)

bit 7: AUTOXFR (auto transfer)

High: Host automatic transfer mode (described later) is enabled.

Low: Host automatic transfer mode is disabled. Transfers to the host are accomplished by setting HADRC and HXFRC.

bit 6: RESERVED

Set this bit high when HMDS is low.

bits 5, 4, 1: RESERVED

Normally set low.

bit 3: CPUDMAEN (sub CPU DMA enable)

Setting this bit high enables sub CPU buffer memory access. The sub CPU sets this bit high after setting the buffer access head address in CADRC.

bit 2: CPUSRC (sub CPU source)

High: Data is transferred from the sub CPU to the buffer memory.

Low: Data is transferred from the buffer memory to the sub CPU.

bit 0: HSTSRC (host source)

High: Data is transferred from the host to the buffer memory.

Low: Data is transferred from the buffer memory to the host.

This bit is valid when host automatic transfer mode is enabled (the AUTOXFR bit (bit 7) of the XFRCTL register is high).

2-10. XFRCTL1 (transfer control 0) register (address: 09HEX)

bits 7 to 5: RESERVED

Normally set low.

bit 4: HSTXFREN (host transfer enable)

When this bit is set high, transfer with the host buffer memory begins. This bit is automatically reset low when the transfer is completed. In addition, a transfer can be forcibly terminated by setting this bit low.

bits 3 to 0: RESERVED

Normally set low.

2-11. DSPCTL (DSP control) register (address: 0BHEX)

bits 7, 6: DSTBSL1, 0

These bits determine the frequency of the DSTB and XLAT clocks used for passing data (DATO) to the CD DSP. The sub CPU sets this bit according to the frequency of the clock on the XTL1 pin. (The maximum frequency for DSTB is 1MHz.)

DSTBDL1	DSTBDL0	Frequency
0	0	1/24 of XTL1
0	1	1/32 of XTL1
1	0	1/48 of XTL1
1	1	1/64 of XTL1

bit 5: DISXLAT (disable XLAT output)

High: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is not output from the XLAT pin. In this case, the sub CPU uses DSPCMDLT (bit 0 of the CHPCTL0 register) to output a latch pulse from the XLAT pin at the appropriate time.

Low: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is output from the XLAT pin.

bits 4, 3: XFRBYT1, 0 (transfer command byte length)

These bits determine the number of bytes in the command data (DSPCMD register) to be sent to the CD DSP. The relationship between the settings and the number of bytes is shown in the following table.

XFRBYT1	XFRBYT0	Number of bytes
"L"	"L"	Prohibited
"L"	"H"	1
"H"	"L"	2
"H"	"H"	3

bits 2 to 0: RESERVED

Normally set low.

2-12. CHPCTL0 (chip control 0) register (address: 0CHEX)

bit 7: CHIPRST (chip reset)

This IC is reset when this bit is set high.

bit 6: TGTMET (target met)

(1) During execution of a write-only or a real-time error correction command, if the target sector is found, the sub CPU sets TGTMET high.

(2) TGTMET is sampled 3/4 sectors (depends on playback speed) after the decoder interrupt. Accordingly, if the target sector is found, the sub CPU must set TGTMET high within this interval after DECINT.

(3) Once TGTMET is set high, it remains high until the decoder is disabled within the IC.

(4) If TGTMET is sampled and found to be low during execution of a write-only or a real-time error correction command:

- The main data and subcode buffering areas are not renewed.
- Main data error correction is not performed.

bit 5: INCTGT (increment target register)

If this bit is set high, the target registers (TGTMIN, TGTSEC, and TGTBLK) are incremented. The target registers use BCD code.

TGTMIN, TGTSEC, and TGTBLK are connected in cascading fashion and are incremented as shown below.

(1) The TGTBLK register is always incremented by this bit. When the TGTBLK register is incremented after reaching "74", it returns to "0".

(2) The TGTSEC register is incremented when the TGTBLK register is "74" and this bit goes high. When the TGTSEC register is incremented after reaching "59", it returns to "0".

(3) The TGTMIN register is incremented when the TGTBLK register is "74", the TGTSEC register is "59", and this bit goes high. When the TGTMIN register is incremented after reaching "99", it returns to "0".

bit 4: RPCORTRG (repeat correction trigger)

If this bit is set high while the decoder is disabled, CD-ROM sector error correction begins. The sector that is corrected is specified by the BFARA# register.

bit 0: RESERVED

Normally set low.

bit 2: CLDSPCMD (clear DSP DATA register)

Setting this bit high clears the DSPCMD register.

bit 1: DSPCMDXF (DSP command transfer)

Setting this bit high starts serial transfer of the contents of the DSPCMD register to the CD DSP.

bit 0: DSPCMDLT (DSP command latch)

Setting this bit high outputs a pulse from the XLAT pin.

2-13. CPUBWDT (CPU buffer write data) register (address: 0DHEX)

The sub CPU writes the data to be written in the buffer memory in this register.

2-14. DSPCMD (DSP command) register (address: 0EHEX)

The data to be serially transferred to the CD DSP is written in this register. This register is a three-byte LIFO (last-in, first-out) register.

2-15. SCTINF (sector information) (address: 10HEX)

When DECINT is active, the current sector information is written in this register. When making transfers to the host automatically, be sure to set the information in this register each time DECINT is active. The value in this register is written in the last address in the buffer memory area.

bits 7 to 3: RESERVED

Normally set low.

bit 2: Mode2

High: This sector is a Mode2 sector.

Low: This sector is a Mode1 or CD-DA sector.

bit 1: Form2

This bit is valid only when the Mode2 bit is high.

High: This sector is a Form2 sector.

Low: This sector is a Form1 sector.

This bit can be either high or low in the Mode2 for the Yellow Book.

MODE2	FORM2	
"L"	"L"	MODE1
"L"	"H"	RESERVED
"H"	"L"	MODE2/FORM1
"H"	"H"	MODE2/FORM2

bit 0: XFRSCT (transfer sector)

High: The data in this sector is transferred to the host.

Low: The data in this sector is not transferred to the host. In this case, bits 2 and 1 have no meaning.

2-16. BLKESTS (block error status) register (address: 11HEX)

The data to be transferred to the host as the block error status byte is written in this register. Set this register before writing the SCTINF register.

2-17. SBCESTS (subcode error status) register (address: 12HEX)

The data to be transferred to the host as the subcode error status byte is written in this register.
Set this register before writing the SCTINF register.

2-18. INCBLKS (increment blocks) (address: 13HEX)

bits 7 to 3: RESERVED

Normally set low.

bits 2 to 0: INCBLKS2

This register specifies the increment value (+1 to 4) of the BFBLKC (buffer block count) register. Setting "0" or a value of "5" or greater is prohibited. After a reset, the increment value is set to "1".

2-19. BYTERSTS (byte error status) register (address: 14HEX)

When ENBYTFBT and ENBYTEFG in the XFRFMT1 register are both high, the data to be transferred to the host as the byte error status byte is written in this register. Set this register before writing the SCTINF register.

2-20. CHPCTL1 (chip control 1) register (address: 15HEX)

bit 7: BURSTXFR (burst transfer)

High: Data transfer to the SCSI controller IC is performed in burst mode.

Low: Data transfer to the SCSI controller IC is performed in single mode.

bits 6, 5: XFRRATE1, 0 (transfer rate 1, 0)

These bits are used to limit the data transfer speed during data transfers with the SCSI controller IC.

XFRRATE1	XFRRATE0	
"H"	"H"	Limit the SDRQ reception interval to eight times the XTL1 cycle or more.
"H"	"L"	Limit the SDRQ reception interval to seven times the XTL1 cycle or more.
"L"	"H"	Limit the SDRQ reception interval to six times the XTL1 cycle or more.
"L"	"L"	Do not limit the SDRQ reception interval.

bits 4, 3: RFRSCTL1, 0 (refresh control 1, 0)

These bits are used to control the refresh interval when this IC is connected to DRAM. Set these bits in accordance with the XTL1 clock frequency. The refresh interval is designed to be 8ms. In addition, this IC performs RAS-only refresh. Don't care the settings of these bits when this IC is connected to SRAM.

RFRSCTL1	RFRSCTL0	
"L"	"L"	XTL1 frequency is less than 24MHz.
"L"	"H"	XTL1 frequency is 24MHz or more.
"H"	"L"	XTL1 frequency is 32MHz or more.
"H"	"H"	XTL1 frequency is 33.8688MHz or more.

bits 2, 0: RESERVED

Normally set low.

2-21. TGTMIN (target minute) register (address: 17HEX)

0 to 99

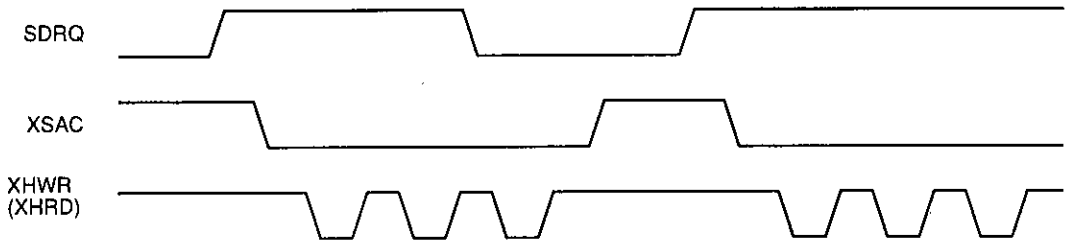
2-22. TGTSEC (target second) register (address: 18HEX)

0 to 59

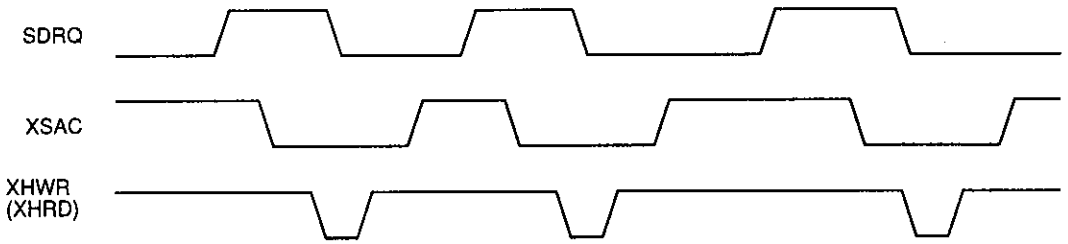
2-23. TGTBLK (target block) register (address: 19HEX)

0 to 74

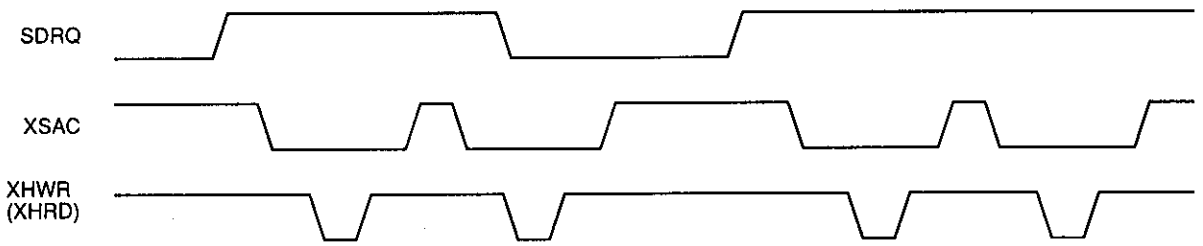
Set the target sector address in these three registers when executing a monitor-only, write-only, or real-time error correction command. This address is compared with the current sector address, and if they are not matched, TGTNTMT (target not met) status (bit 0 of the DECSTS0 register) is established.



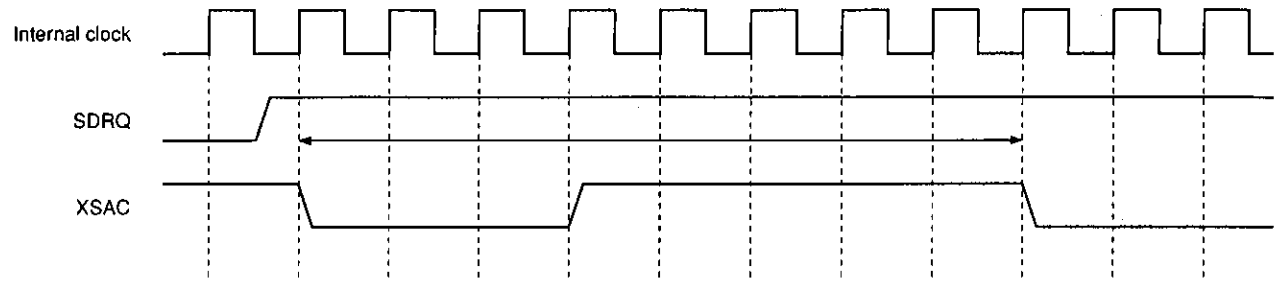
Burst mode transfer



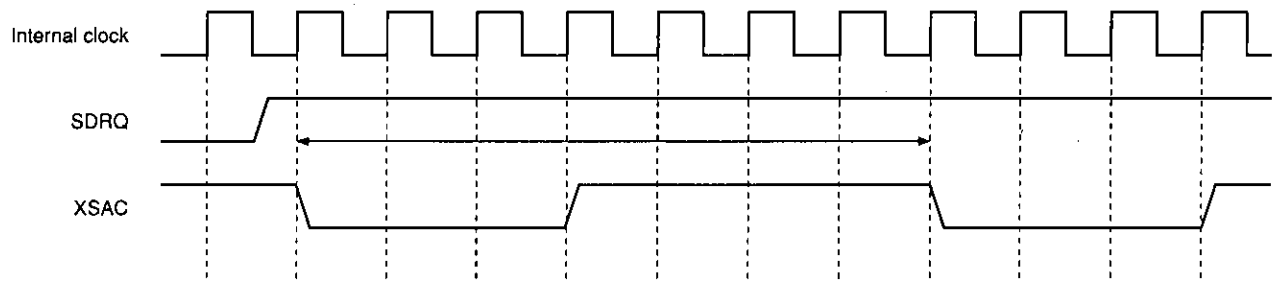
Single mode transfer (1)



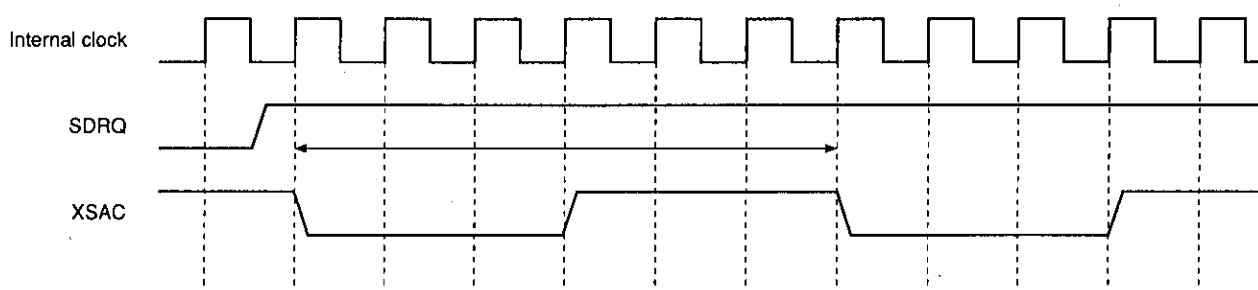
Single mode transfer (2)



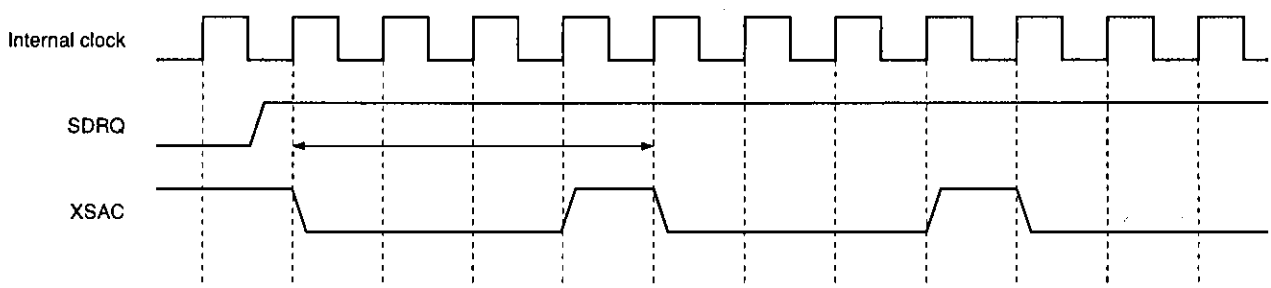
XFRRATE [1:0] = 3



XFRRATE [1:0] = 2



XFRRATE [1:0] = 1



XFRRATE [1:0] = 1

2-24. XFRCNT-H, M, L (transfer block counter-high, middle, low) register (address: 1B to 1DHEX)

This is a 24-bit register that shows the number of blocks remaining to be transferred. Before the start of the transfer the sub CPU sets the total number of blocks to be transferred in this register.

This register is decremented as the transfer of each block is completed.

The sub CPU can read the value of XFRCNT at any time. However, because the reads by the sub CPU are not synchronized with the variation of XFRCNT, note that there is a possibility of an error of ±1 between the value that is read and the actual value.

The sub CPU can read the value of XFRARA, XFRPOS, BFBLKC, or XFRCNT at any time. However, because the reads by the sub CPU are not synchronized with the variation of BFBLKC, note that there is a possibility of an error of ±1 between the value that is read and the actual value.

2-25. BFARA# (buffering area number) register (address: 1EHEX)

This register indicates the buffering area when executing a write-only, real-time error correction, or CD-DA command. Before executing one of these commands, the sub CPU specifies the area where buffering is to start initially. When the buffering of a sector is completed, this register is incremented.

When executing a subcode buffering command, buffering starts from address 0.

2-26. DLARA (drive last area) register (address: 1FHEX)

This register specifies the last buffering area while the decoder is executing a write-only, real-time error correction, or CD-DA command. If the ENDLA bit (bit 1) of the DECCTL0 register is set high and the data from the drive (CD DSP) is written in the area specified by DLARA while the decoder is executing one of the above commands, subsequent buffering is prohibited.

2-27. XFRARA (transfer area) register (address: 20HEX)

During an automatic transfer, this register specifies the initial area from which the transfer is to start. This register is incremented after a block is transferred.

2-28. XFRPOS (first transfer position) register (address: 21HEX)

bits 1, 0: XFRPOS1, 0

These bits specify the initial block position from which transfer is to start when in 512- or 1024-byte transfer mode (automatic transfer mode). In 1024-byte transfer mode, XFRPOS1 is invalid. This register is incremented after a block is transferred.

2-29. HXFRC-H, M, L (host transfer counter - high, middle, low) registers (addresses: 23 to 25HEX)

In manual transfer mode, these registers set the number of bytes to be transferred. (20 bits)

2-30. HADRC-H, M, L (host address counter - high, middle, low) registers (addresses: 27 to 29HEX)

In manual transfer mode, these registers set the head address from which the transfer begins.

2-31. CADRC-H, M, L (sub CPU address counter - high, middle, low) registers (addresses: 2F to 31HEX)

The sub CPU sets this address when accessing buffer memory. This address is incremented when data is either read from or written to the buffer memory.

2-32. CLRINT0 (clear interrupt status 0) register (address: 32HEX)

When each bit of this register is set high, the corresponding interrupt status is cleared. The bit concerned is automatically set low after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset low.

bit 7: DECINT (decoder interrupt)
bit 6: DECTOUT (decoder time out)
bit 5: DRVOVRN (drive overrun)
bit 4: SUBCSYNC (Subcode Sync)
bits 3 to 0: RESERVED
Normally set low.

2-33. CLRINT1 (clear interrupt status 1) register (address: 33HEX)

When each bit of this register is set high, the corresponding interrupt status is cleared. The bit concerned is automatically set low after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset low.

bits 7 to 2: RESERVED
Normally set low.
bit 1: XFRSTOP (transfer stop)
bit 0: BLXFRCMP (block transfer complete)

2-34. INTEN0 (interrupt enable 0) register (address: 34HEX)

Setting each bit in this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT0 pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bit 7: DECINT (decoder interrupt)
bit 6: DECTOUT (decoder time out)
bit 5: DRVDVRN (drive overrun)
bit 4: SUBCSYNC (subcode sync)
bits 3 to 0: RESERVED
Normally set low.

2-35. INTEN1 (interrupt enable 1) register (address: 35HEX)

Setting each bit in this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT0 pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bits 7 to 2: RESERVED
Normally set low.
bit 1: XFRSTOP (transfer stop)
bit 0: BLXFRCMP (block transfer complete)

2-36. BFBLKC-H, L (buffer block count-high, low) registers (addresses: 36 and 37HEX)

This register is a 10-bit counter that indicates the number of blocks in the buffer that can be transferred. Before the start of the transfer, the sub CPU sets the number of blocks that can be transferred.

Once the number of transferable blocks is reached (once the buffer is written with XFRSCT (bit 0) of the SCTINF register high), the value of BFBLKC is incremented (+1 to 4). The increment value is specified by the INCBLKS register.

When the transfer of one block is completed, this register is decremented (–1).

3. Sub CPU Read Registers

Descriptions that are identical with those for the write registers are omitted here.

3-1. RAWHDR (raw header) register (address: 00HEX)

The Header byte for the sector being sent from the CD DSP while DECINT is active can be read from this register.

3-2. BFHDR (buffer header) register (address: 02HEX)

During the execution of a write-only or a real-time error correction command and after execution of a repeat correction command, the Header byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

3-3. BFSHDR (buffer sub header) register (address: 03HEX)

During the execution of a write-only or a real-time error correction command and after execution of a repeat correction command, the Sub Header byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

3-4. RAWHDRFLG (raw header flag) register (address: 04HEX)

This register indicates the C2PO value for the RAWHDR register.

bit7	Minute
bit6	Second
bit5	Block
bit4	Mode
bit3 to 0	RESERVED

3-5. BFHDRFLG (buffer header flag) (address: 05HEX)

This register shows the error status of each byte in the BFHDR and BFSHDR registers. High means an error.

bit7	Minute
bit6	Second
bit5	Block
bit4	Mode
bit3	File
bit2	Channel
bit1	Submode
bit0	Data Type

3-6. DECSTS0 (decoder status 0) register (address: 06HEX)

bit 7: SHRTSCT (short sector)

Indicates that the Sync mark interval was less than 2351 bytes. This sector does not remain in the buffer memory.

bit 6: NOSYNC

Indicates that the Sync mark was inserted because one was not detected in the prescribed position.

bit 5: CORINH (correction inhibit)

This is high if the current sector Mode and Form could not be determined when the AUTODIST bit of the DECCTL register is set high. ECC or EDC is not executed in this sector. The CORINH bit is invalid when AUTODIST is set low. It is high in any of the conditions below when the AUTODIST bit is set high.

(1) When an error was found in the Mode byte.
(2) When the Mode byte is a value other than 01HEX or 02HEX.
(3) When the Mode byte is 02HEX and the C2 pointer is high in the Submode byte.

bit 4: ERINBLK (erasure in block)

(1) When the decoder is operating in the monitor-only, write-only or real-time mode which prohibits erasure correction, this indicates that at least a 1-byte error flag (C2PO) has been raised in the data excluding the Sync mark from the current sector CD DSP.
(2) When the decoder is operating in the real-time correction mode which performs erasure correction, this indicates that at least a 1-byte error flag (MDBP) has been raised in the data excluding the Sync mark from the current sector CD DSP.

bit 3: CORDONE (correction done)

Indicates that there is an error corrected byte in the current sector.

bit 2: EDCNG

Indicates that an error was found in the current sector through an EDC check.

bit 1: ECCNG

Indicates that an uncorrectable error was found somewhere between the Header byte and the Parity byte in the current sector. (Bit 1 = don't care in the Mode2, Form2 sectors.)

bit 0: TGTNTMET (target not met)

Indicates that the current sector address and the target address in the TGTMNT, TGTSEC, and TGTBLK registers do not match. The error pointer is not referenced in this instance.

3-7. DECSTS1 (decoder status 1) register (address: 07HEX)

bits 7 to 3: RESERVED

bit 2: EDCALL0 (EDC ALL 0)

This is high when there are no error flags in all the 4 EDC parity bytes of the current sector and their values are all 00H.

bit 1: CMODE (correction mode)

bit 0: CFORM (correction form)

Indicates the Mode and Form of the current sector the decoder has discriminated to correct errors when the decoder is operating in the real-time correction or repeat correction mode.

CFORM	CMODE	
"X"	"L"	MODE1
"L"	"H"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

3-8. XFRSTS (data transfer status) register (address: 08HEX)

bits 7 to 2: RESERVED

bit 1: CBFWRRDY (sub CPU buffer write ready)
The sub CPU can write in the CPUBWDT register when this bit is high.

bit 0: CBFRDRDY (sub CPU buffer read ready)
The sub CPU can read the CPUBRDT register when this bit is high.

3-9. DSPSTS (DSP status) register (address: 0BHEX)

bits 7 to 5: REV# (revision number) 2 to 0
001HEX is read.

bits 4 to 1: RESERVED

bit 0: CMDOBUSY (command output busy)
This bit goes high if DSPCMDXFR is set. Once the transfer of the contents of the DSPCMD register to the CD DSP is completed, this bit goes low.

3-10. CPUBRDT (CPU buffer read data) register (address: 0DHEX)

The sub CPU reads the data in the buffer memory through this register.

3-11. SBQSTS (subcode-Q status) register (address: 11HEX)

This register indicates the error status of the subcode-Q fetched from the CD DSP. The data in this register is valid from SBCSYNC to SBCSYNC.

bits 7 to 3: RESERVED

bit 2: SHTSBCS1 (short subcode sector 1)
Indicates that the subcode Sync mark interval since the previous SBCSYNC interrupt was less than 98 WFCK.

bit 1: NOSYNC1
Indicates that since a subcode Sync mark could not be detected at the prescribed position, a Sync mark was inserted.

bit 0: SUBQERR1 (subcode-Q error 1)
An error was detected in the subcode-Q as a result of the CRC check.

3-12. SBQDT (subcode-Q DATA) register (address: 12HEX)

The subcode-Q value can be read by reading this register ten times. The subcode-Q that is read is the data immediately prior to the SBCSYNC interrupt.

3-13. CSCTARA (current sector area) register (address: 13HEX)

This register indicates the area number where the current sector is being written.

3-14. CHPCTL1 (chip control 1) register (address: 15HEX)

The values written in bits 7 to 2 in the write register CHPCTL1 can be read as is.

3-15. TGTMNT (target minute) register (address: 17HEX)

3-16. TGTSEC (target second) register (address: 18HEX)

3-17. TGTBLK (target block) register (address: 19HEX)

3-18. XFRCNT-H, M, L (transfer block counter-high, middle, low) register (address: 1B to 1DHEX)

3-19. BFARA# (buffering area number) register (address: 1EHEX)

3-20. DLADR (drive last address) register (address: 1FHEX)

3-21. XFRARA (transfer area) register (address: 20HEX)

3-22. XFRPOS (first transfer position) register (address: 21HEX)

3-23. HXFRC-H, M, L (host transfer counter-high, middle, low) register (address: 23 to 25HEX)

3-24. HADRC-H, M, L (host address counter-high, middle, low) register (address: 27 to 29HEX)

3-25. SLDR-H, M, L (subcode last address-high, middle, low) register (address: 2B to 2DHEX)

3-26. SADRC-H, M, L (subcode address counter-high, middle, low) register (address: 2F to 31HEX)
The buffer address can be read in the subcode buffering command.

3-27. INTSTS0 (interrupt status 0) register (address: 32HEX)
The value of each bit in this register indicates that of the corresponding interrupt status. These bits are not affected by the values of the INTEN0 register bits.

bit 7: DECINT (decoder interrupt)
This interrupt is generated while the decoder is executing a command.
(1) During execution of a write-only, monitor-only, or real-time error correction command:
If the Header byte is received from the CD DSP when a Sync mark was detected or inserted, the DECINT status is generated. However, while the Sync mark detection window is open, the DECINT status is not established if the Sync mark interval is less than 2352 bytes.
(2) During repeat correction execution:
The DECINT status is established each time one correction is completed.
(3) During CD-DA command execution:
The DECINT status is established each time 2352 bytes of data are written.
(4) During subcode buffering execution:
The DECINT status is established when the subcode for one sector is written in the buffer.

bit 6: DECTOUT (decoder time out)
The DECTOUT status is established when the Sync mark is not detected even after the time it takes to search 3 sectors (40.6ms at normal-speed playback) has elapsed after the decoder has been set to the monitor-only, write-only or real-time correction mode.

bit 5: DRVOVRN (drive overrun)
While the decoder is executing a write-only, real-time correction, or CD-DA command, if buffering in the area specified by DLARA is completed, the DRVOVRN status results.

bit 4: SUBCSYNC (subcode sync)
If a subcode Sync mark is detected or inserted while subcode fetching is enabled, the SUBCSYNC status results.
Note that if the SUBCSYNC interrupt is not cleared within 95 WFCK cycles, the SUBCSYNC status is not established the next time a subcode Sync mark is detected or inserted. In this event, the subcode-Q read from the SBQDT register is also not renewed.

bits 3 to 0: RESERVED

3-28. INTSTS1 (interrupt status) register (address: 33HEX)

The value of each bit in this register indicates that of the corresponding interrupt status. These bits are not affected by the values of the INTEN1 register bits.

bits 7 to 2: RESERVED

bit 1: XFRSTOP (transfer stop)

If transfer to the host is stopped while host automatic transfer mode is enabled because the value of the BFBLKC register or XFRCNT register is "0", the XFRSTOP status is established.

bit 0: BLXFRCMP (block transfer complete)

When host automatic transfer mode is enabled, the BLXFRCMP status is established when the transfer of one block is completed. However, if the XFRSTOP status was established by the completion of a block transfer, the BLXFRCMP status is not established. When host automatic transfer mode is disabled, the BLXFRCMP status is established when transfer to the host by HXFRC is completed.

3-29. INTEN0 (interrupt enable 0) register (address: 34HEX)

The value written in the INTEN0 register can be read as is.

3-30. INTEN1 (interrupt enable 1) register (address: 35HEX)

The value written in the INTEN1 register can be read as is.

3-31. BFBLKC-H, L (buffer block count-high, low) register (addresses: 36 and 37HEX)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CONFIG0	00	CINT POL	"L"	SXFR CYC1	SXFR CYC0	EXCK SL	DIS CLK	DIS HCLK	RAM SIZE
CONFIG1	01	SW OPEN	SYC NGC2	SYC NGC1	SYC NGC0	"L"	"L"	"L"	"L"
LSTARA /LHADR	02	b7	b6	b5	b4	b3	b2	b1	b0
DRVIF	03	C2PO L 1st	LCH LOW	BCK RED	BCKL MD1	BCKL MD0	LSB 1st	"L"	"L"
XFRFMT0	04	1024 XFR	512 XFR	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	"L"
XFRFMT1	05	BLKE FLAG	BLKE FLSL	ENBY TFBT	BYTE FLSL	ENSB CBT	"L"	SBCE STS	ZASQ EF
DECCTL0	06	AUTO DIST	MODE SEL	FORM SEL	"L"	ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW
DECCTL1	07	ENSB QRD	ENSB CDEC	DEC CMD2	DEC CMD1	DEC CMD0	"L"	"L"	"L"
XFRCTL0	08	AUTO XFR	"H"	"L"	"L"	CPUD MAEN	CPU SRC	"L"	HST SRC
XFRCTL1	09	"L"	"L"	"L"	HSTX FREN	"L"	"L"	"L"	"L"
	0A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
DSPCTL	0B	DSTB SL1	DSTB SL0	DIS XLAT	XFR BYT1	XFR BYT0	"L"	"L"	"L"
CHPCTL0	0C	CHIP RST	TGT MET	INC TGT	RPCO RTRG	CLR RSLT	CLDS PCMD	DSPC MDXF	DSPC MDLT
CPUBW DT	0D	b7	b6	b5	b4	b3	b2	b1	b0
DSPCMD	0E	b7	b6	b5	b4	b3	b2	b1	b0
	0F	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
SCTINF	10	"L"	"L"	"L"	"L"	"L"	MODE 2	FORM 2	XFR SCT
BLKE STS	11	b7	b6	b5	b4	b3	b2	b1	b0
SBCE STS	12	b7	b6	b5	b4	b3	b2	b1	b0
INC BLKS	13	"L"	"L"	"L"	"L"	"L"	INCB LKS2	INCB LKS1	INCB LKS0
BYTER STS	14	b7	b6	b5	b4	b3	b2	b1	b0
CHPCTL1	15	BURS TXFR	XFRR ATE1	XFRR ATE0	RFRS CTL1	RFRS CTL0	"L"	"L"	"L"
	16	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"

Sub CPU write registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TGTMNT	17	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	18	b7	b6	b5	b4	b3	b2	b1	b0
TGTBLK	19	b7	b6	b5	b4	b3	b2	b1	b0
	1A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
XFRCNT -H	1B	b23	b22	b21	b20	b19	b18	b17	b16
XFRCNT -M	1C	b15	b14	b13	b12	b11	b10	b9	b8
XFRCNT -L	1D	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	1E	b7	b6	b5	b4	b3	b2	b1	b0
DLARA	1F	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	20	b7	b6	b5	b4	b3	b2	b1	b0
XFRPOS	21	"L"	"L"	"L"	"L"	"L"	"L"	XFR POS1	XFR POS0
	22	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HXFRC -H	23	"L"	"L"	"L"	"L"	b19	b18	b17	b16
HXFRC -M	24	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	25	b7	b6	b5	b4	b3	b2	b1	b0
	26	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HADRC -H	27	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
HADRC -M	28	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	29	b7	b6	b5	b4	b3	b2	b1	b0
	2A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	2B	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	2C	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	2D	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"

Sub CPU write registers (2)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	2E	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
CADRC -H	2F	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
CADRC -M	30	b15	b14	b13	b12	b11	b10	b9	b8
CADRC -L	31	b7	b6	b5	b4	b3	b2	b1	b0
CLRINT0	32	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	"L"	"L"
CLRINT1	33	"L"	"L"	"L"	"L"	"L"	RSLT EMPT	XFR STOP	BLXF RCMP
INTEN0	34	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	"L"	"L"
INTEN1	35	"L"	"L"	"L"	"L"	"L"	"L"	XFR STOP	BLXF RCMP
BFBLKC -H	36	"L"	"L"	"L"	"L"	"L"	"L"	b9	b8
BFBLKC -L	37	b7	b6	b5	b4	b3	b2	b1	b0

Sub CPU write registers (3)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RAWHDR	00	b7	b6	b5	b4	b3	b2	b1	b0
	01								
BFHDR	02	b7	b6	b5	b4	b3	b2	b1	b0
BFSHDR	03	b7	b6	b5	b4	b3	b2	b1	b0
RAWHDR FLG	04	MIN UTE	SEC OND	BLO CK	MODE				
BFHDR FLG	05	MIN UTE	SEC OND	BLO CK	MODE	FILE	CHAN NEL	SUB MODE	DATA TYPE
DECSTS0	06	SHRT SCT	NO SYNC	COR INH	ERIN BLK	COR DONE	EDC NG	ECC NG	TGTN TMET
DECSTS1	07						EDC ALL0	C MODE	C FORM
XFRSTS	08							CBFW RRDY	CBFR DRDY
	09								
HIFSTS	0A	BUSY STS	RSLT EMPT	RSLT WRDY	PRM FULL	PRM RRDY	HINT STS2	HINT STS1	HINT STS0
DSPSTS	0B	REV# 2 "L"	REV# 1 "L"	REV# 0 "H"					CMDO BUSY
	0C								
CPUBR DT	0D	b7	b6	b5	b4	b3	b2	b1	b0
	0E	b7	b6	b5	b4	b3	b2	b1	b0
	0F	b7	b6	b5	b4	b3	b2	b1	b0
	10								
SBQSTS	11						SHTS BCS1	NOSY NC1	SUBQ ERR1
SUBQDT	12	b7	b6	b5	b4	b3	b2	b1	b0
CSCT ARA	13	b7	b6	b5	b4	b3	b2	b1	b0
	14								
CHPCTL1	15	BURS TXFR	XFRR ATE1	XFRR ATE0	RFRS CTL1	RFRS CTL0	PACK MODE		
	16								

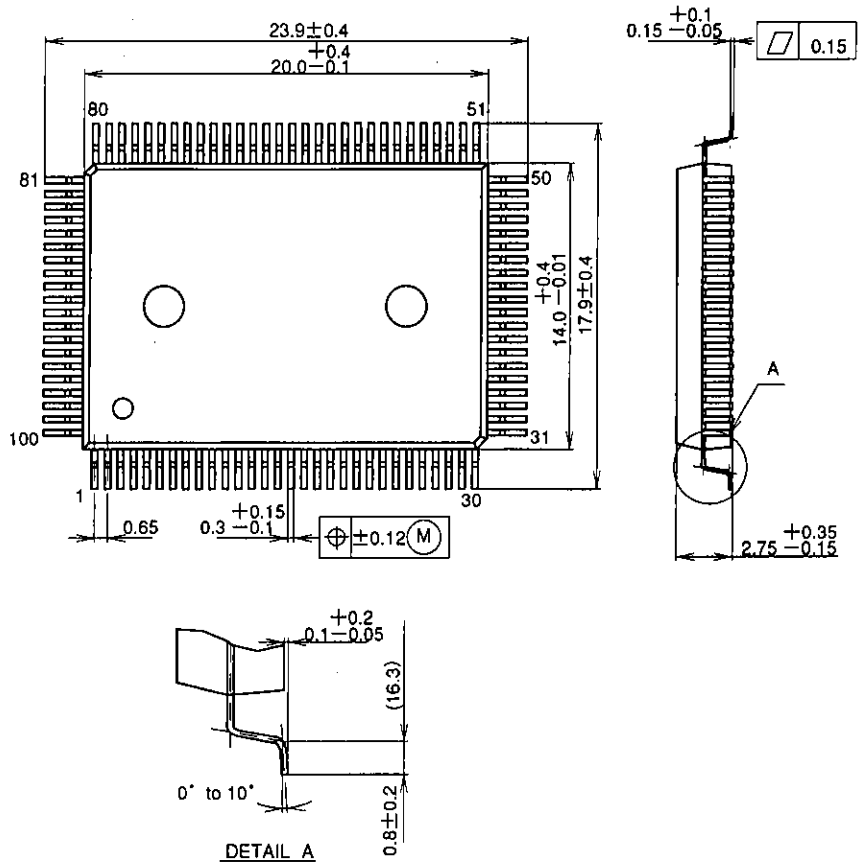
Sub CPU read registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TGTMNT	17	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	18	b7	b6	b5	b4	b3	b2	b1	b0
TGTBLK	19	b7	b6	b5	b4	b3	b2	b1	b0
	1A								
XFRCNT -H	1B	b23	b22	b21	b20	b19	b18	b17	b16
XFRCNT -M	1C	b15	b14	b13	b12	b11	b10	b9	b8
XFRCNT -L	1D	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	1E	b7	b6	b5	b4	b3	b2	b1	b0
DLADR	1F	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	20	b7	b6	b5	b4	b3	b2	b1	b0
XFRPOS	21							XFR POS1	XFR POS0
	22								
HXFRC -H	23					b19	b18	b17	b16
HXFRC -M	24	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	25	b7	b6	b5	b4	b3	b2	b1	b0
	26								
HADRC -H	27						b18	b17	b16
HADRC -M	28	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	29	b7	b6	b5	b4	b3	b2	b1	b0
	2A								
SLADR -H	2B						b18	b17	b16
SLADR -M	2C	b15	b14	b13	b12	b11	b10	b9	b8
SLADR -L	2D	b7	b6	b5	b4	b3	b2	b1	b0

Sub CPU read registers (2)

Package Outline Unit : mm

100PIN QFP(PLASTIC)



DETAIL A

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.7 g