

Digital Comb Filter (PAL/NTSC)

Description

The CXD2064Q is an adaptive intra-field comb filter compatible with NTSC, PAL, M-PAL and N-PAL systems, and can provide high-precision Y/C separation with a single chip.

Features

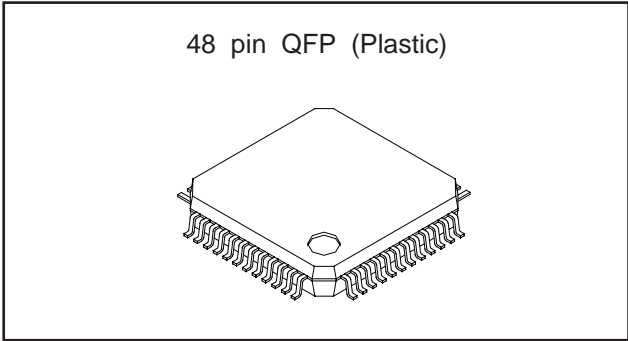
- Adaptive intra-field Y/C separation
- Vertical enhancer
- Horizontal aperture correction
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- 4x PLL
- Sync tip clamp
- Four 1H delay lines

Applications

Y/C separation for color TVs and VCRs

Structure

Silicon gate CMOS IC



Absolute Maximum Ratings (Ta=25 °C, Vss=0 V)

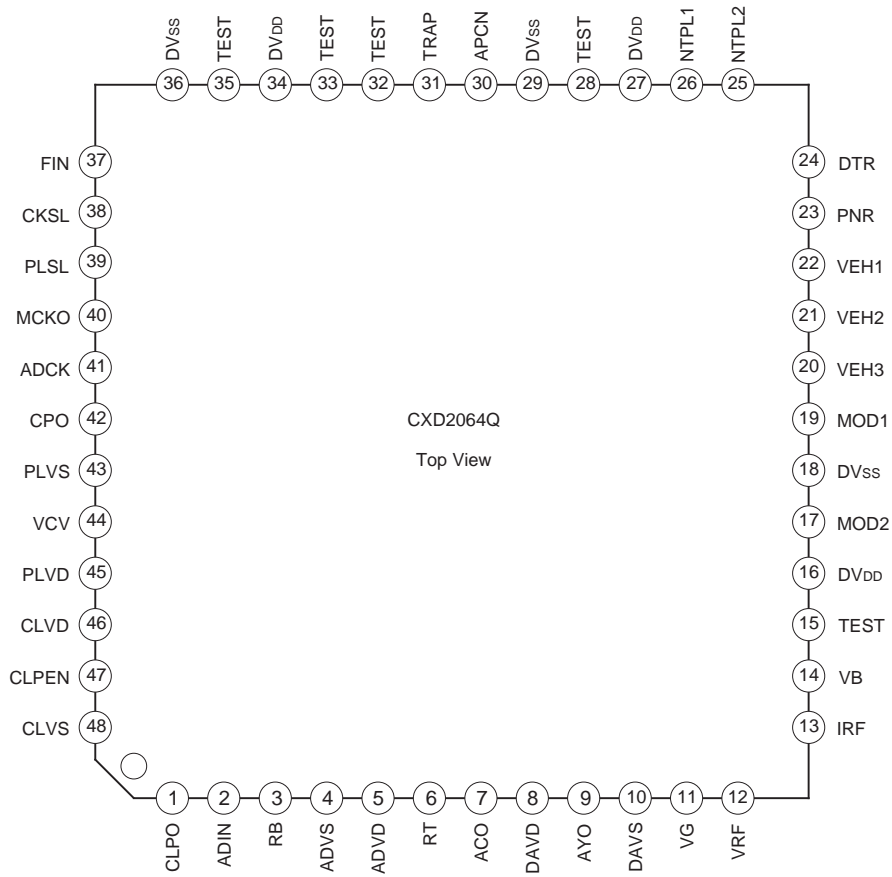
• Supply voltage	DV _{DD}	V _{SS} -0.5 to +7.0	V
	DAVD	V _{SS} -0.5 to +7.0	V
	ADVD	V _{SS} -0.5 to +7.0	V
	PLVD	V _{SS} -0.5 to +7.0	V
	CLVD	V _{SS} -0.5 to +7.0	V
• Input voltage	V _I	V _{SS} -0.5 to V _{DD} +0.5	V
• Output voltage	V _O	V _{SS} -0.5 to V _{DD} +0.5	V
• Storage temperature	T _{stg}	-55 to +150	°C

Recommended Operating Conditions

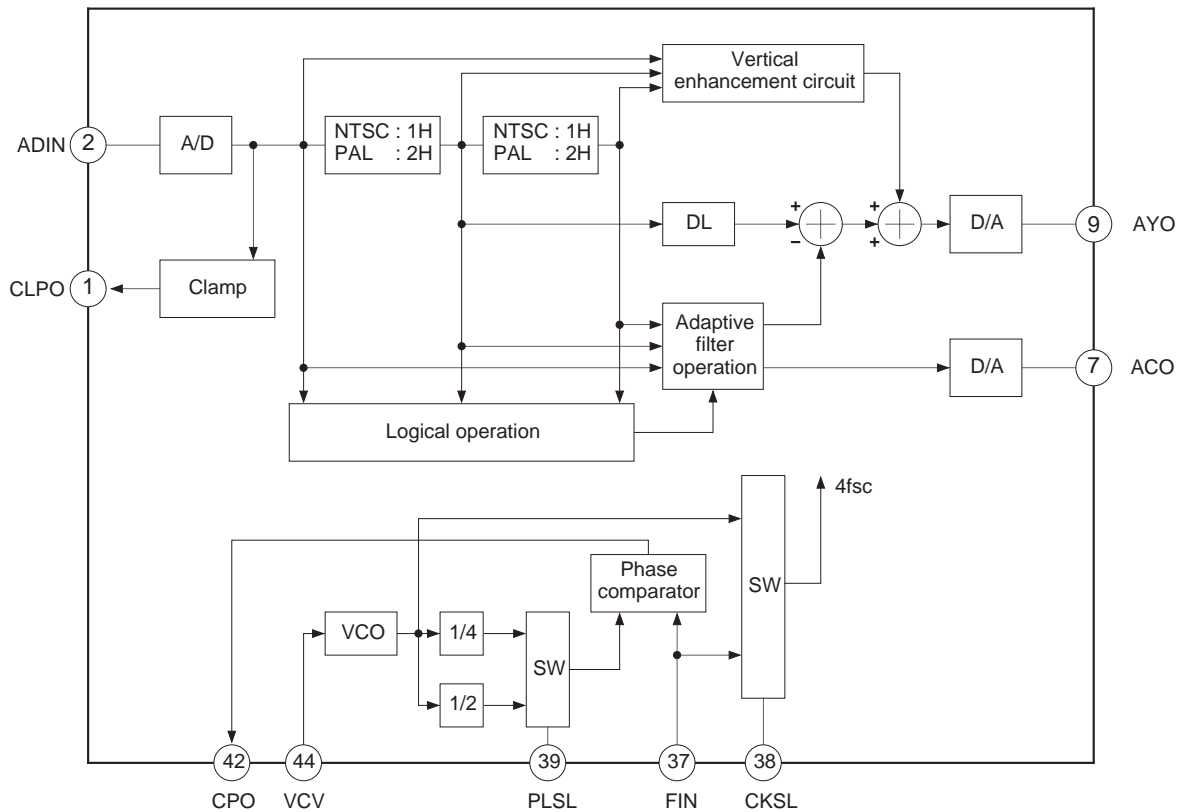
• Supply voltage	DV _{DD}	5.0 ± 0.25	V
	DAVD	5.0 ± 0.25	V
	ADVD	5.0 ± 0.25	V
	PLVD	5.0 ± 0.25	V
	CLVD	5.0 ± 0.25	V
• Analog input	ADIN	1.8	V _{p-p}
• Operating temperature	T _{opr}	-20 to +70	°C

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Pin Configuration



Block Diagram



Pin No.	Symbol	I/O	Description
31	TRAP	I	Trap filter setting. Low : Off, High : On.
32	TEST	I	Test pin. Normally open or fix to "Low".
33	TEST	I	Test pin. Normally open or fix to "Low".
34	DV _{DD}	—	Digital power supply. (5.0 V)
35	TEST	I	Test pin. Normally open or fix to "Low".
36	DV _{SS}	—	Digital ground.
37	FIN	I	Clock input. Input the burst-locked fsc (2fsc) when using the internal PLL. Input the burst-locked 4fsc when not using the internal PLL.
38	CKSL	I	PLL control. Low : The internal PLL is not used. The clock (4fsc) which is input to FIN is supplied internally. High : The internal PLL is used. VCO oscillation output 4fsc clock is supplied internally.
39	PLSL	I	Selects the clock input to FIN. Low : fsc, High : 2fsc. When inputting 4fsc to FIN (when not using the internal PLL), this pin may be set to either "Low" or "High".
40	MCKO	O	Clock (4fsc) output.
41	ADCK	I	Clock input for A/D converter. Normally connect to MCKO.
42	CPO	O	PLL phase comparator output. Leave open when not using the PLL.
43	PLVS	—	PLL analog ground.
44	VCV	I	VCO control voltage input. Connect to PLVS when not using the PLL.
45	PLVD	—	PLL analog power supply. (5.0 V)
46	CLVD	—	Clamp D/A converter analog power supply. (5.0 V)
47	CLPEN	I	Clamp circuit enable pin. Low : Clamp on, High : Clamp off.
48	CLVS	—	Clamp D/A converter analog ground.

Electrical Characteristics

DC Characteristics

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	DV _{DD} DAVD ADVD PLVD CLVD	—	4.75	5.0	5.25	V	*1
Operating temperature	Topr	—	-20		+70	°C	
Input/output voltage	V _I , V _O	—	V _{SS}		V _{DD}	V	*2
Input voltage	V _{IH}	CMOS level input	0.7 V _{DD}			V	*3
	V _{IL}				0.3 V _{DD}		
Input rise/fall time	tr, tf	—	0		500	ns	*1
Output voltage	V _{OH}	I _{OH} =-2 mA	V _{DD} -0.8			V	*4
		I _{OH} =-3 mA					*5
	V _{OL}	I _{OL} =4 mA			0.4		*4
		I _{OL} =1.5 mA					*5
Logical V _{th}	LV _{th}	—		V _{DD} /2		V	
Input voltage	V _{IH}	—	0.7 V _{DD}			V	*6
	V _{IL}				0.3 V _{DD}		
Clock input amplitude	V _{IN}	f _{max} =50 MHz sine wave	0.5			V _{p-p}	
Feedback resistance value	R _{Fb}	V _{IN} =V _{SS} or V _{DD}	250 k	1 M	2.5 M	Ω	
Input leak current	I _{IL} , I _{IH}	V _{IN} =V _{SS} or V _{DD}	-10		10	μA	*7
	I _{IH}	V _{IH} =V _{DD}	40	100	240		*8
Clock amplifier output delay	—	—	3.0	9.0	18.0	ns	*9

- *1 All pins
- *2 All pins other than *6
- *3 All input pins other than *6
- *4 All output pins other than *5
- *5 CPO (Pin 42)
- *6 FIN (Pin 37)
- *7 All pins other than *8
- *8 Pins 32, 33 and 35
- *9 MCKO (Pin 40)

I/O Pin Capacitance

(Ta=25 °C, f=1 MHz, VIN=VOUT=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C _{IN}	—	—	9	pF
Output pin capacitance	C _{OUT}	—	—	11	

Internal 8-bit A/D Converter Characteristics(V_{DD}=5 V, Ta=25 °C, f=10 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	f _{max}		18	—	—	MSPS
Analog input bandwidth	BW	-3 dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT—VRB		1.96	2.08	2.22	V
Output data delay	tpd		—	—	45	ns
Differential linearity error	E _D		-1.0	—	+1.0	LSB
Integral linearity error	E _L		-2.0	—	+2.0	LSB

Internal 8-bit D/A Converter Characteristics(V_{DD}=5 V, V_{RF}=2 V, R_{IRF}=3.3 kΩ, R=200 Ω, Ta=25 °C, f=10 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	f _{max}		18	—	—	MSPS
Differential linearity error	E _D		-0.8	—	+0.8	LSB
Integral linearity error	E _L		-2.0	—	+2.0	LSB
Output full-scale voltage	V _{FS}		1.805	1.90	1.995	V
Output full-scale current	I _{FS}		—	9.5	15	mA
Output offset voltage	V _{OS}		—	—	1.0	mV
Glitch energy	G _E	R=75 Ω, 1 V _{p-p} output	—	30	—	pV-s

Internal Clamp(V_{DD}=5 V, Ta=25 °C, f=10 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clamp level *1	CLV		—	0.67	—	V

*1 Sync tip clamp

Description of Functions

- Y/C separation mode

The Y/C separation mode can be switched by the following pin settings.

Mode name	MOD2 (Pin 17)	MOD1 (Pin 19)
Adaptive processing mode	L	L
BPF separation mode	H	L
Through mode	H	H

Adaptive processing mode :

Y/C separation is performed by detecting the correlation between three lines and switching between comb filter and BPF processing.

BPF separation mode :

Y/C separation is performed only by BPF processing.

Through mode :

The composite video signal input from ADIN (Pin 2) is A/D converted and then D/A converted without modification. D/A outputs are AYO (Pin 9) and ACO (Pin 7).

- Horizontal aperture correction circuit

This circuit corrects the frequency response degradation caused by the aperture effects accompanying D/A conversion. This circuit is valid in the adaptive processing and BPF separation modes noted above.

- Trap filter circuit

A trap filter is applied to remove the frequency components near fsc in the luminance signal after Y/C separation.

This reduces the fsc frequency component gain by approximately 2.5 dB.

This circuit is valid in the adaptive processing and BPF separation modes noted above.

- Using the internal PLL (clock selection method)

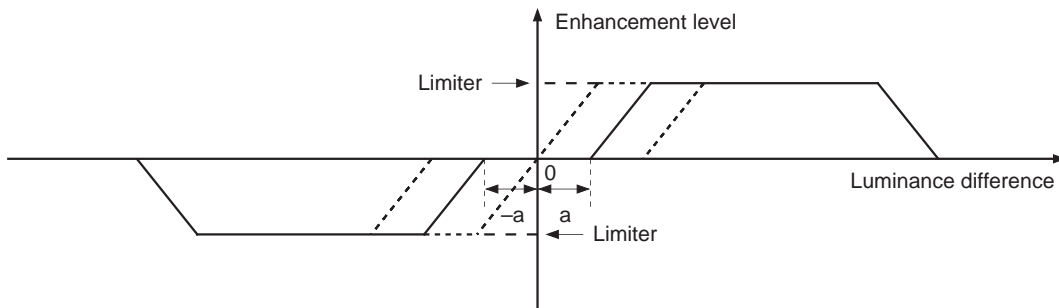
	FIN (Pin 37)	CKSL (Pin 38)	PLSL (Pin 39)
PLL used	fsc input	H	L
	2 fsc input	H	H
PLL not used	4 fsc input	L	L/H

• Vertical enhancement circuit

This circuit generates an enhanced component in accordance with the vertical aperture component (luminance difference from the preceding and following lines) of the luminance signal. The vertical aperture of the picture can be enhanced naturally by adding this enhanced component to the luminance signal after Y/C separation.

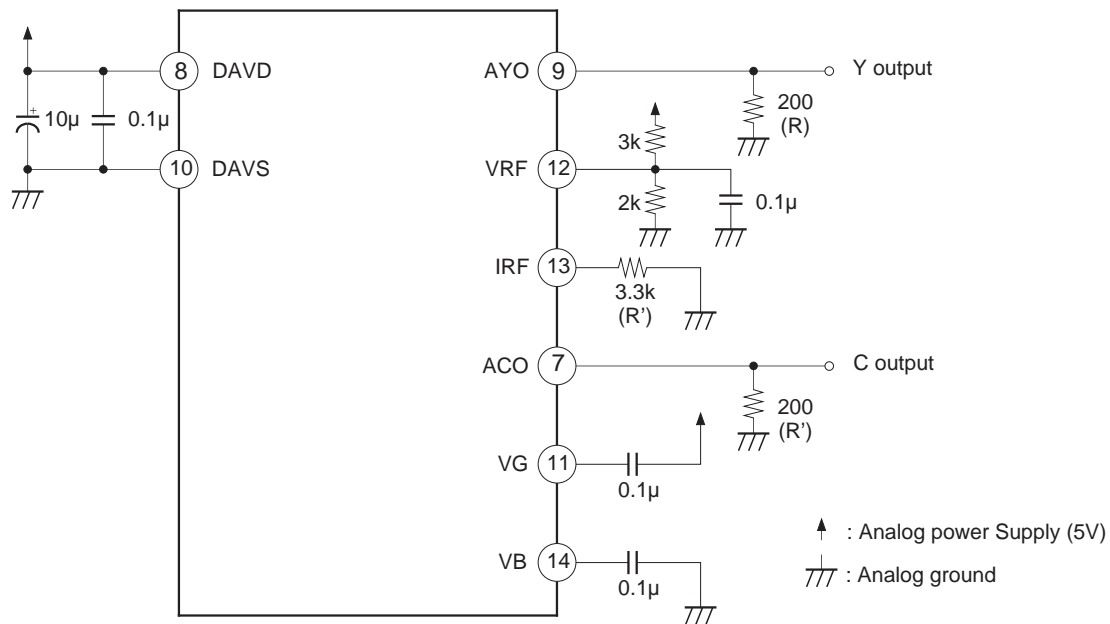
The enhancement level can be set in eight steps. The size of $|a|$ in the figure below varies according to the pin settings. Accordingly, enhanced level can be changed for portions of natural pictures with small luminance differences where the effects are particularly easy to see.

Portions with large luminance differences are cut with a limiter so that they are not excessively enhanced. Also, portions with extremely large luminance differences such as white and black lines are not enhanced because they need be enhanced any more.



Enhancement level	Pin settings			$ a $
	VEH3 (Pin 20)	VEH2 (Pin 21)	VEH1 (Pin 22)	
OFF	L	L	L	—
1	L	L	H	Large ↑
2	L	H	L	
3	L	H	H	
4	H	L	L	↓ Small
5	H	L	H	
6	H	H	L	
Max	H	H	H	

Application Circuit for D/A Converter Block



- Method of selecting the output resistor

The CXD2064Q has a built-in current output type D/A converter. To obtain the output voltages, connect resistors to the AYO and ACO pins.

The specs are as follows : output full-scale voltage $V_{FS}=0.5$ to 2.0 [V], output full-scale current $I_{FS}=0$ to 15 [mA].

Calculate the output resistance value using the relationship $V_{FS}=I_{FS} \times R$. In addition, connect a resistor of 16 times the output resistor to the reference current pin (IRF). In case this results in a unpractical value, use a resistance value as close to the calculated value as possible.

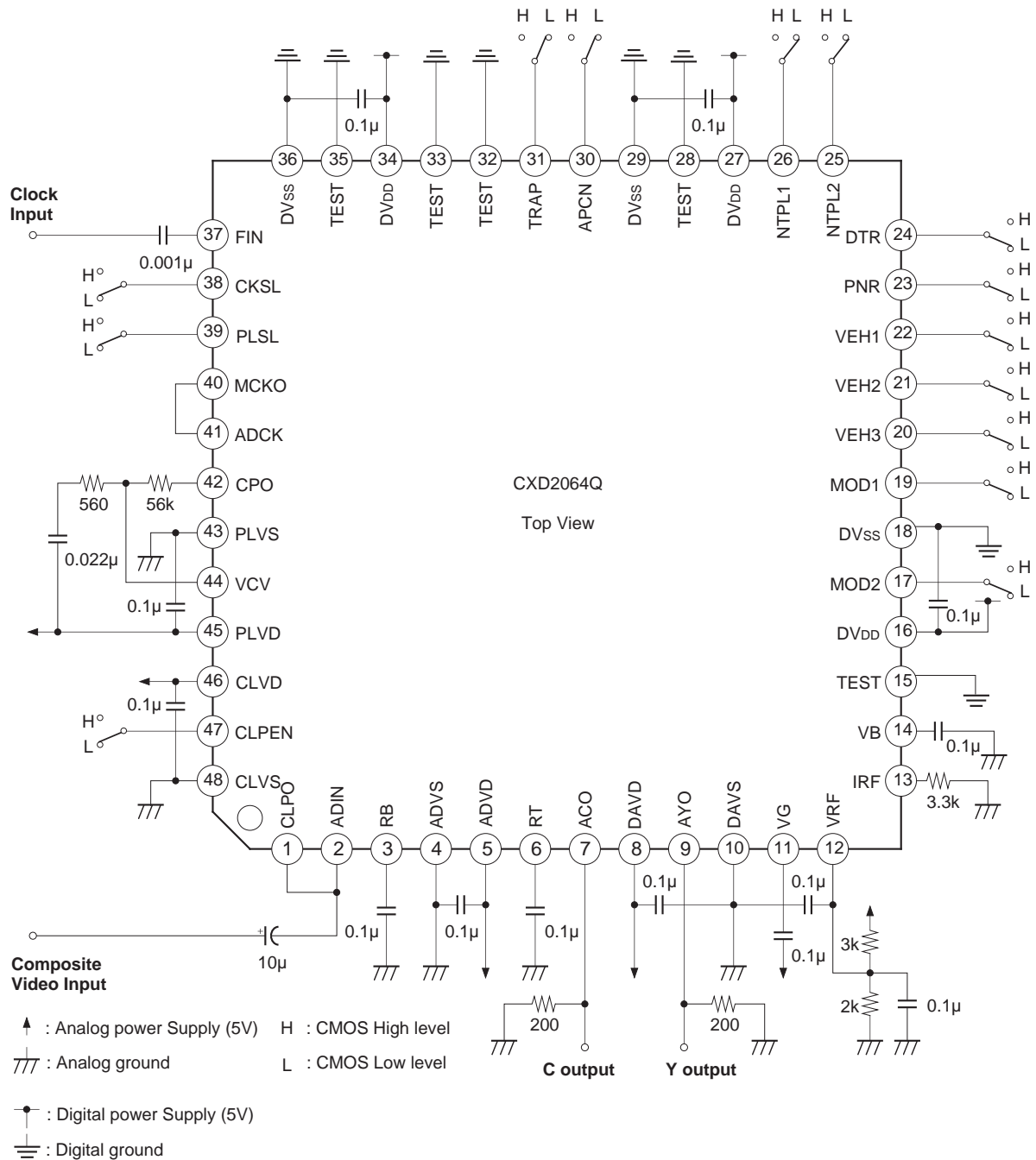
Note that, at this time, $V_{FS}=V_{RF} \times 16R/R'$ (V_{RF} : Pin voltage of VRF). Here, R is the resistor connected to AYO/ACO, and R' is the resistor connected to IRF.

Power consumption can be reduced by using higher resistance values, but the glitch energy and data settling time increase contrastingly. Set the optimum values according to the system applications.

- V_{DD} , V_{SS}

Separate the analog and digital systems around the device to reduce the effects of noise. DAVD is bypassed to DAVS as close to each other as possible through a ceramic capacitor of approximately $0.1 \mu\text{F}$.

External Connection Diagram



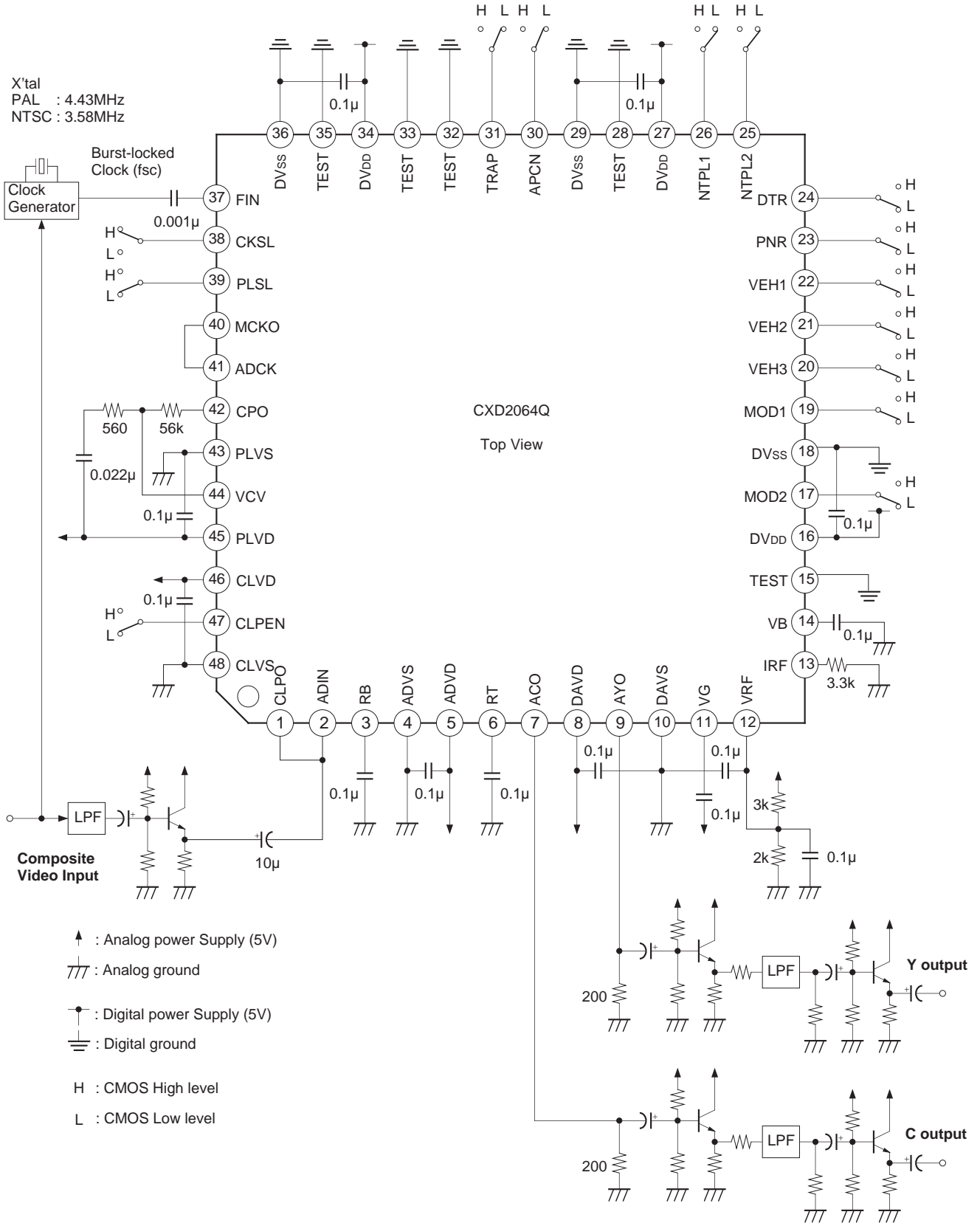
Notes on Operation

- Make the wiring for the signal input to ADIN (Pin 2) as short as possible. Also, drive the input signal to ADIN at low impedance.
- Make the analog and digital power supply and GND lines as wide and short as possible to ensure low impedance.
- Bypass the analog and digital power supply pins to GND with a ceramic capacitor of about 0.1 µF connected as close to the pin as possible.
- Input a clock that is locked to the burst signal of the input video signal.
- Separate the wiring to the clock input pin FIN (Pin 37) from the external analog circuits, analog power supplies and analog GND.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 1

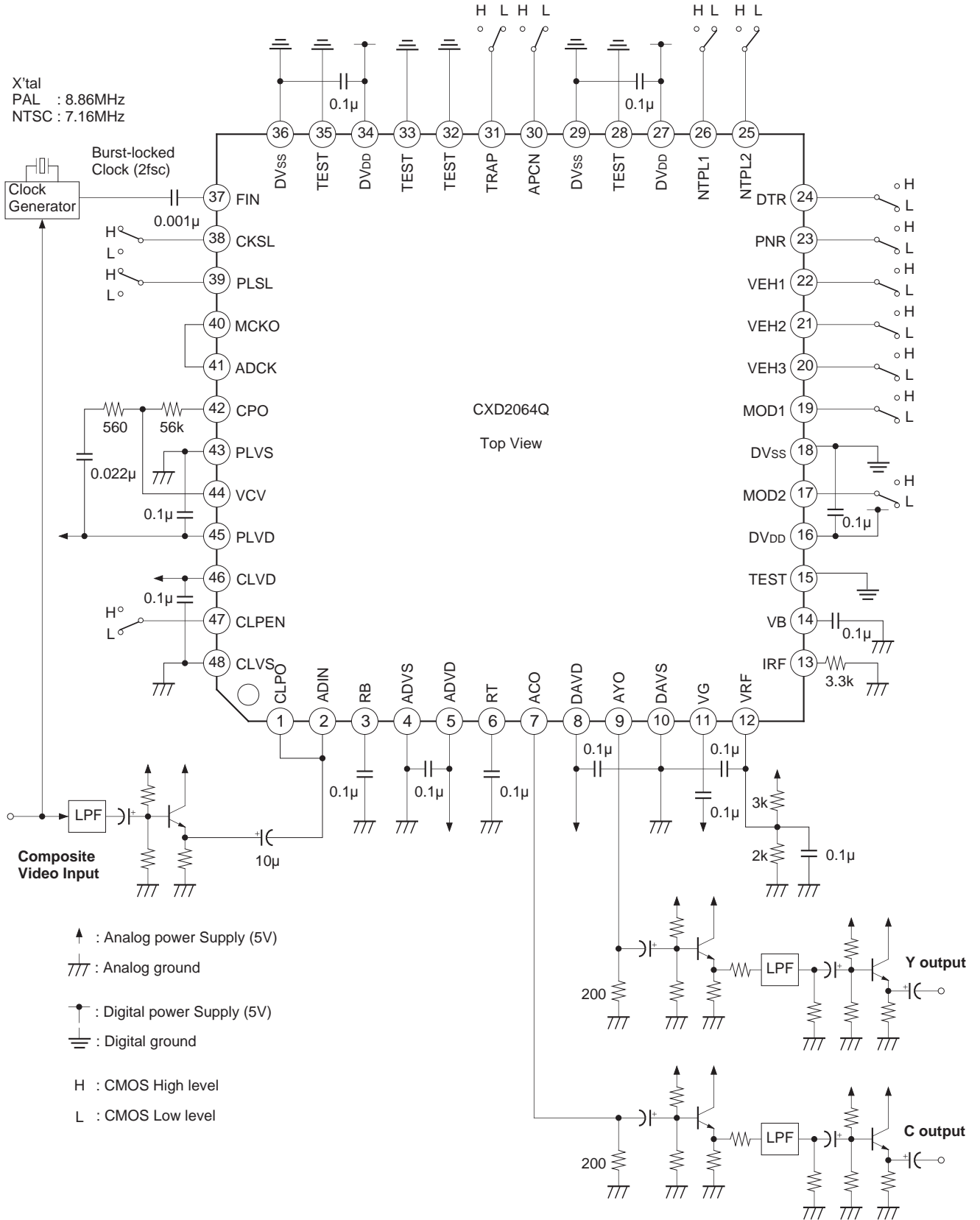
- fsc is used for clock



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Application Circuit 2

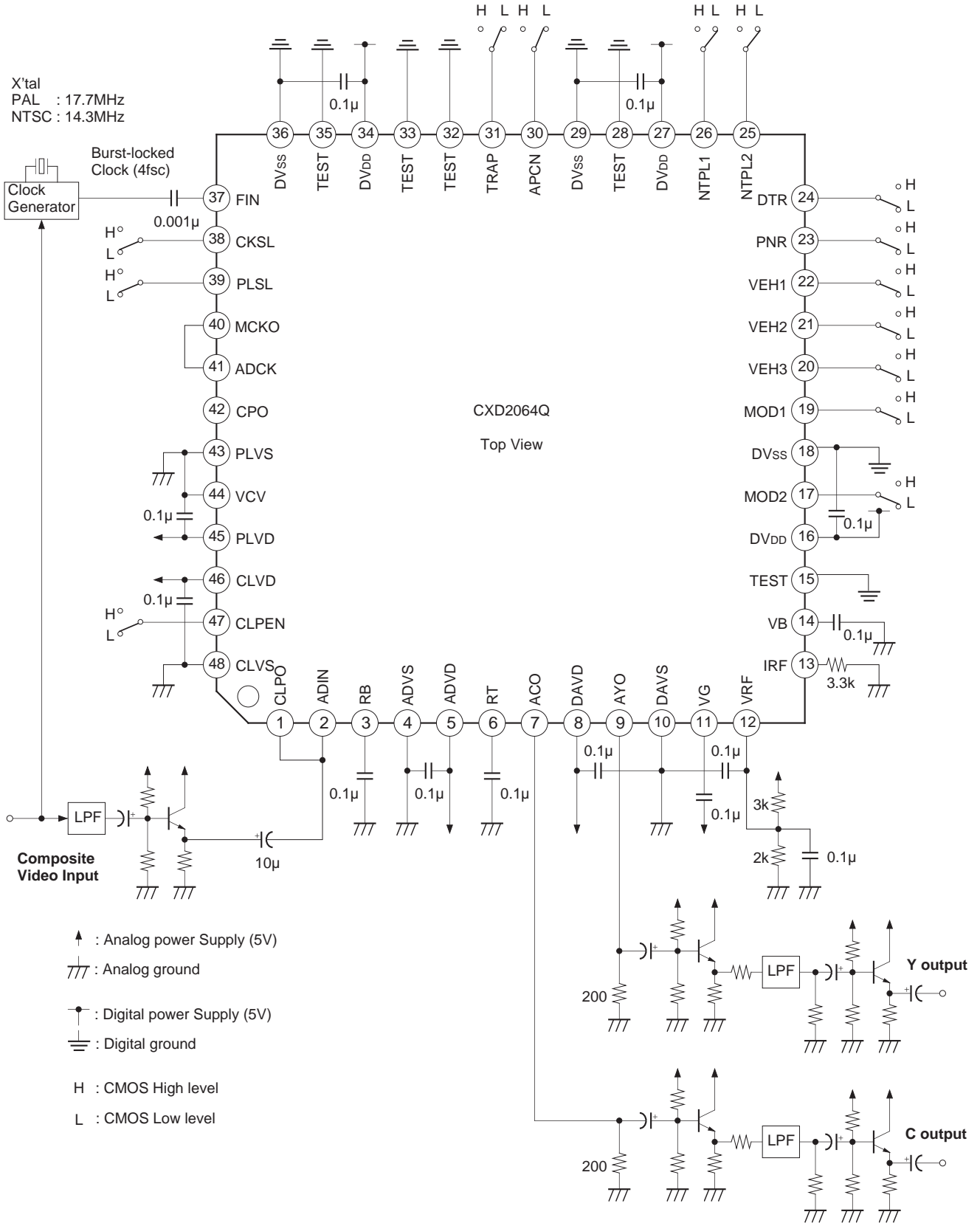
- 2fsc is used for clock



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Application Circuit 3

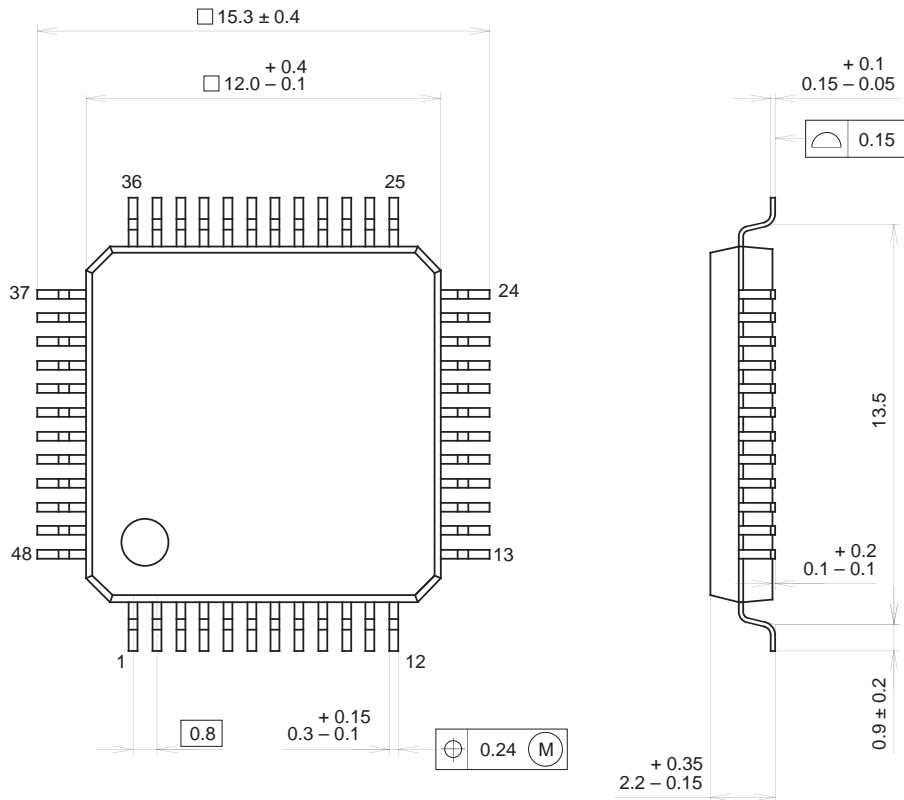
- 4fsc is used for clock



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Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g