SONY

CXD2302Q

8-bit 50MSPS Video A/D Converter with Clamp Function

Description

The CXD2302Q is an 8-bit CMOS A/D converter for video with synchronizing clamp function. The adoption of 2 step-parallel method achieves low power consumption and a maximum conversion rate of 50MSPS.

Features

- Resolution: 8 bit ± 1/2LSB (DL)
- Maximum sampling frequency: 50MSPS
- Low power consumption: 125mW (at 50MSPS typ.) (reference current excluded)
- Synchronizing clamp function
- Clamp ON/OFF function
- Reference voltage self-bias circuit
- Input CMOS/TTL compatible
- 3-state TTL compatible output
- Single 5V power supply or dual 5V/3.3V power supply
- Low input capacitance: 15pF
- Reference impedance: 370Ω (typ.)

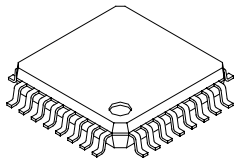
Applications

Wide range of applications that require high-speed A/D conversion such as TV and VCR.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

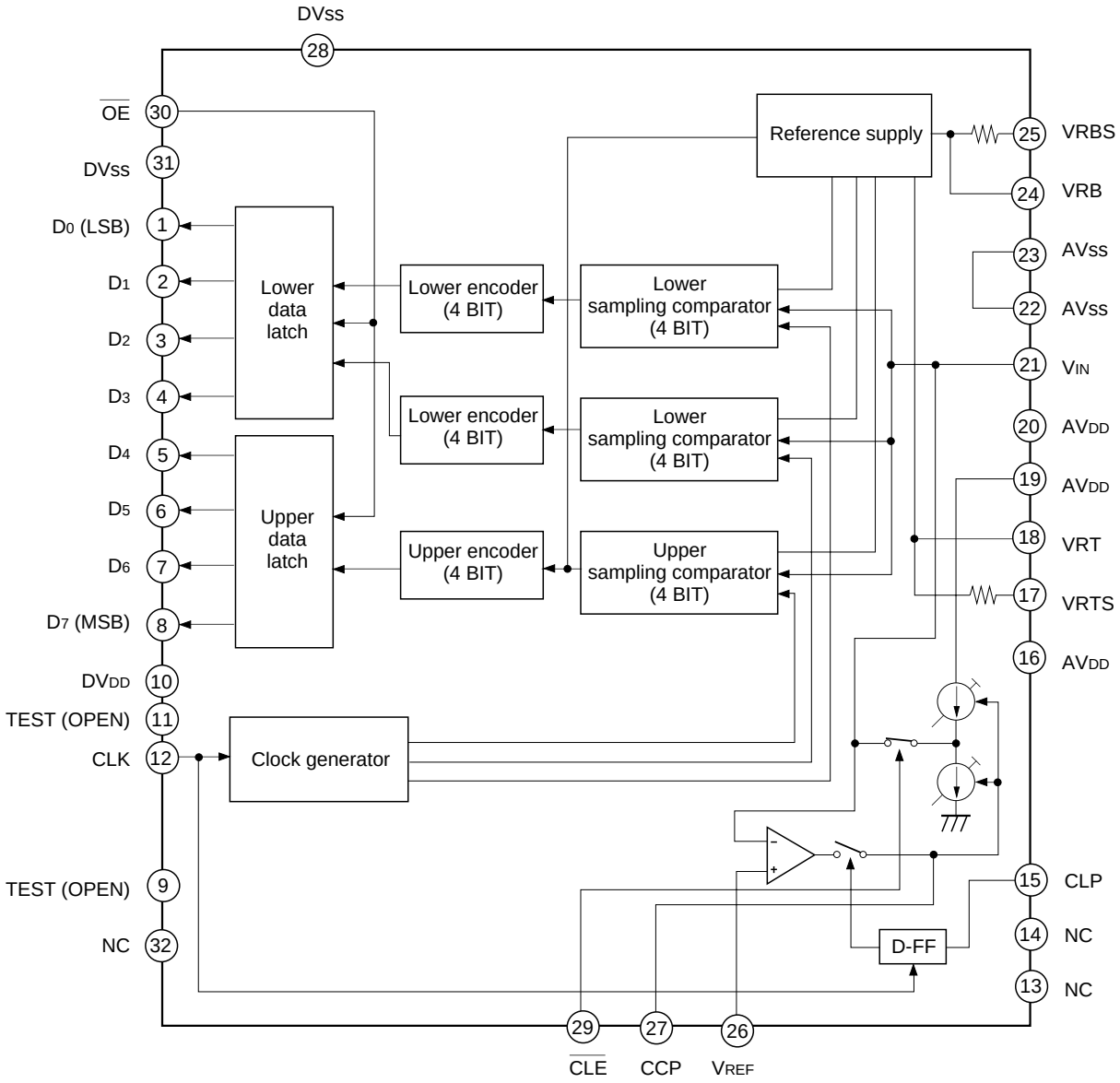
• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} + 0.5 to Vss – 0.5	V
• Input voltage (Analog)	V_{IN}	V_{DD} + 0.5 to Vss – 0.5	V
• Input voltage (Digital)	V_I	V_{DD} + 0.5 to Vss – 0.5	V
• Output voltage (Digital)	V_O	V_{DD} + 0.5 to Vss – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

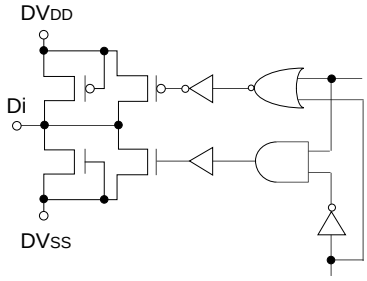
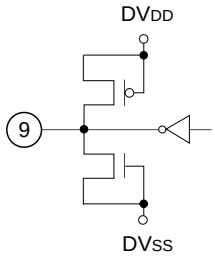
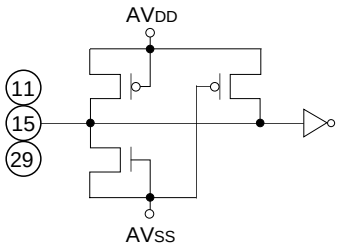
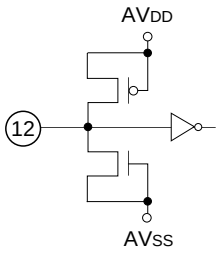
• Supply voltage	AV_{DD}, AVss	4.75 to 5.25	V
	DV_{DD}, DVss	3.0 to 5.5	V
	| DVss – AVss |	0 to 100	mV
• Reference input voltage			
	V_{RB}	0 and above	V
	V_{RT}	2.7 and below	V
• Analog input	V_{IN}	1.7Vp-p above	
• Clock pulse width			
	T_{PW1}, T_{PW0}	9ns (min) to 1.1µs (max)	
• Operating ambient temperature			
	Topr	–40 to +85	°C

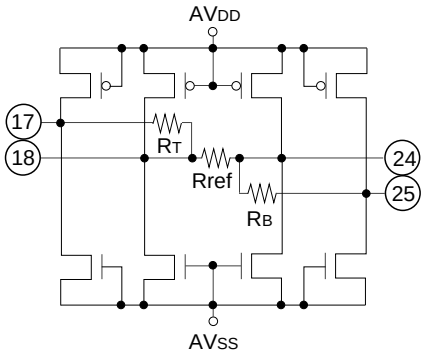
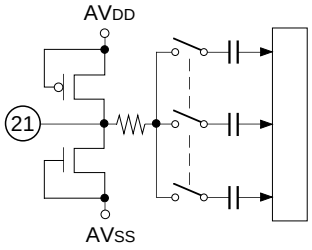
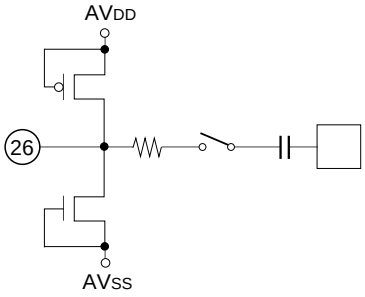
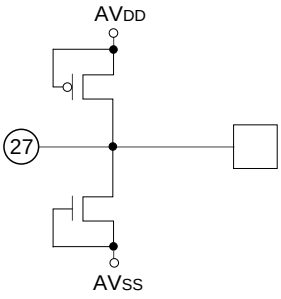
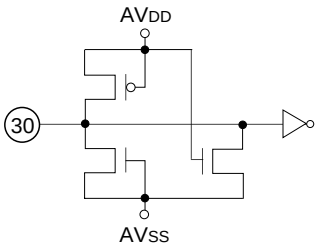
E94102F0Z-PS

Block Diagram



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
9	TEST		Leave open for normal use.
10	DV_{DD}		Digital power supply +5V or +3.3V
11	TEST		Leave open for normal use. Pull-up resistor is built in.
15	CLP		Input the clamp pulse. Clamps the signal voltage during Low interval. Pull-up resistor is built in.
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE}$ = High. Pull-up resistor is built in.
12	CLK		Clock input. Set to Low level when no clock is input.
13, 14, 32	NC		
16, 19, 20	AV_{DD}		Analog power supply +5V

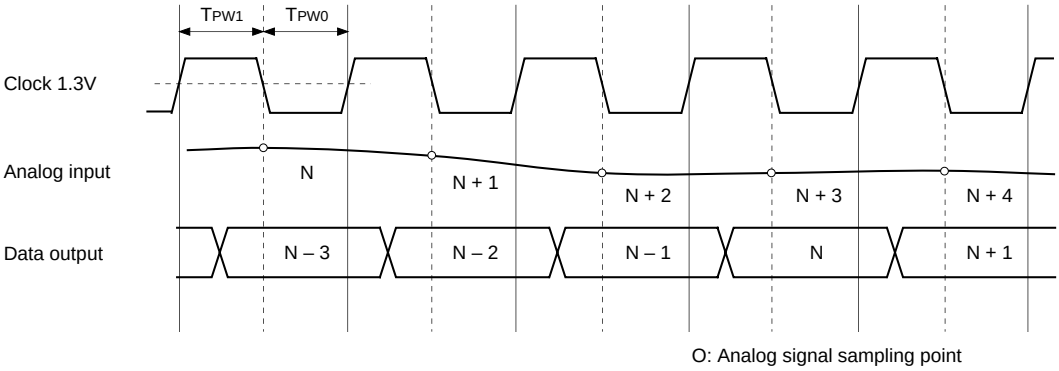
Pin No.	Symbol	Equivalent circuit	Description
17	VRTS		Generates approximately +2.5V when shorted with AVDD.
18	VRT		Reference voltage (top)
24	VRB		Reference voltage (bottom)
25	VRBS		Generates approximately +0.6V when shorted with AVSS.
21	VIN		Analog input
22, 23	AVSS		Analog ground
26	VREF		Clamp reference voltage input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in VIN voltage is positive phase.
28, 31	DVSS		Digital ground
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High. Pull-down resistor is built in.

Digital output

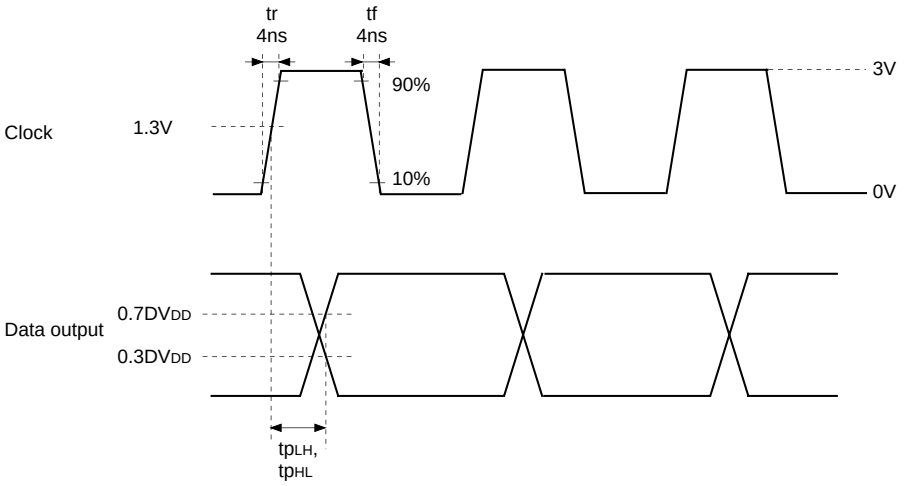
The following table shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
:	:	:
:	127	1 0 0 0 0 0 0 0
:	128	0 1 1 1 1 1 1 1
:	:	:
V_{RB}	255	0 0 0 0 0 0 0 0

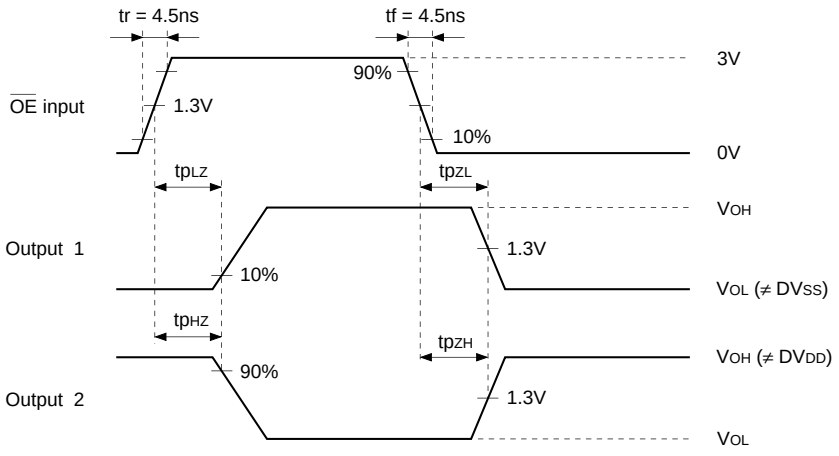
Timing Chart I



Timing Chart I-1.



Timing Chart I-2.



Timing Chart I-3.

Electrical Characteristics

Analog characteristics (Fc = 50MHz, AV_{DD} = 5V, DV_{DD} = 3 to 5.5V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Max. conversion rate	Fc max.	AV_{DD} = 4.75 to 5.25V Ta = –40 to +85°C, V_{IN} = 0.5 to 2.5V f_{IN} = 1kHz triangular wave		50	65		MSPS
Min. conversion rate	Fc min.					0.5	
Analog input band width	BW	Envelope R_{IN} = 33Ω	–1dB		60		MHz
			–3dB		100		
Differential non-linearity error	E_D	End point			±0.3	±0.5	LSB
Integral non-linearity error	E_L				+0.7	±1.5	
Offset voltage*1	E_{OT}	Potential difference to VRT		–70	–50	–30	mV
	E_{OB}	Potential difference to VRB		20	40	60	
Differential gain error	DG	NTSC 40 IRE mod ramp Fc =14.3MSPS			3		%
Differential phase error	DP				1.5		deg
Sampling delay	tsd				0		ns
Clamp offset voltage*2	E_{OC}	V_{IN} = DC C_{IN} = 10µF tpcw = 2.75µs Fc = 14.3MHz Fclp = 15.75kHz	V_{REF} = 0.5V	0	20	40	mV
			V_{REF} = 2.5V	0	20	40	
Signal-to-noise ratio	SNR	FIN = 100kHz			45		dB
		FIN = 500kHz			44		
		FIN = 1MHz			44		
		FIN = 3MHz			43		
		FIN = 10MHz			38		
		FIN = 25MHz			32		
Spurious free dynamic range	FSDR	FIN = 100kHz			51		dB
		FIN = 500kHz			46		
		FIN = 1MHz			49		
		FIN = 3MHz			46		
		FIN = 10MHz			45		
		FIN = 25MHz			45		

*1 The offset voltage EOB is a potential difference between VRB and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from “00000000” to “00000001”. EOT is a potential difference between VRT and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from “11111111” to “11111110”.

*2 Clamp offset voltage varies individually. When using with R, G, B 3 channels, color sliding may be generated.

DC characteristics (Fc = 50MHz, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item		Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current		I_{AD} + I_{DD}	NTSC ramp wave input $\overline{CLE}$ = 0V	DV_{DD} = 5V		25	36	mA
	Analog	I_{AD}		DV_{DD} = 3.3V		23	33	
	Digital	I_{DD}				2	3	
Reference current		I_{REF}			4.1	5.4	7.7	mA
Reference resistance (V_{RT} – V_{RB})		R_{REF}			260	370	480	Ω
Self-bias voltage		V_{RB}	Shorts V_{RTS} and AV_{DD} Shorts V_{RBS} and AV_{SS}		0.52	0.56	0.60	V
		V_{RT} – V_{RB}			1.80	1.92	2.04	
Analog input resistance		R_{IN}	VIN	Fc = 50MHz		13		kΩ
				Fc = 35MHz		16		
				Fc = 20MHz		30		
Input capacitance		C_{AI1}	VIN, VIN = 1.5V + 0.07Vrms			15		pF
		C_{AI2}	VRTS, VRT, VRB, VRBS, VREF				11	
		C_{DIN}	TEST, CLK, CLP, $\overline{CLE}$, $\overline{OE}$				11	
Output capacitance		C_{AO}	CCP				11	pF
		C_{DO}	D0 to D7, TEST				11	
Digital input voltage		V_{IH}	AV_{DD} = 4.75 to 5.25V DV_{DD} = 3 to 5.5V Ta = –40 to +85°C		2.2			V
		V_{IL}					0.8	
Digital input current		I_{IH} I_{IL}	V_I = 0V to AV_{DD} Ta = –40 to +85°C	CLK	–240		240	µA
				TEST, CLP, $\overline{CLE}$	–240		40	
				$\overline{OE}$	–40		240	
Digital output current		I_{OH}	$\overline{OE}$ = 0V DV_{DD} = 5V Ta = –40 to +85°C	V_{OH} = DV_{DD} – 0.8V			–2	mA
		I_{OL}		V_{OL} = 0.4V	4			
		I_{OH}	$\overline{OE}$ = 0V DV_{DD} = 3.3V Ta = –40 to +85°C	V_{OH} = DV_{DD} – 0.8V			–1.2	mA
		I_{OL}		V_{OL} = 0.4V	2.4			
		I_{OZH}	$\overline{OE}$ = 3V DV_{DD} = 3 to 5.5V Ta = –40 to +85°C	V_{OH} = DV_{DD}	–40		40	µA
		I_{OZL}		V_{OL} = 0V	–40		40	

Note) The voltage of up to (AV_{DD} + 0.5V) can be input when DV_{DD} = 3.3V. But the output pin voltage is less than the DV_{DD} voltage. When the digital output is in the high impedance mode, the IC may be damaged by applying the voltage which is more than the (DV_{DD} + 0.5V) voltage to the digital output.

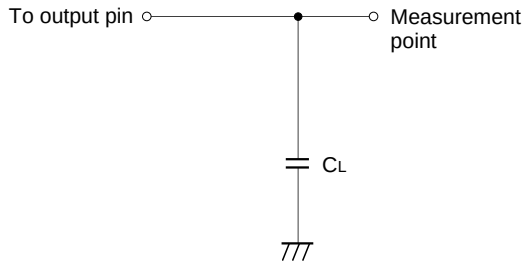
Timing (Fc = 50MHz, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output data delay	t_{pLH}	C_L = 15pF $\overline{OE}$ = 0V	DV_{DD} = 5V	5.5	9.5	12.0	ns
	t_{pHL}				8.5		
	t_{pLH}		DV_{DD} = 3.3V	4.3	11.8	16.3	
	t_{pHL}				7.6		
Tri-state output enable time	t_{pZH}	R_L = 1kΩ C_L = 15pF $\overline{OE}$ = 3V → 0V	DV_{DD} = 5V	2.5	4.5	8.0	ns
	t_{pZL}				6.0		
	t_{pZH}		DV_{DD} = 3.3V	3.0	7.0	9.0	
	t_{pZL}				5.0		
Tri-state output disable time	t_{pHZ} t_{pLZ}	R_L = 1kΩ C_L = 15pF $\overline{OE}$ = 0V → 3V	DV_{DD} = 5V	3.5	5.5	7.5	ns
	t_{pHZ} t_{pLZ}		DV_{DD} = 3.3V	2.5	5.5	8.0	
Clamp pulse width*	t_{CPW}	Fc = 14.3MHz, C_{IN} = 10µF for NTSC wave		1.75	2.75	3.75	µs

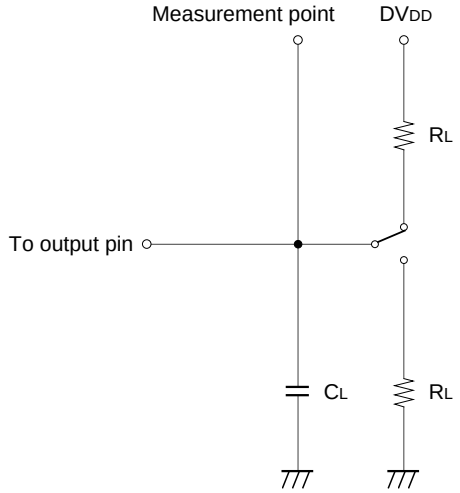
* The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) for other processing systems to equal the values for NTSC.

Electrical Characteristics Measurement Circuit

Output data delay measurement circuit

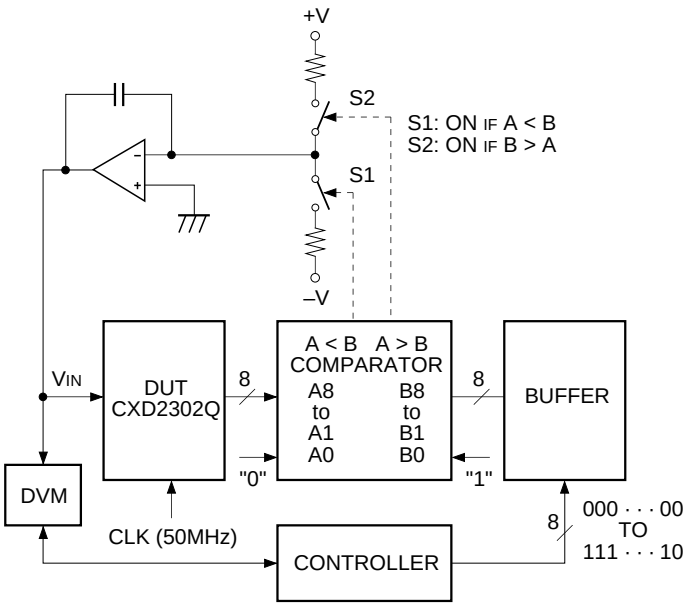


Tri-state output measurement circuit

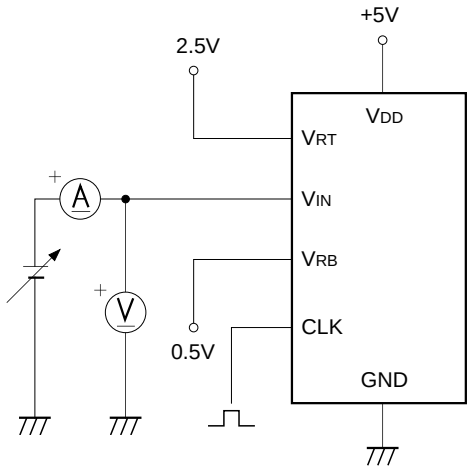


Note) C_L includes capacitance of probes.

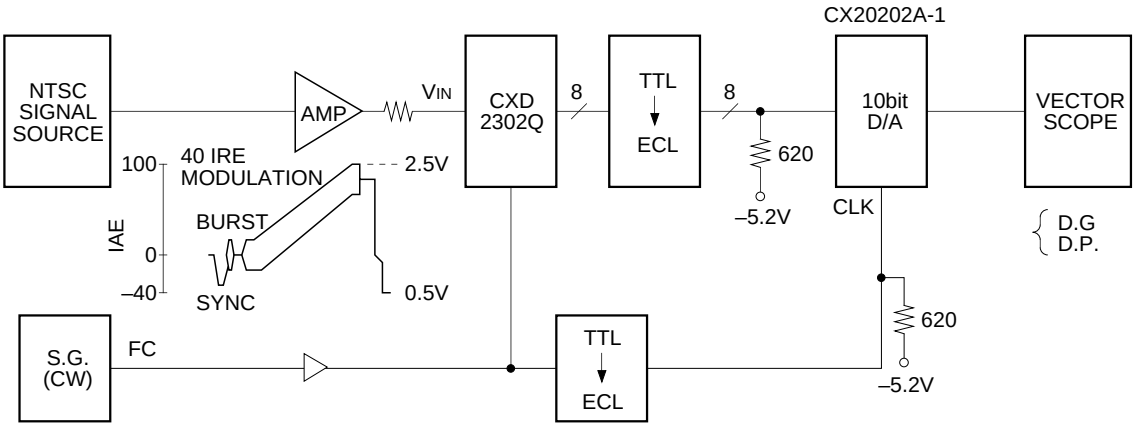
Integral non-linearity error
Differential non-linearity error } **test circuit**
Offset voltage



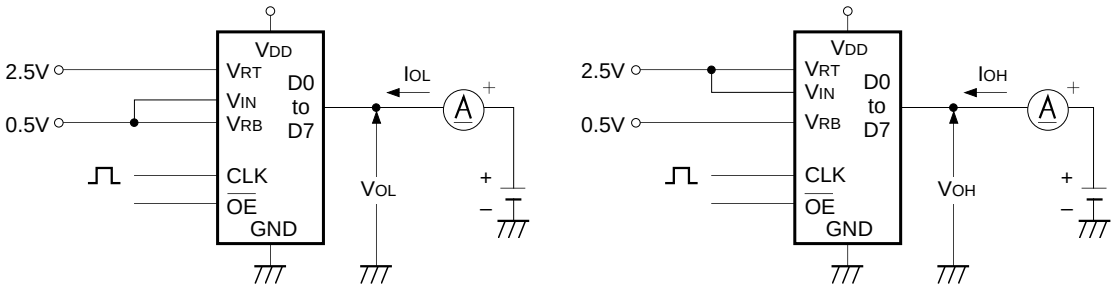
Analog input resistance test circuit



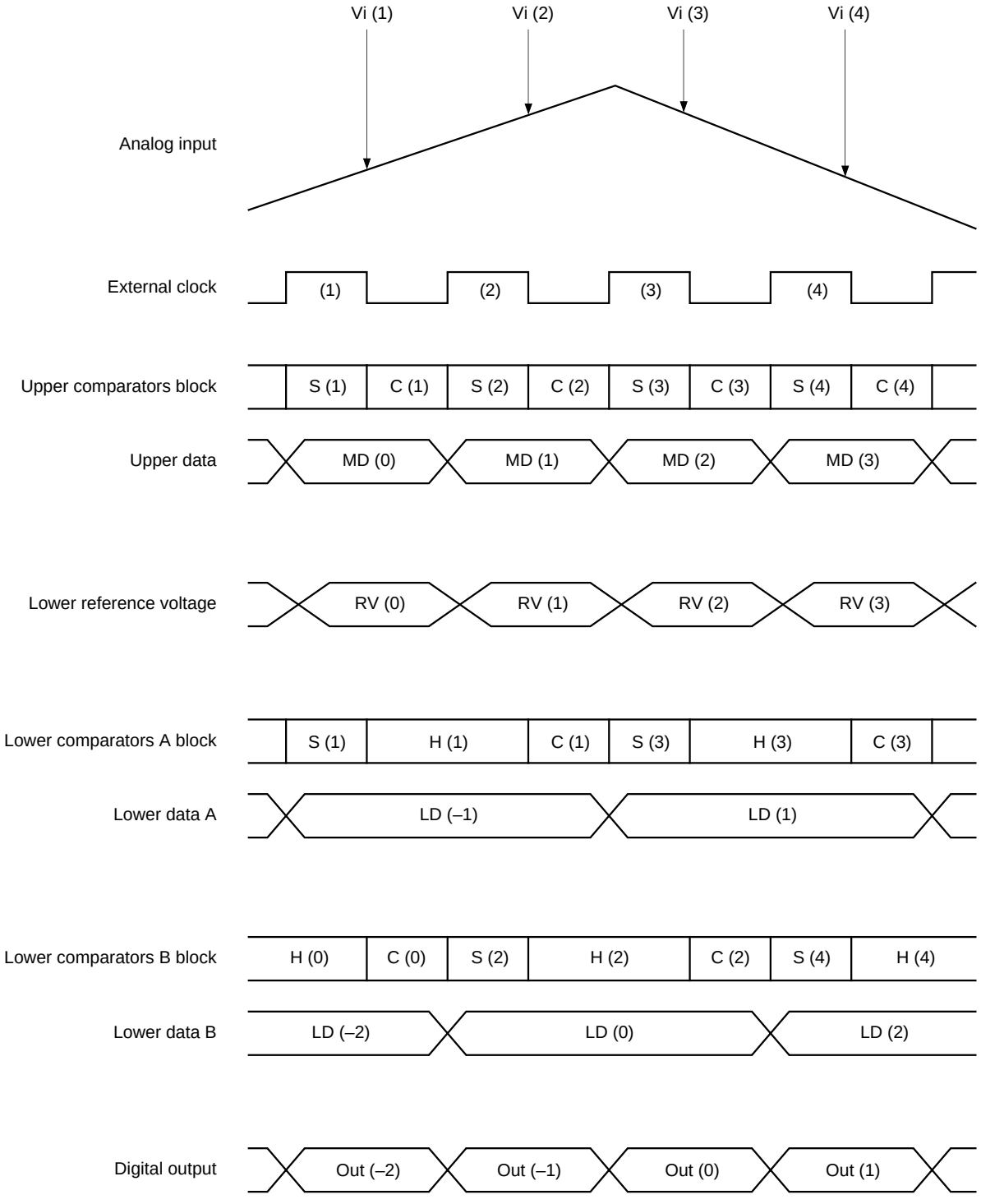
Differential gain error
Differential phase error } **test circuit**



Digital output current test circuit



Timing Chart II



Operation (See Block Diagram and Timing Chart II)

1. The CXD2302Q is a 2-step parallel system A/D converter featuring a 4-bit upper comparator block and 2 lower comparator blocks of 4-bit each. The reference voltage that is equal to the voltage between V_{RT} – V_{RB}/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower 4-bit comparator block. VRTS and VRBS pins serve for the self generation of V_{RT} (Reference voltage top) and V_{RB} (Reference voltage bottom), and they are also used as the sence pins as shown in the Application Circuit examples I-4 and I-5.

2. This IC uses an offset cancel type comparator which operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart II with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the Timing Chart II. For instance input voltage Vi (1) is sampled with the falling edge of the external clock (1) by means of the upper comparator block and the lower comparator A block.
   The upper comparator block finalizes comparison data MD (1) with the rising edge of the external clock (2). Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator A block finalizes comparison data LD (1) with the rising edge of the external clock (3). MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the external clock (4). Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small.
   However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability.
   When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by insetting a resistance of about 33Ω in series between the amplifier output and A/D input.
   When the V_{IN} signal of pin No. 21 is monitored, the kickback noise of clock is. However, this has no effect on the characteristics of A/D conversion.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference input
   Voltage V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1µF, stable characteristics are obtained. By shorting V_{DD} and V_{RTS}, V_{SS} and V_{RBS} respectively, the self-bias function that generates V_{RT}=about 2.5V and V_{RB}=about 0.6V, is activated.

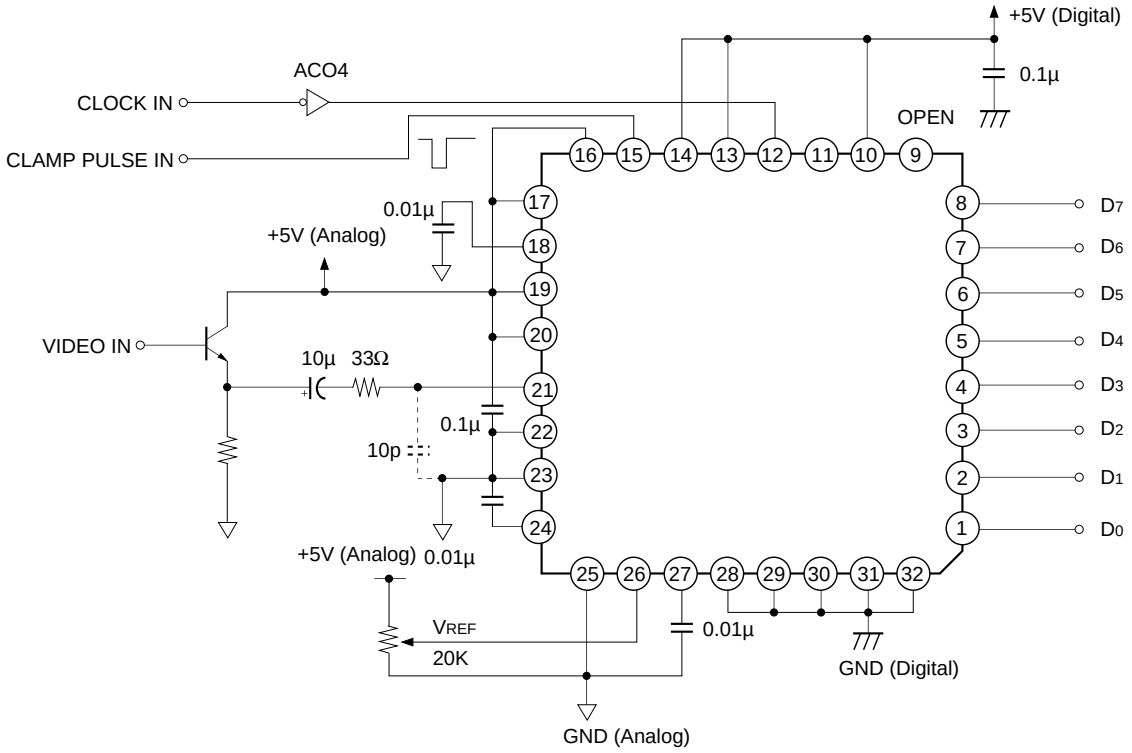
5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data synchronized with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 9ns (DV_{DD} = 5V).

6. $\overline{OE}$ pin
   Pins 1 to 8 (D_0 to D_7) are in the output mode by leaving $\overline{OE}$ open or connecting it to DV_{SS}, and they are in the high impedance mode by connecting it to DV_{DD}.

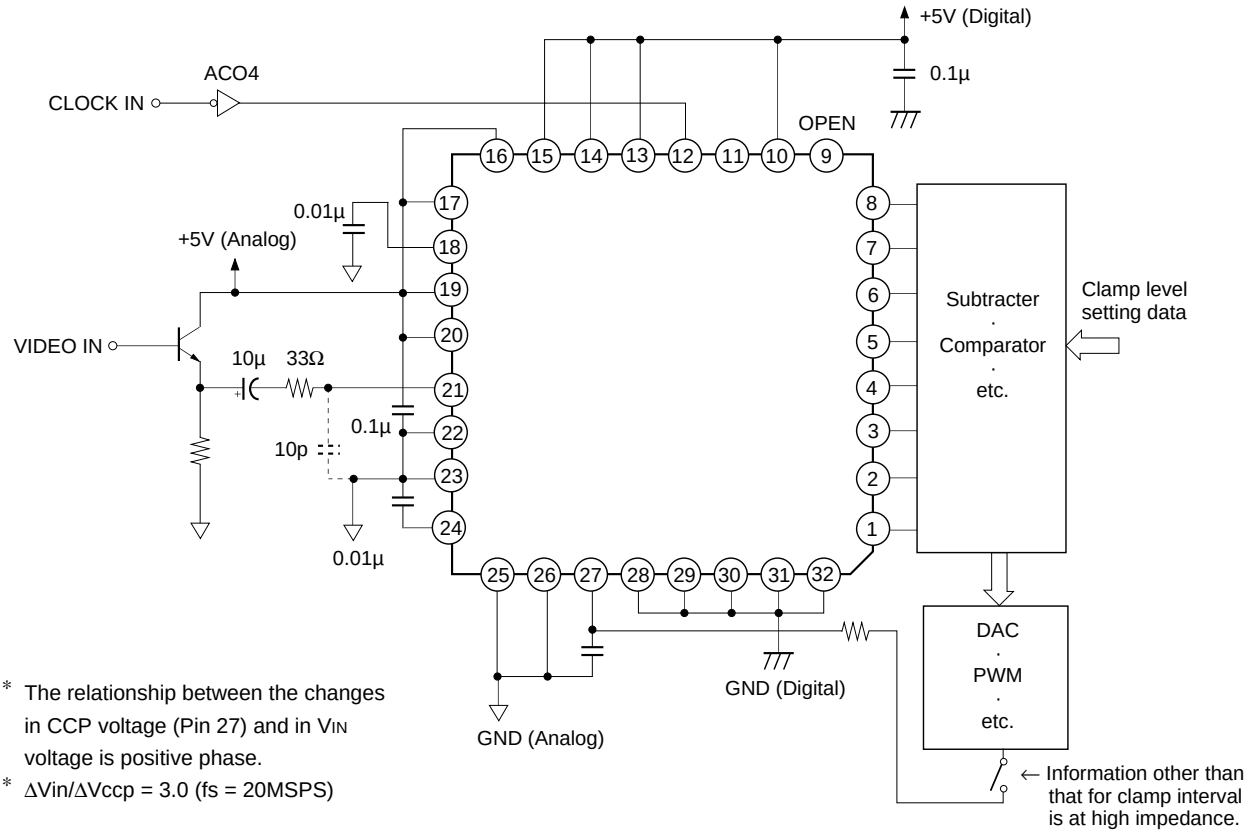
Application Circuit

I. Single +5V Power Supply

I-1. When clamp is used (self-bias used)



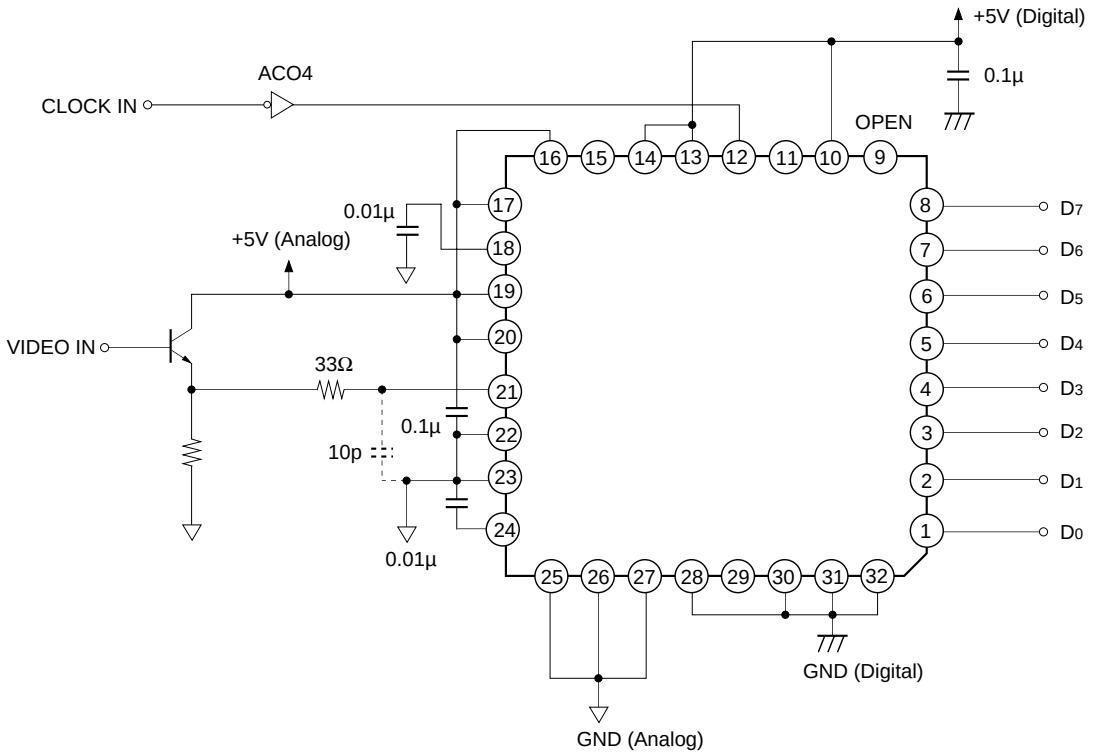
I-2. Digital clamp (self-bias used)



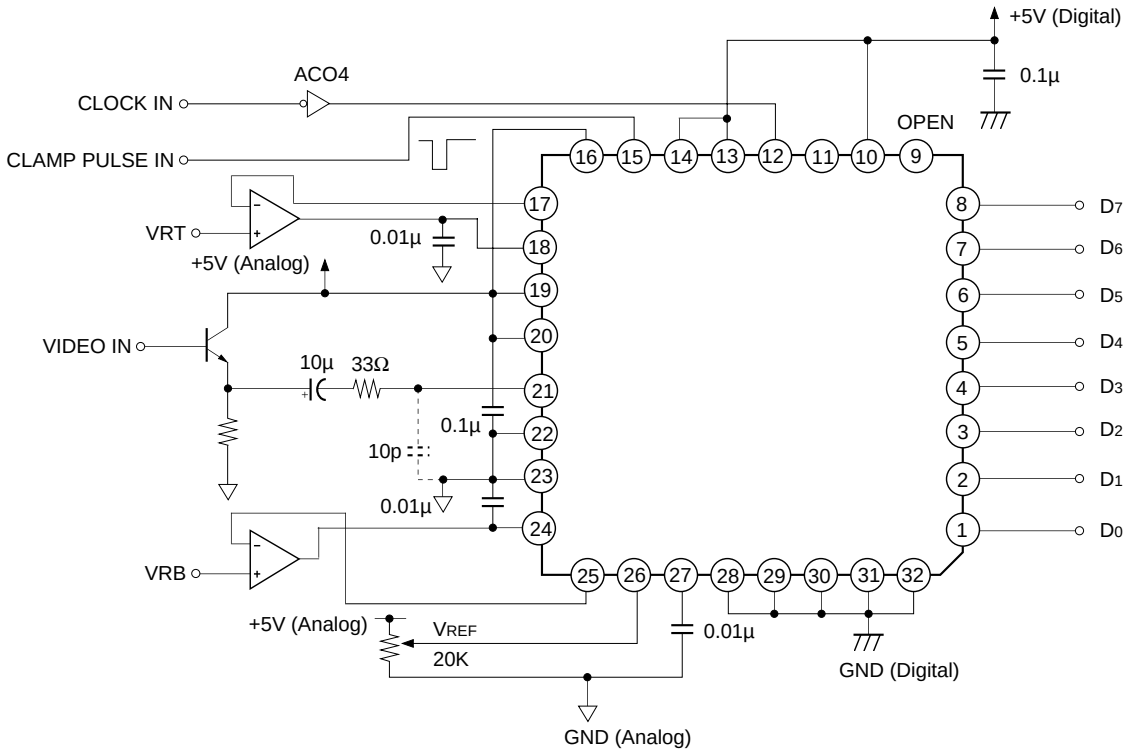
* The relationship between the changes in CCP voltage (Pin 27) and in V_{IN} voltage is positive phase.

* $\Delta Vin/\Delta Vccp = 3.0$ (fs = 20MSPS)

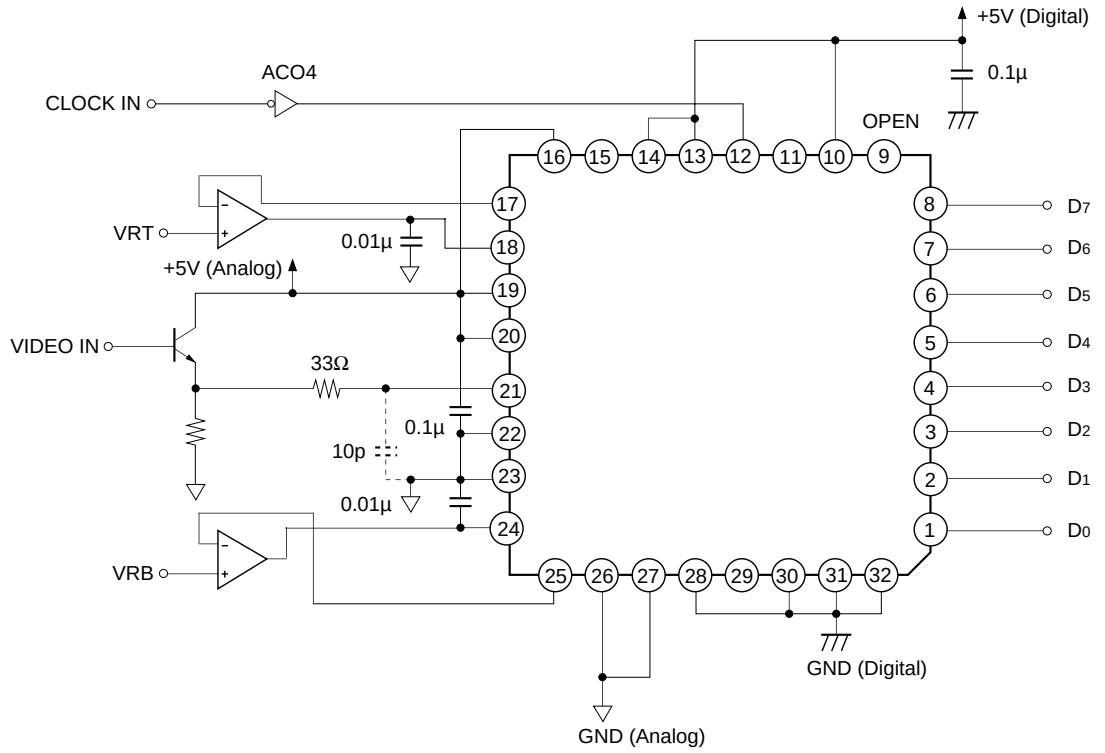
I-3. When clamp is not used (self-bias used)



I-4. When clamp is used (self-bias not used)

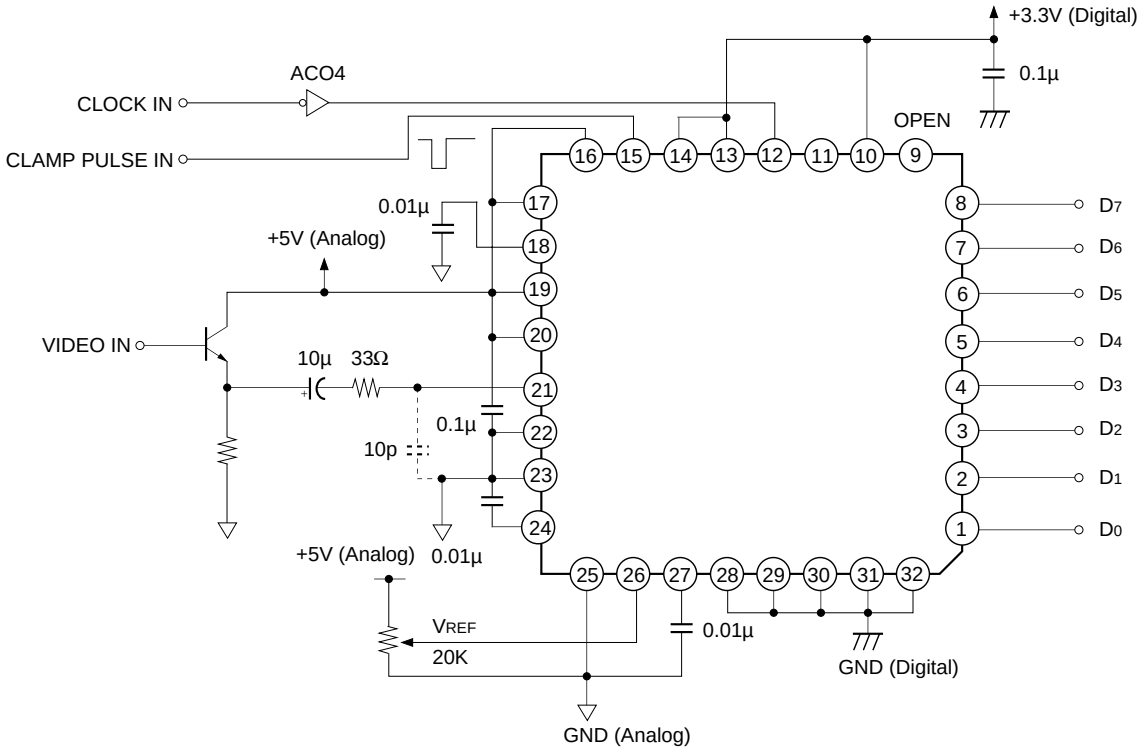


I-5. When clamp is not used (self-bias not used)



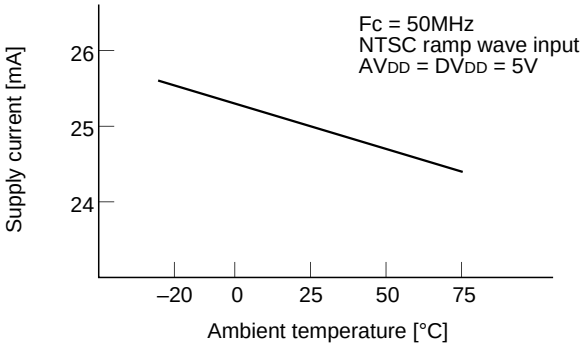
II. Dual +5V/+3.3V Power Supply

II-1. When clamp is used (self-bias used)

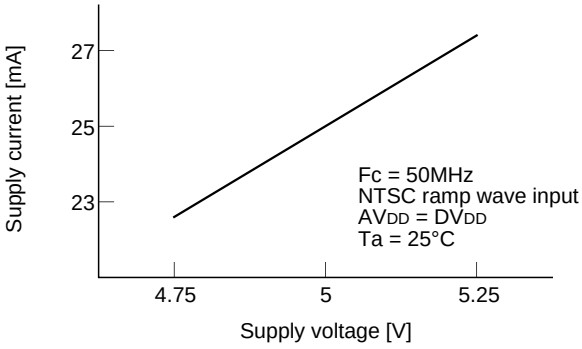


Example of Representative Characteristics

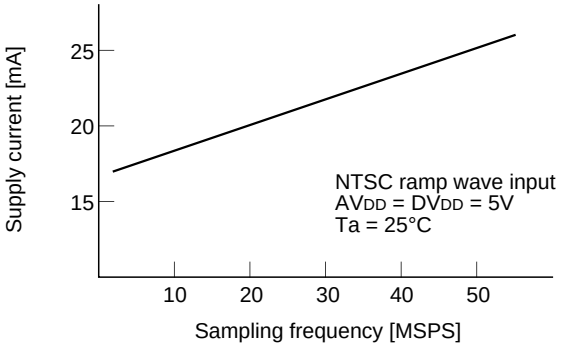
Ambient temperature vs. Supply current



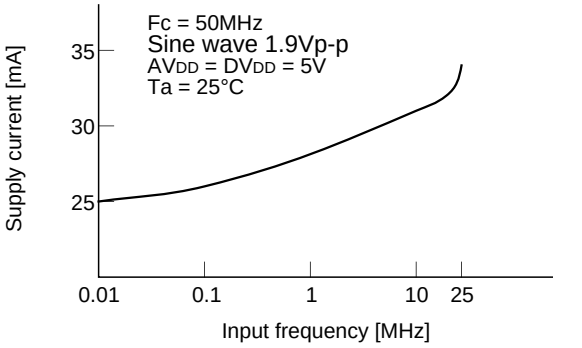
Supply voltage vs. Supply current



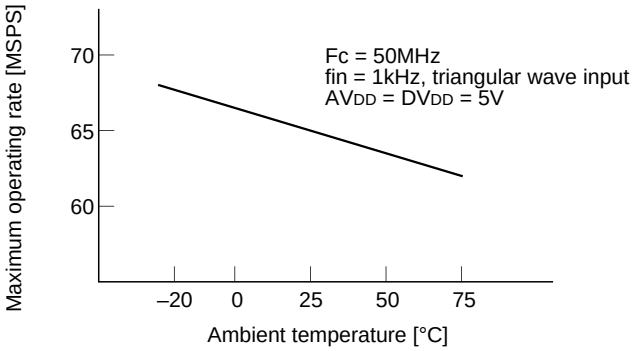
Sampling frequency vs. Supply current



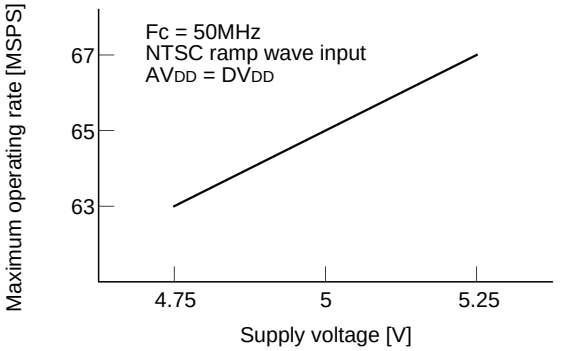
Input frequency vs. Supply current



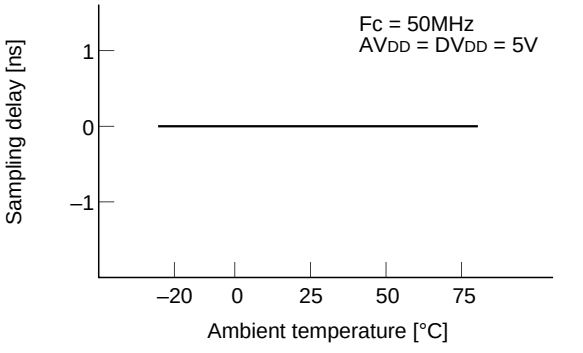
Ambient temperature vs. Maximum operating frequency



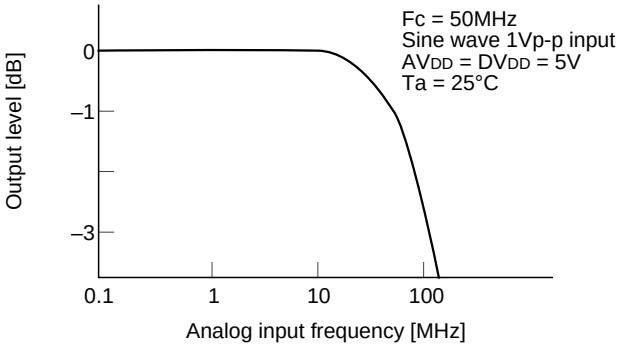
Supply voltage vs. Maximum operating frequency



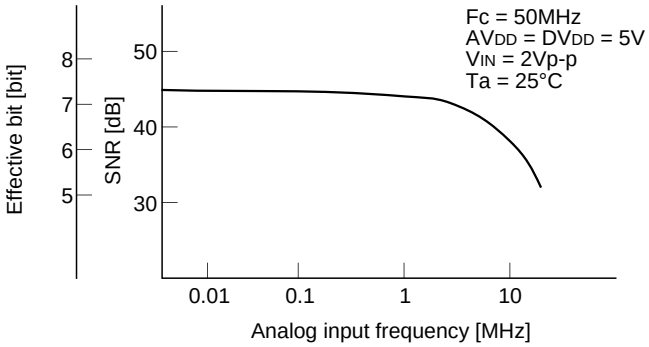
Ambient temperature vs. Sampling delay



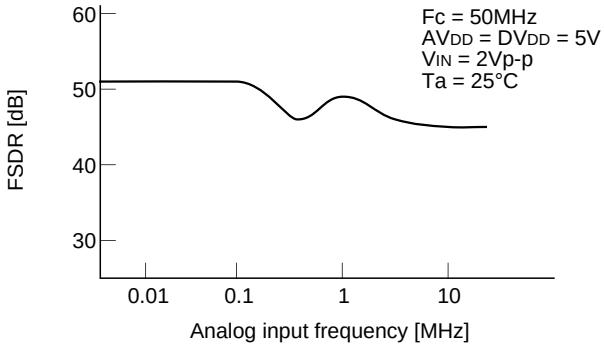
Analog input band



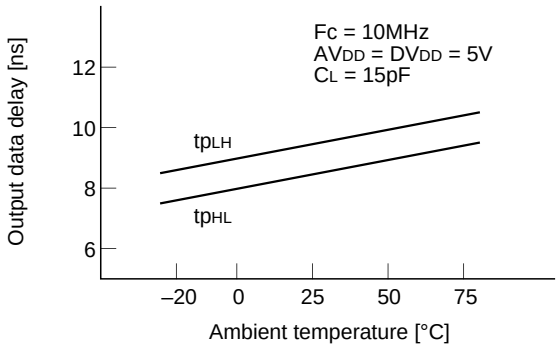
Analog input frequency vs. SNR, effective bit



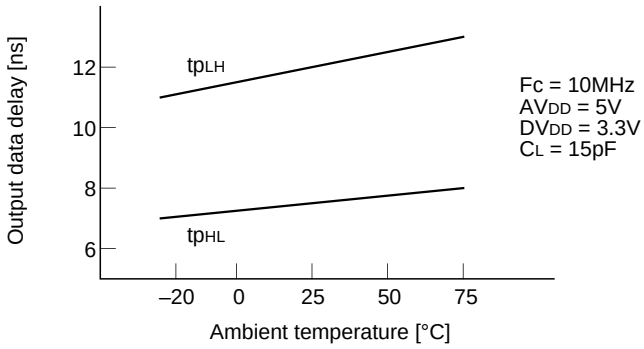
Analog input frequency vs. FSDR



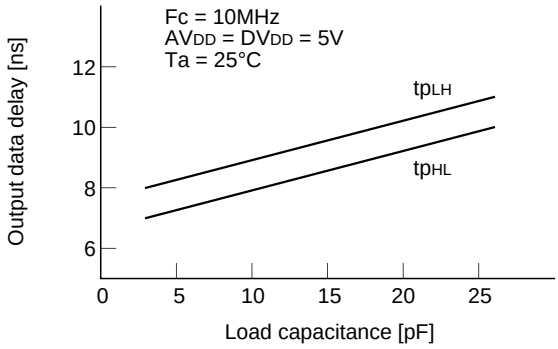
Ambient temperature vs. Output data delay



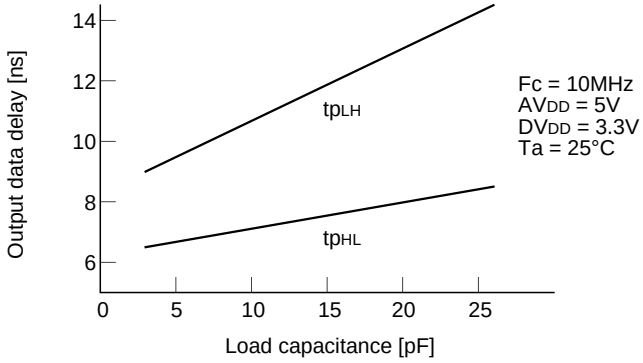
Ambient temperature vs. Output data delay



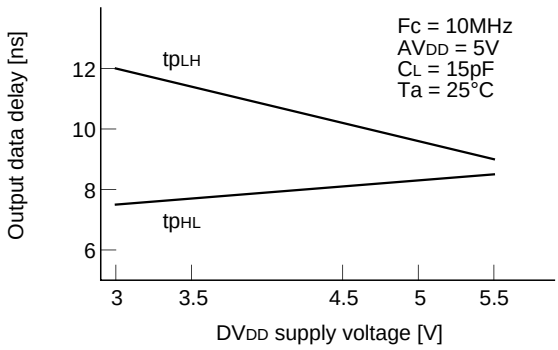
Load capacitance vs. Output data delay



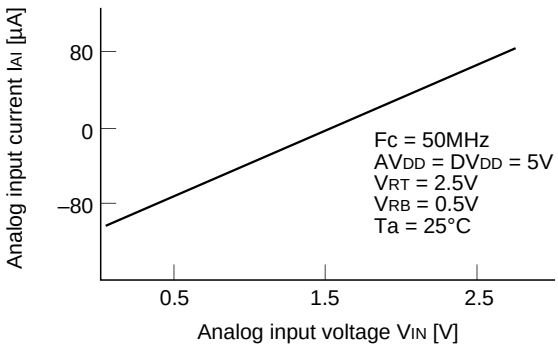
Load capacitance vs. Output data delay



DVDD supply voltage vs. Output data delay



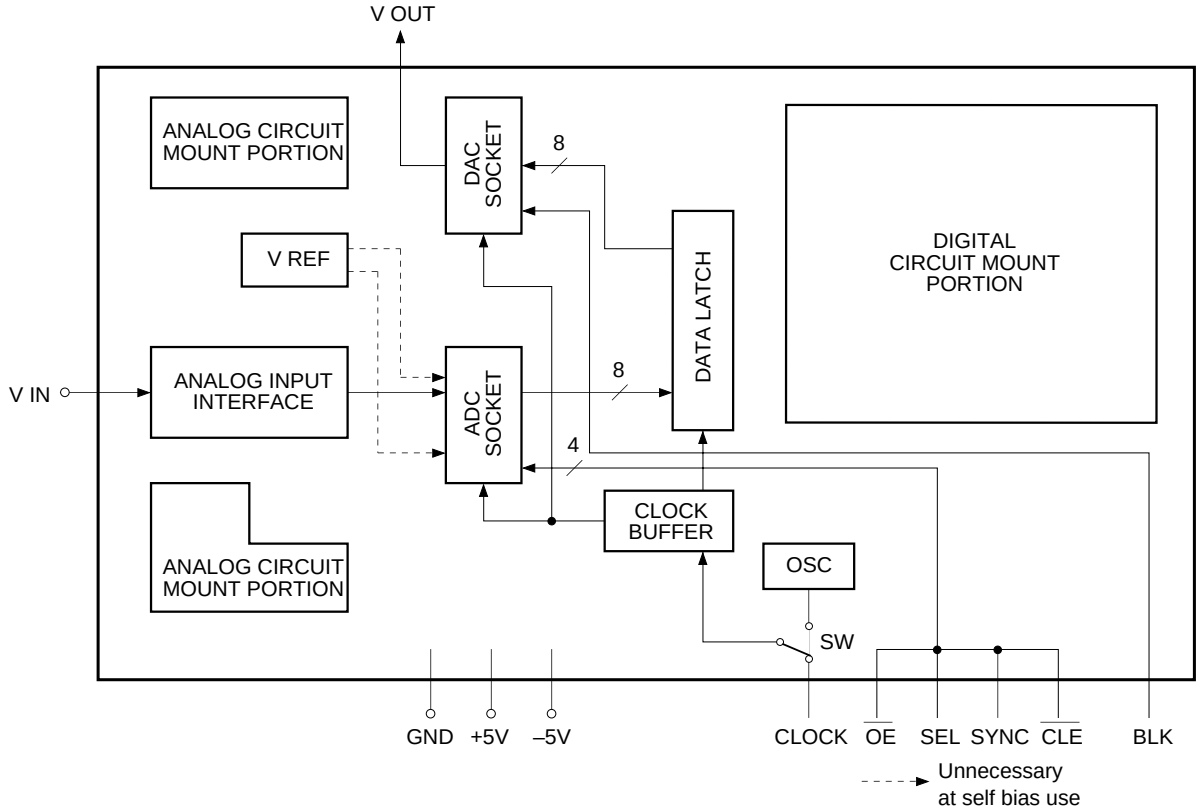
Analog input voltage vs. Input current



8-bit 50MSPS ADC and DAC Evaluation Board

Evaluation boards are available for the high speed, low power consumption CMOS converters CXD2302Q (8-bit 50MHz A/D) and CXD1171M (8-bit 40MHz D/A).
The evaluation boards are composed of a main board, CXD2302Q sub board and CXD1171M sub board. The each board is connected with sockets.
An input interface, clock buffer and latches are mounted on the main board. The CXD2302Q and CXD1171M are mounted on each of the sub boards. Those ICs are mounted according to recommended print patterns designed to provide maximum performance to the A/D and D/A converters.

Block Diagram



Characteristics

- Resolution 8bit
- Maximum conversion rate 50MHz
- Digital input level CMOS level
- Supply voltage ±5.0V (Single +5V power supply possible at self bias use)

Supply voltage

Item	Min.	Typ.	Max.	Unit
+5V –5V			185 20	mA

Clock input

CMOS compatible

Pulse width T_{CW1} 10ns (min)

T_{CW0} 10ns (min)

Analog Output (CXD1171M) (R_L > 10kΩ)

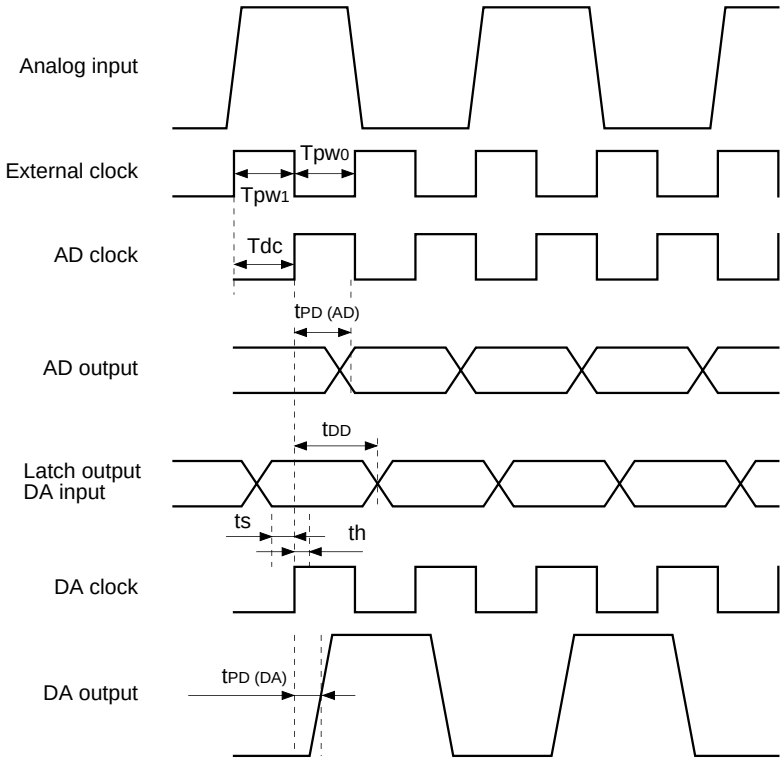
Item	Min.	Typ.	Max.	Unit
Analog output	1.8	2.0	2.1	V

Output Format (CXD2302Q)

The table shows the output format of AD Converter.

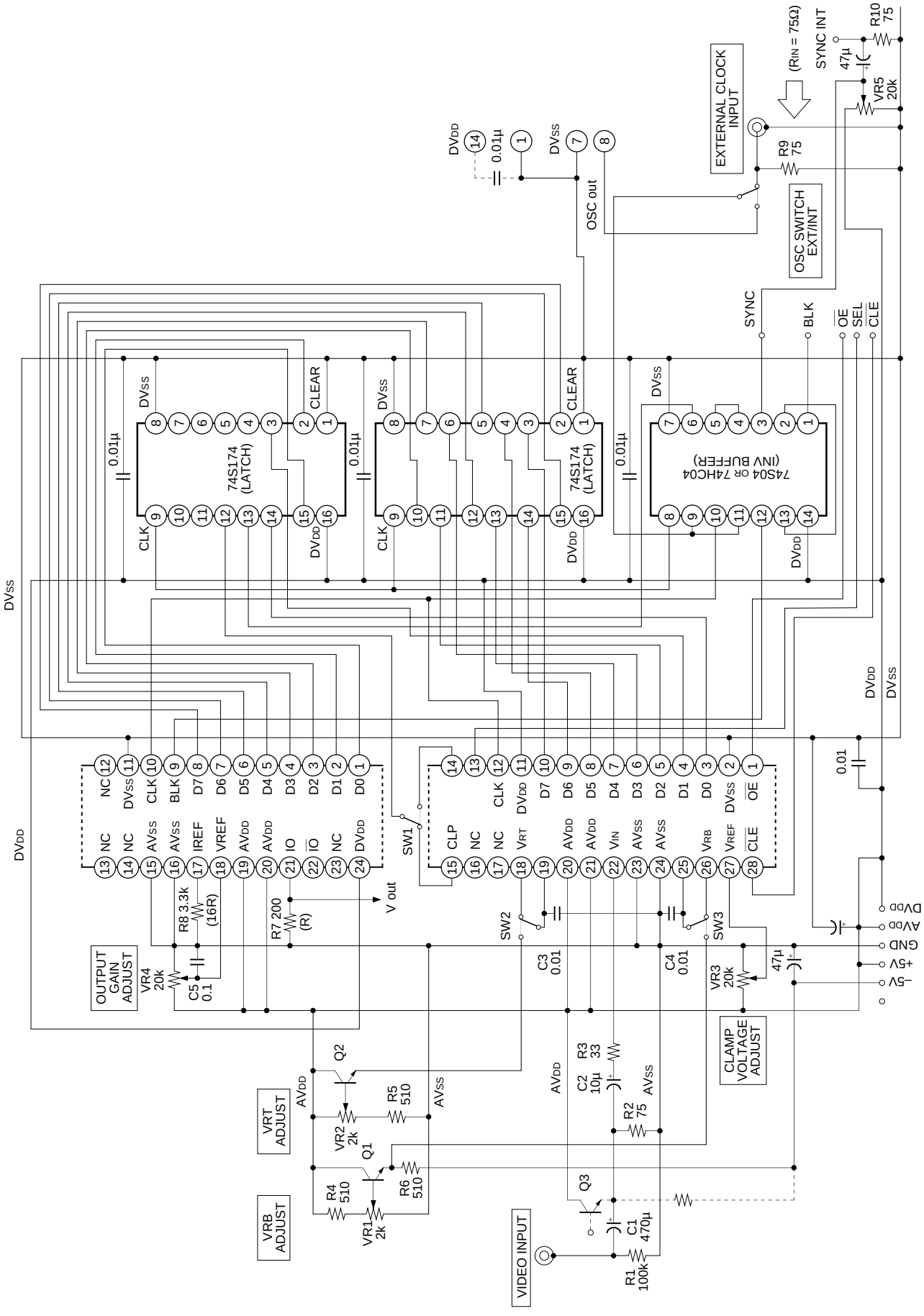
Analog input voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
:	:	:
:	127	1 0 0 0 0 0 0 0
:	128	0 1 1 1 1 1 1 1
:	:	:
V_{RB}	255	0 0 0 0 0 0 0 0

Timing Chart

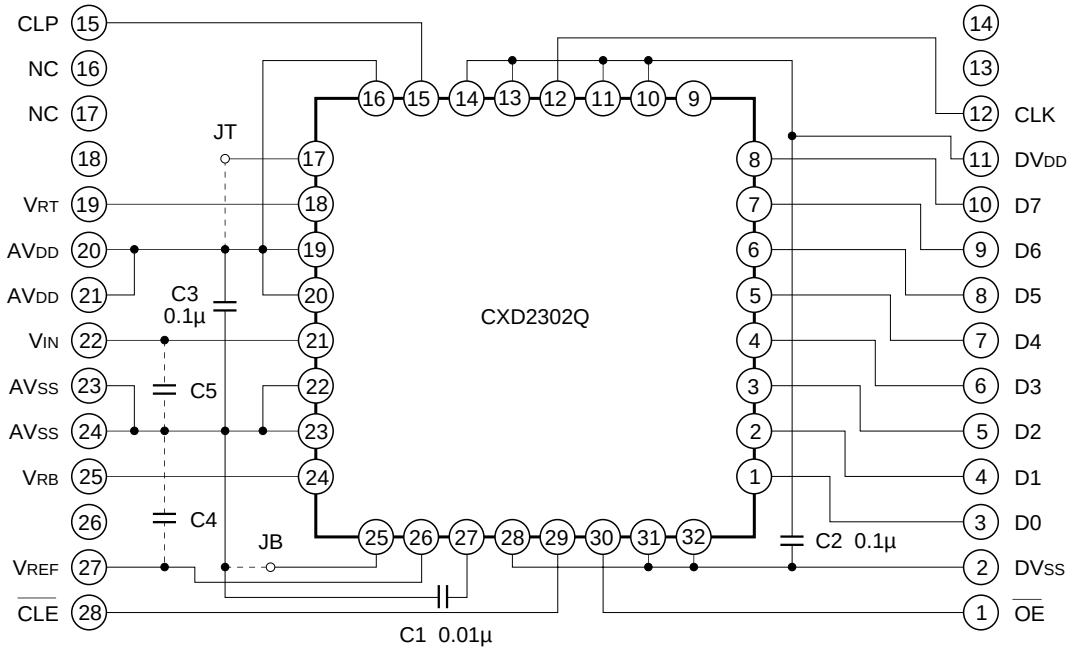


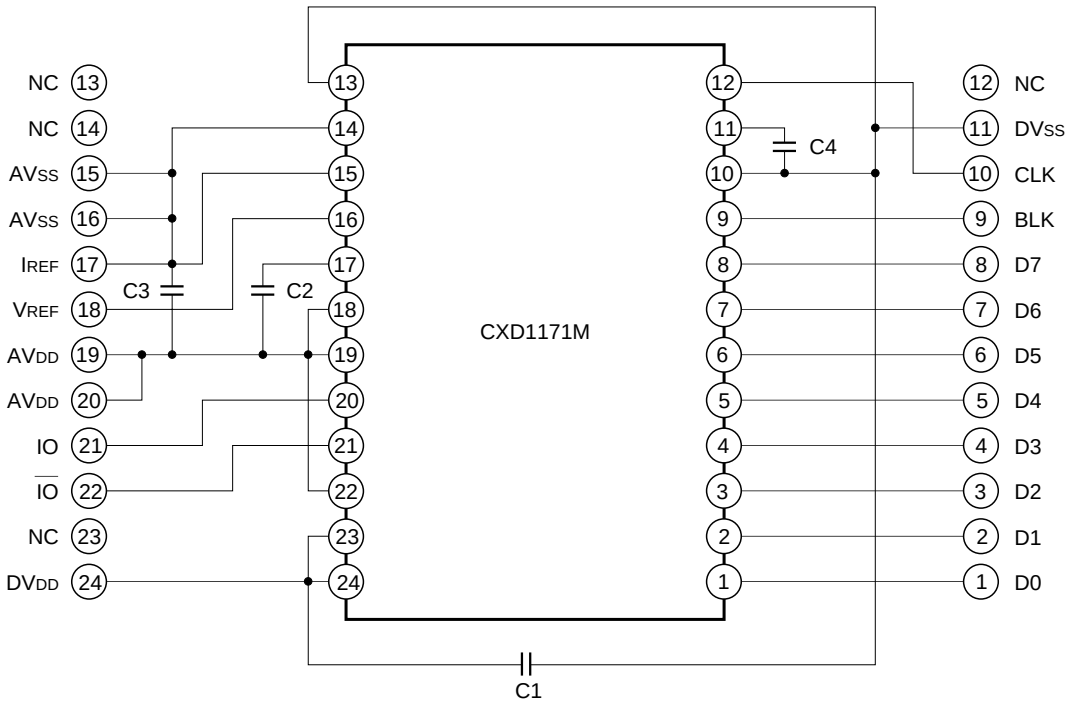
Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	10			ns
Clock Low time	T_{PW0}	10			ns
Clock Delay	Tdc			24	ns
Data delay AD	$t_{PD\ (AD)}$		9		ns
Data delay (latch)	t_{DD}			17	ns
Settling time	t_S	5			ns
Hold time	th	10			ns
Data delay DA	$t_{PD\ (DA)}$		10		ns

CMOS ADC/DAC Peripheral Circuit Board (Main Board)



CMOS ADC/DAC Peripheral Circuit Board (Sub Board)





List of Parts

resistance

R1	100K
R2	75Ω
R3	75Ω
R4	510Ω
R5	510Ω
R6	510Ω
R7	R = 200
R8	18R ≈ 3.3K
R9	75Ω
R10	75Ω
VR1	2K
VR2	2K
VR3	20K
VR4	20K
VR5	20K

capacitance

C1	470µF/6.3V (chemical)
C2	10µF/16V (chemical)
C3	0.01µF
C4	0.01µF
C5	0.1µF
C6	0.1µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	47µF/10V (chemical)
C12	47µF/10V (chemical)
C13	47µF/10V (chemical)
C14	0.1µF

transistor

Q1	2SC2785
Q2	2SC2785
Q3	2SC2785

IC

IC1	74S174
IC2	74S174
IC3	74S04

oscillator

OSC

others

connector	BNC071
SW	AT1D2M3

Adjustment

1. Vref adjustment (VR1, VR2)
   Adjustment of A/D converter reference voltage. VRB is adjusted through VR1 and VRT through VR2. When self bias is used, there is no need for adjustment. Reference voltage is set through self bias delivery.

2. Setting of clamp reference voltage (VR3)
   Clamp reference voltage is set.

3. DAC output full scale adjustment (VR4)
   Full scale voltage of D/A converter output is adjusted at the PCB shipment, the full scale voltage is adjusted to approx. 2V.

4. Sync (clamp) pulse interface (VR5)
   This adjustment enables interface with the signal generator and others at the PCB shipment, adjustment is performed to obtain a threshold of approx. 2.5V to an H sync of 0 to 5V.

5. $\overline{OE}$, SEL, Sync, BLK, $\overline{CLE}$, Sync INT
   The following pins are set on the main board: $\overline{OE}$, Sync, $\overline{CLE}$, Sync INT (CXD2302Q), BLK (CXD1171M) and SEL (not used). For the pins function, refer to the Pin Description. The difference between Sync pin and Sync INT pin is that a pulse above 3.5Vp-p should be input to Sync INT pin. The pulse threshold is set through VR5. For input through Sync pin, pulse is input at TTL or CMOS level. In this case cut off the junction line between Sync and Sync INT pin.
   At the PCB shipment the main board pins are set as follows.
   - $\overline{OE}$: Low (A/D output ON)
   - SEL : Low
   - Sync : Line junction Sync INT pin
   - $\overline{CLE}$: Low (Clamp function ON)
   - BLK : Low (Blanking OFF)

6. Clamp pulse input method
   Directly input the clamp pulse as shown in Application Circuit example I-1. As SW1 is set to direct input at the PCB shipment, use it in this position.

Points on the PCB Pattern Layout

1. Set the layout not to have Digital current flow into Analog GND (For 1, see p.24 “Component side diagram”.).

2. The C_2 and C_3 capacitors for the CXD2302Q sub board serve the important role of bringing out ICs full performance.
   Connect over 0.1µF (ceramic) capacitors with good high frequency characteristics as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) are on a common voltage supply source. Keeping ADC’s DV_{SS} (For 2, see p.24 “Component side diagram”.) as close to the voltage supply source as possible will provide better characteristics. That is, a layout where ADC is close to the voltage supply source, is recommended.

4. ADC samples analog signals at the clock falling edge. Accordingly it is important that clocks supplied to ADC do not have any jitter.

5. The PCB layout shows ADC and DAC’s Analog GND independently from the voltage supply source. The layout aims at providing an independent evaluation of ADC and DAC, as much as possible. On the actual board, common use will not cause any problems.

Notes on Operation

1. Reference voltage
   Shorting AV_{DD} and V_{RTS}, AV_{SS} and V_{RBS} will activate the self-bias function that generates V_{RT} = about 2.6V and V_{RB}=about 0.5V. On the PCB, either self bias or the external reference voltage can be selected depending on the junction method of the jumper line. At shipment from the factory, reference voltage is provided in self bias. Also, to provide external reference voltage, adjust the dynamic range (V_{RT} – V_{RB}) to above 1.8Vp-p.

2. Clock input
   There are 2 modes for the PCB clock input
   1) Provided from the external signal generator. (External clock)
   2) Using the crystal oscillator (built-in clock driver). (Internal clock)

   The 2 modes are selected using the switch on the PCB.

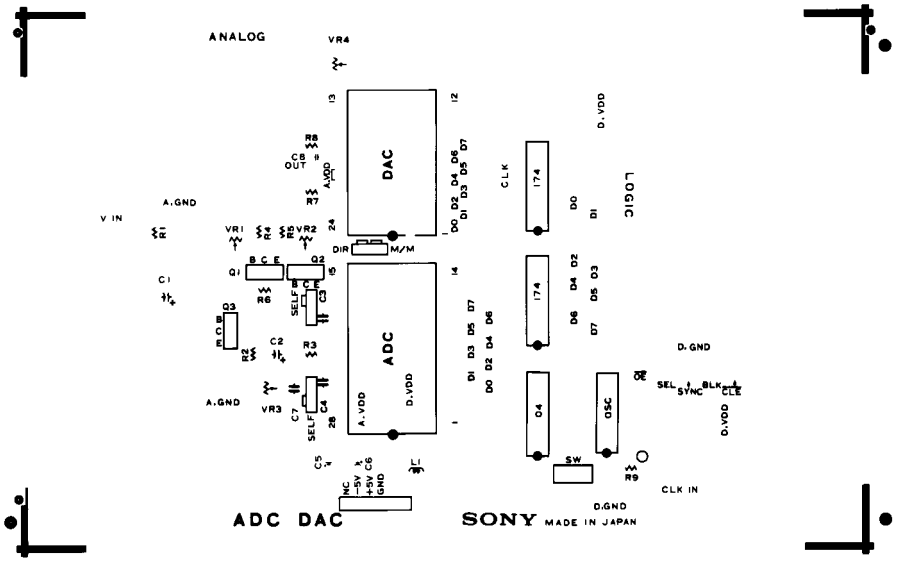
3. The 2 Latch ICs (74S174) are not absolutely necessary for the evaluation of ADC and DAC. That is, operation will still be normal if ADC output data is directly input to DAC input. However, as ADC output data is hardly ever D/A converted without executing Digital signal processing, it was mounted to indicate an example layout of Digital signal processing IC. Use the Latch IC output when the ADC output data is used.

4. When clamp is not used
   Turning $\overline{CLE}$ to H will set OFF the clamp function. In this case, the DC element is cut off by means of C_2 on the main board and DC voltage on the ADC side of C_2 turns to about (V_{RT}+V_{RB})/2. To transfer DC elements of input signals, short C_2. At that time, it is necessary to bias input signals, but keeping R_2 open, Q_3 can also be used as buffer. Use the open space for the bias circuit.

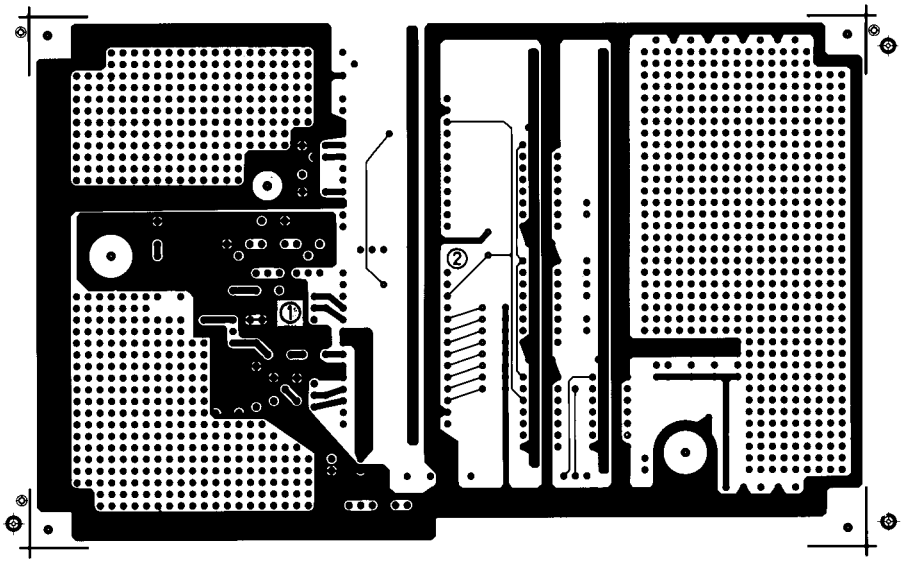
5. Clamp pulse latch
   On the evaluation board, the clamp pulse is latched with ADC sampling CLK and then input to CLP pin. However, the latch is incorporated in CLP pin of the CXD2302Q, so that the external latch is not required.

6. Peripheral through hole
   There is a group of through holes on the Analog input, output and Logic. There are to be used when mounting additional circuits to the PCB. Use when necessary.
   The connector hole on DAC part is used to mount the test chassis mount jack.

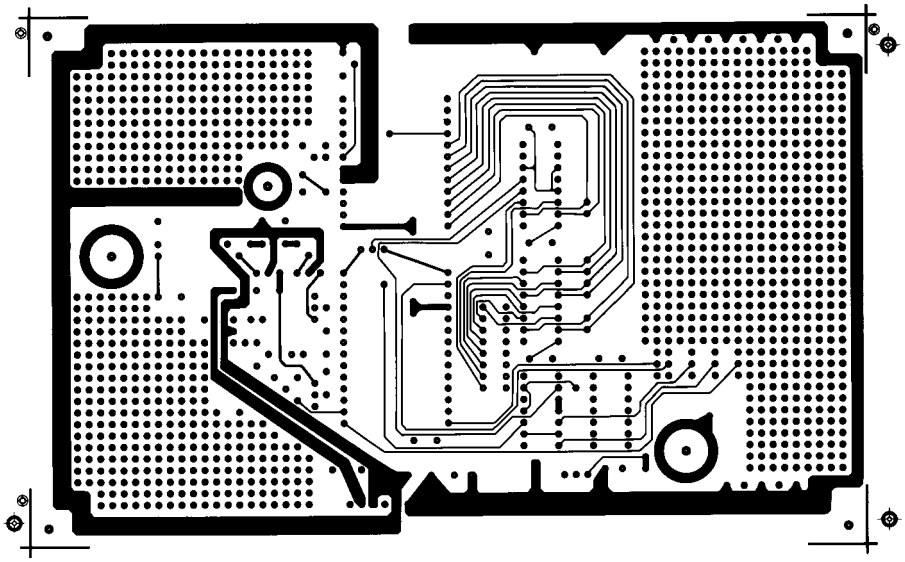
Silk Side



Component Side

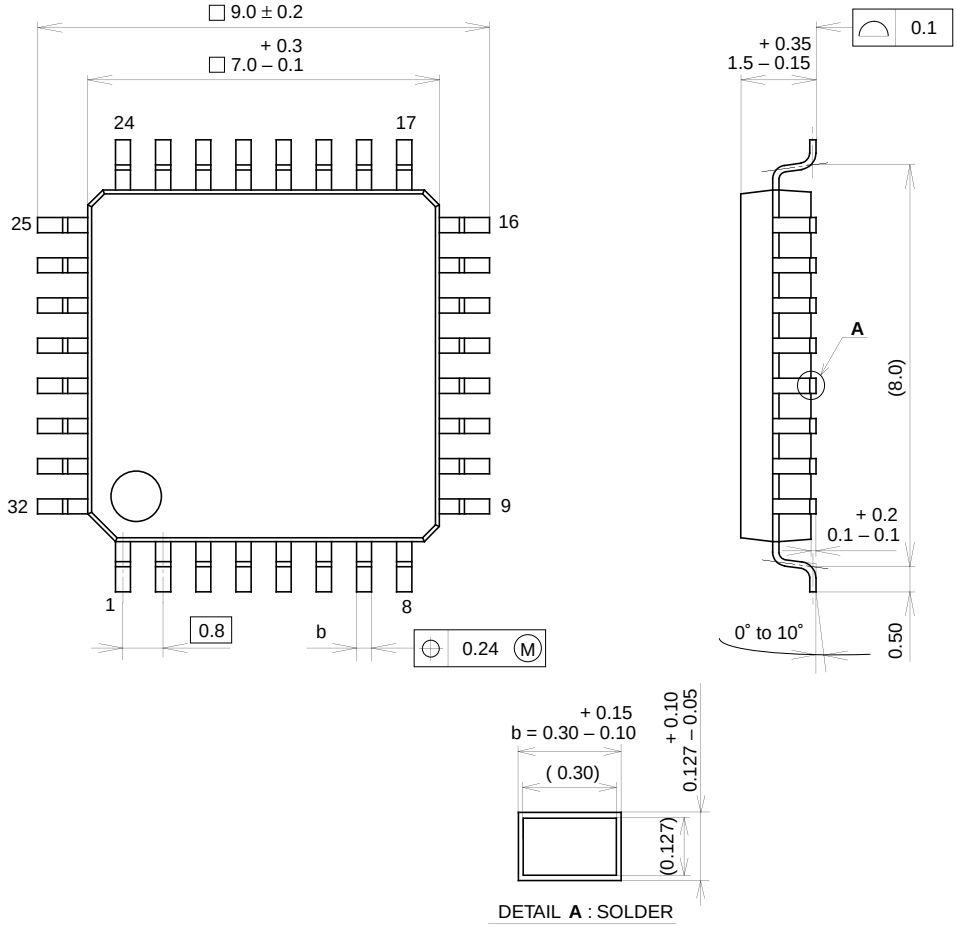


Soldering Side (Diagram seen from the component side)



Package Outline Unit: mm

32PIN QFP (PLASTIC)

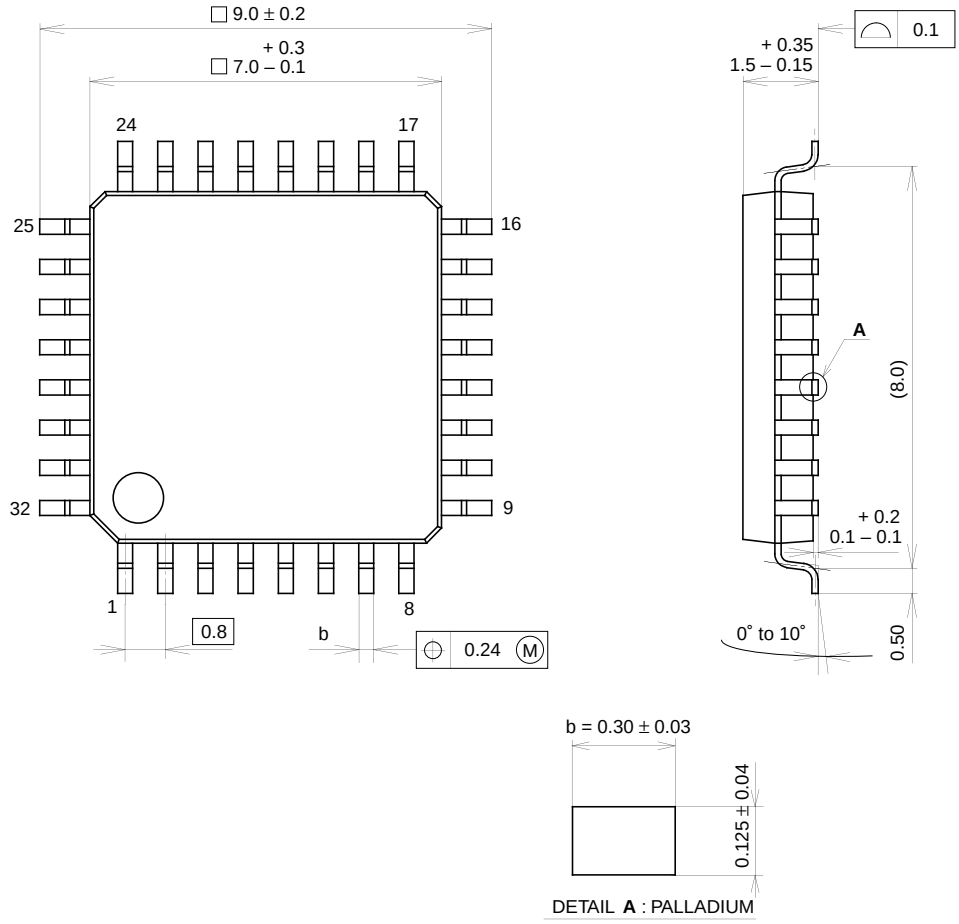


SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g