SONY

CXD2308Q

10-bit 50MSPS RGB 3-channel D/A Converter

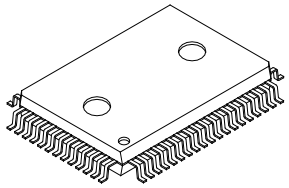
Description

The CXD2308Q is a 10-bit high-speed D/A converter for video band, featuring RGB 3-channel I/O. This is ideal for use in high-definition TVs and high-resolution displays.

Features

- Resolution 10-bit
- Maximum conversion speed 50MSPS
- RGB 3-channel I/O
- Differential linearity error ±0.5LSB
- Low power consumption; 500mW (Typ.)
- Single +5V power supply
- Low glitch

64 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

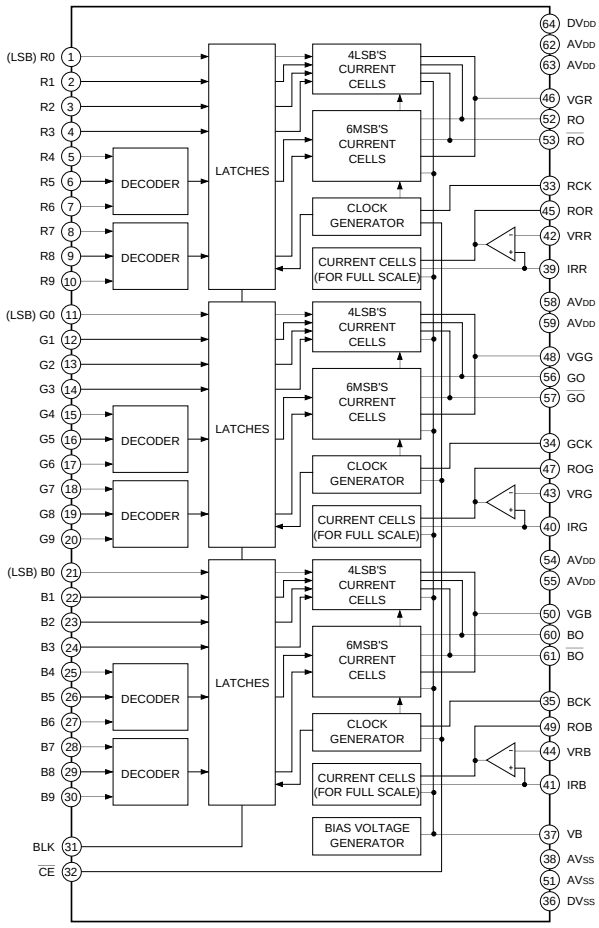
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	T_{PW1}	10 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	–20 to +75	°C

Absolute Maximum Ratings (Ta = 25°C)

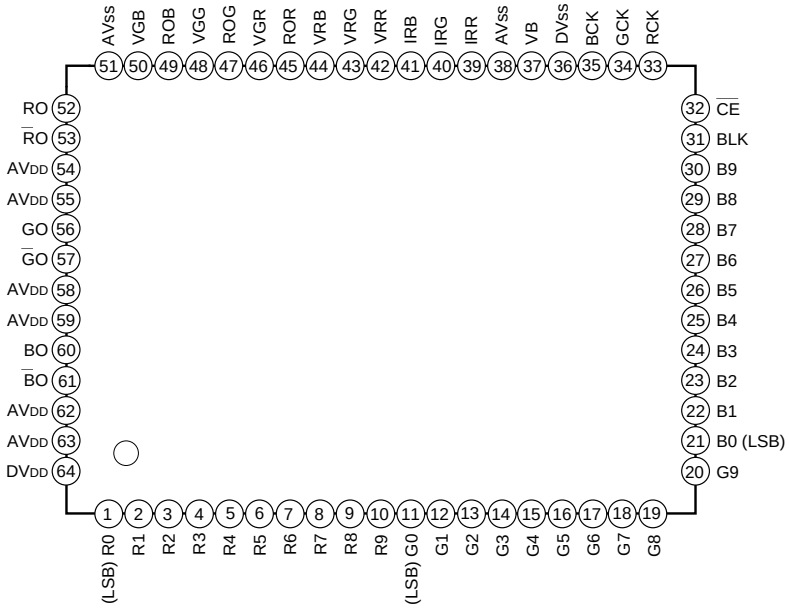
• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Output current (for each channel)	I_{OUT}	0 to 30	mA
• Storage temperature	Tstg	–55 to +150	°C

Block Diagram

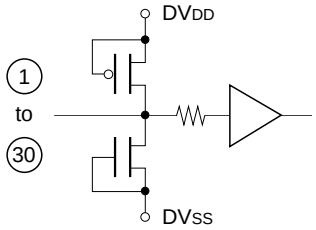
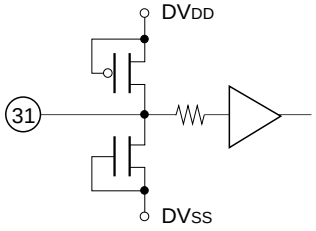
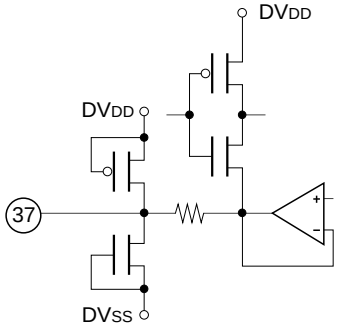
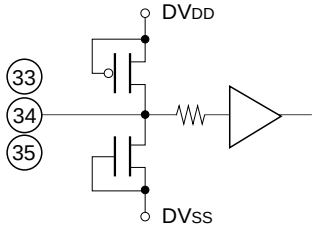


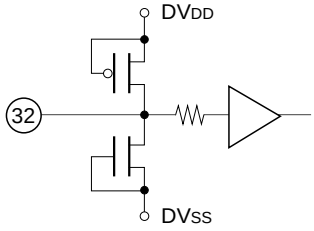
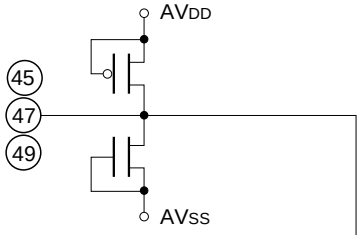
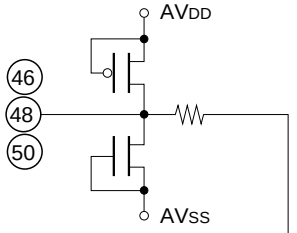
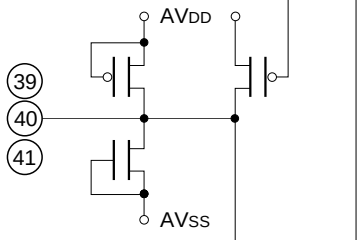
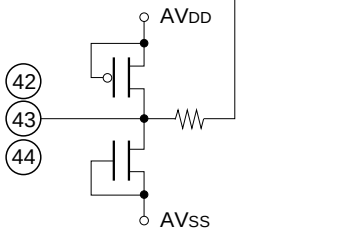
E92929B6X-PS

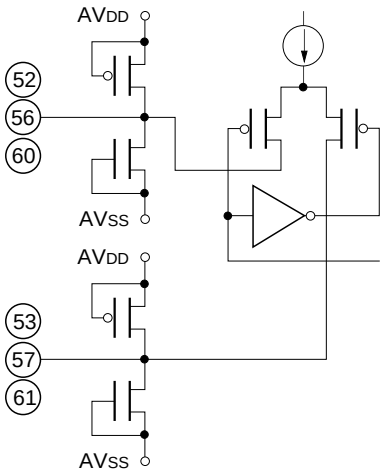
Pin Configuration



Pin Description and Equivalent Circuit

Pin No.	Symbol	Equivalent circuit	Description
1 to 10	R0 to R9		Digital input.
11 to 20	G0 to G9		
21 to 30	B0 to B9		
31	BLK		Blanking pin. No signal for High (0V output). Output generated for Low.
37	VB		Connect to DVss with a capacitor of approximately 0.1µF.
33	RCK		Clock pins. All input pins are TTL compatible.
34	GCK		
35	BCK		

Pin No.	Symbol	Equivalent circuit	Description
36	DVss		Digital GND.
38, 51	AVss		Analog GNDs.
32	$\overline{CE}$		Chip enable pin. No signal at for High (0V output) to minimize power consumption.
54, 55, 58, 59, 62, 63	AVDD		Analog VDD.
45 47 49	ROR ROG ROB		Connect to VGR, VGG and VGB with the control method of output amplitude. See Application Circuit.
46 48 50	VGR VGG VGB		Connect a capacitor of approximately 0.1µF.
39 40 41	IRR IRG IRB		Connect to AVss with a resistance of 1.2kΩ .
42 43 44	VRR VRG VRB		Set output full-scale value. (2.0V)

Pin No.	Symbol	Equivalent circuit	Description
52	RO		Current output pins. Output can be retrieved by connecting a resistance of 75Ω to AVss.
56	GO		
60	BO		
53	$\overline{RO}$		Reverse current output pins. Normally connected to AVss.
57	$\overline{GO}$		
61	$\overline{BO}$		
64	DV_{DD}		Digital V_{DD}

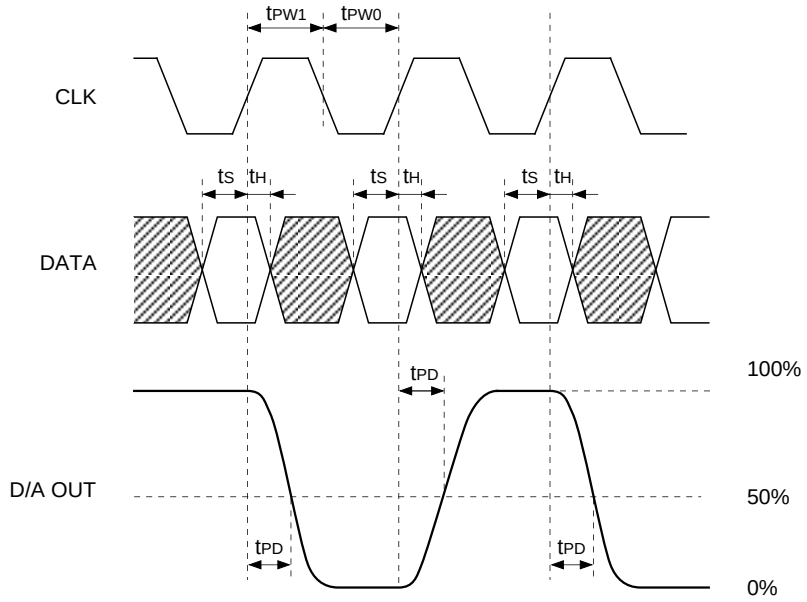
Electrical Characteristics (f_{CLK} = 50MHz, V_{DD} = 5V, R_{OUT} = 75Ω, V_{REF} = 2.0V, Ta = 25°C)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution		n			10		bit
Maximum conversion speed		f_{MAX}				50	MSPS
Minimum conversion speed		f_{MIN}		0.5			MHz
Linearity error		E_L		2.0		2.0	LSB
Differential linearity error		E_D		–0.5		0.5	LSB
Output full-scale voltage		V_{FS}		1.8	1.9	2.0	V
Output full-scale ratio *1		F_{SR}	For the same gain	0	1.5	3	%
Output full-scale current		I_{FS}			27	30	mA
Output offset voltage		V_{OS}				1	mV
Supply current		I_{DD}			100	110	mA
Digital input current	High level	I_{IH}				5	µA
	Low level	I_{IL}		–5			µA
Precision guarantee output voltage range		Voc		1.8	1.9	2.0	V
Setup time		t_S			5	7	ns
Hold time		t_H			1	3	ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE			50		pV-s
Cross talk		CT	For 10MHz sine-wave output		54		dB

*1 Output full-scale ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100\ (\%)$

Description of Operation

Timing Chart

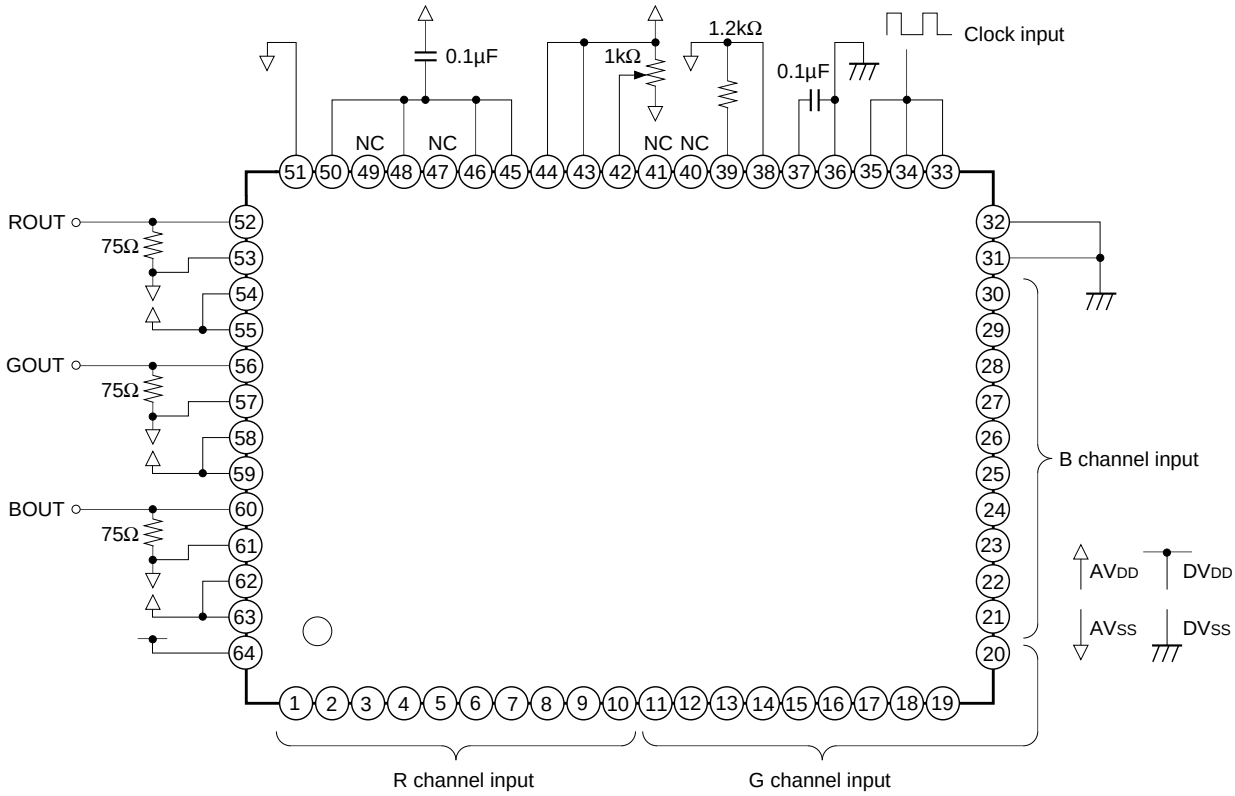


I/O Correspondence Table (output full-scale voltage: 2.00V)

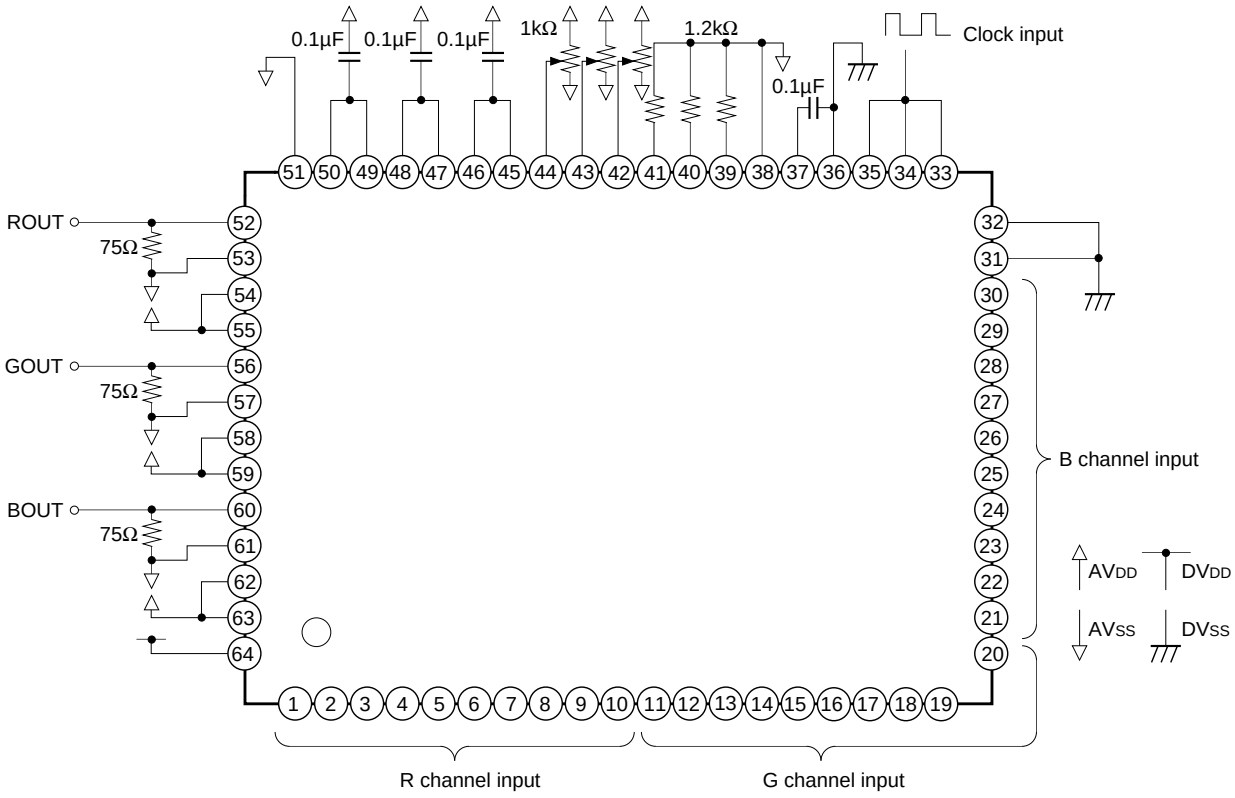
Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1 1 1	2.0V
:	
1 0 0 0 0 0 0 0 0 0	1.0V
:	
0 0 0 0 0 0 0 0 0 0	0V

Application Circuit

(Gain equal)

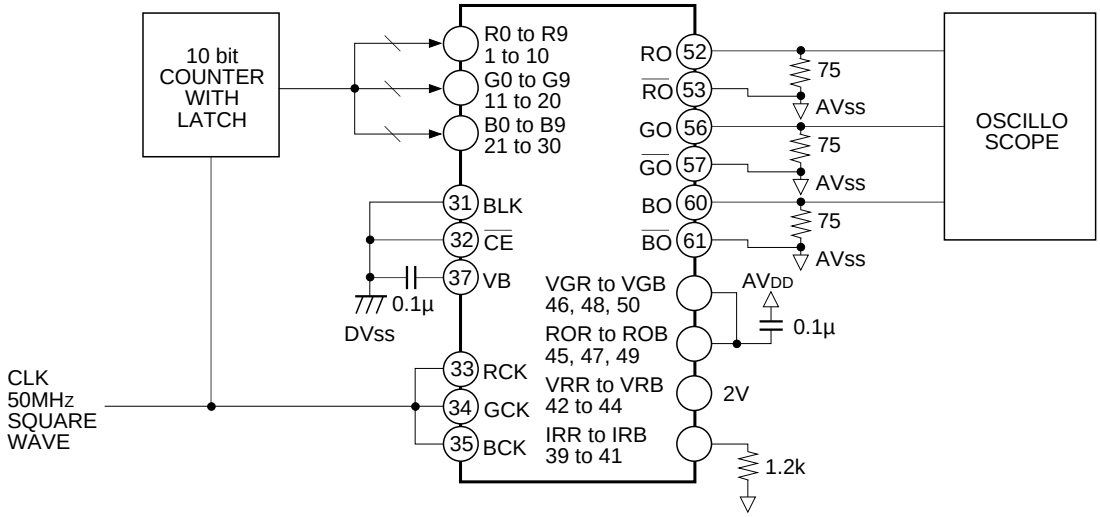


(Gain independently)

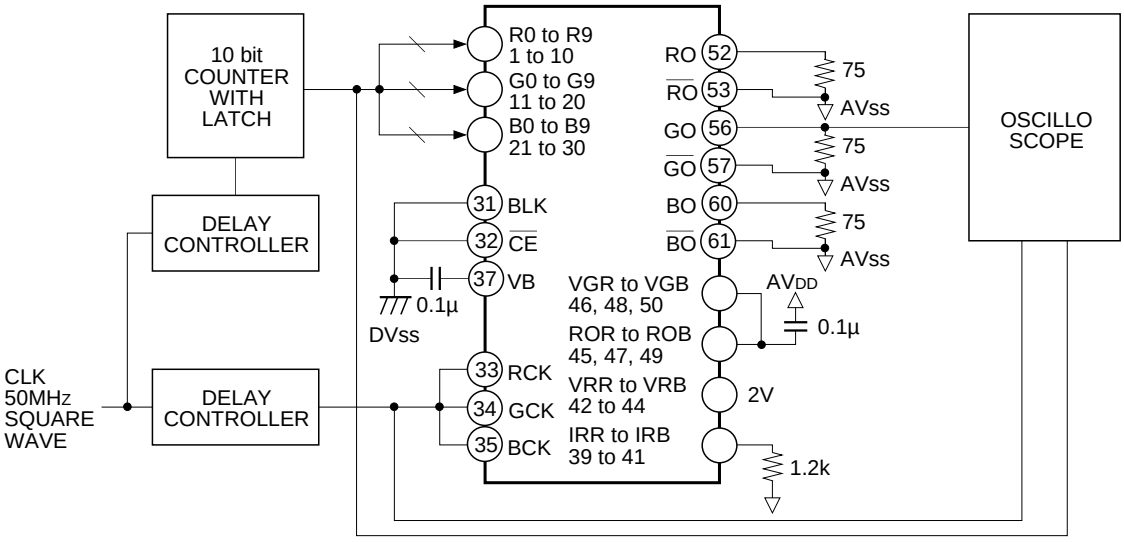


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

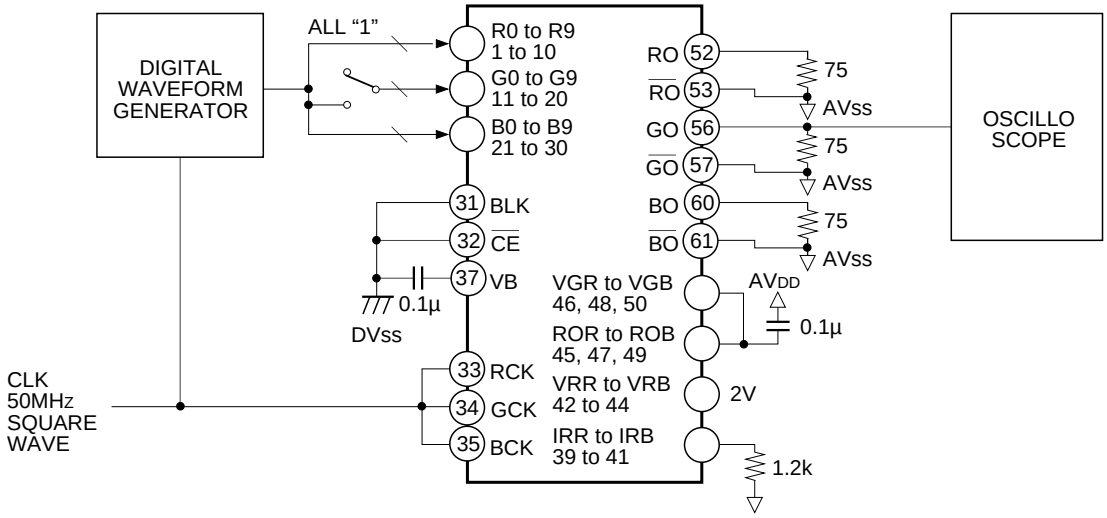
Maximum Conversion Speed Test Circuit



Setup Hold Time
Glitch Energy **Test Circuit**

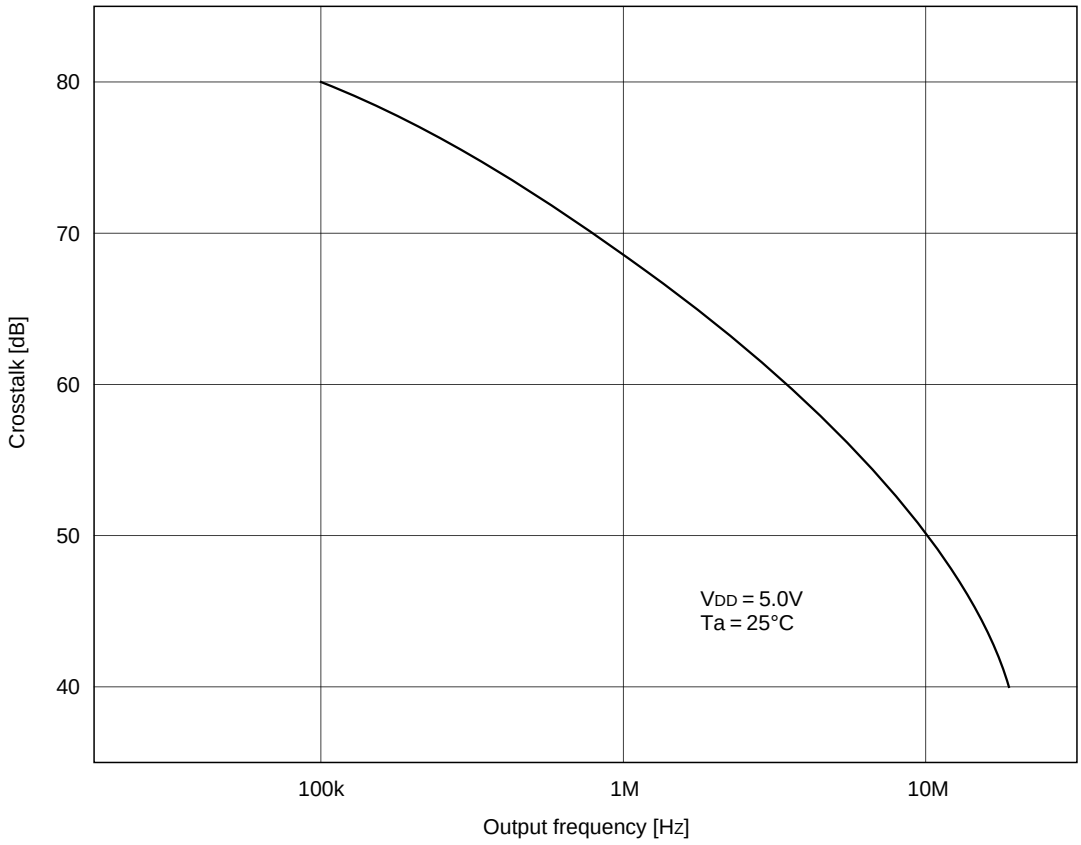


Crosstalk Test Circuit

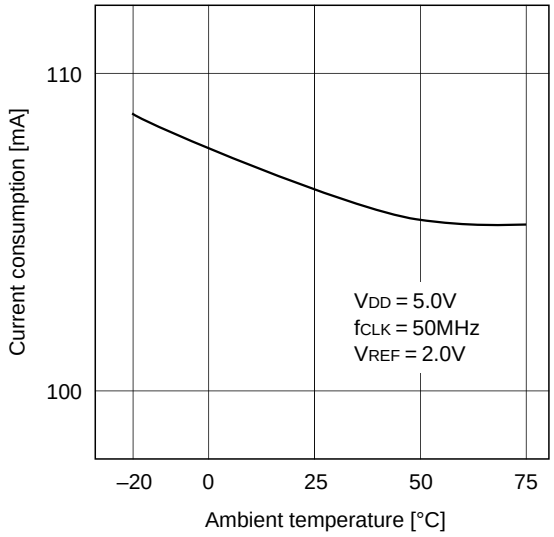


Example of Representative Characteristics

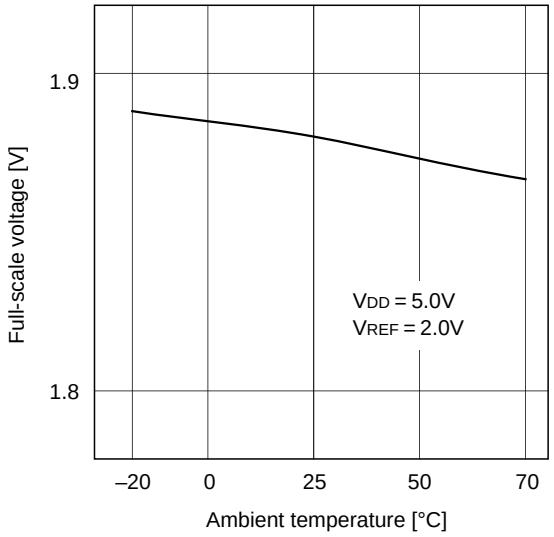
Output frequency vs. Crosstalk



Current consumption vs. Ambient temperature

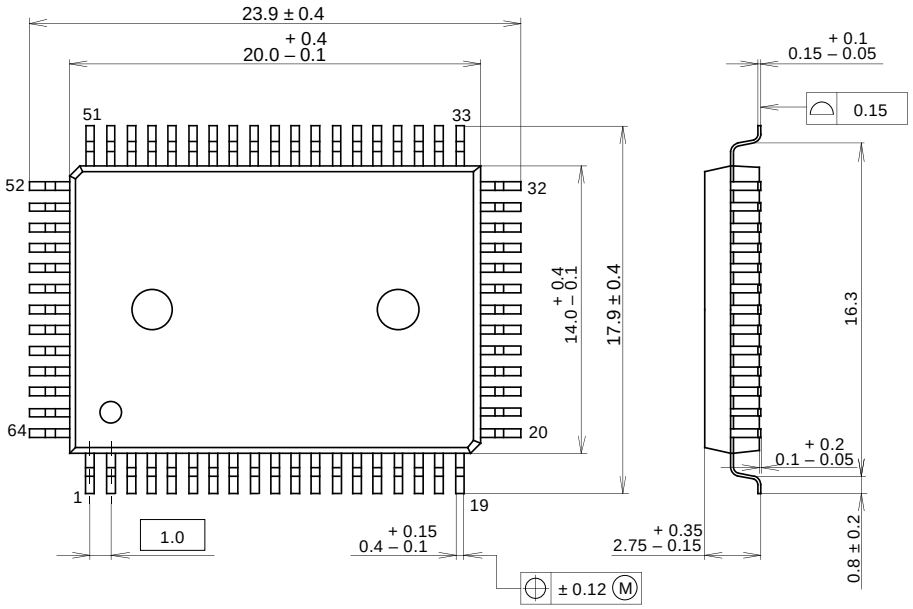


Full-scale voltage vs. Ambient temperature



Package Outline Unit: mm

64PIN QFP(PLASTIC)



SONY CODE	QFP–64P–L01
EIAJ CODE	QFP064–P–1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g