SONY

CXD2450R

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD2450R is a timing generator IC which generates the timing pulses for performing progressive scan readout for digital still camera and personal computer image input applications using the ICX098AK CCD image sensor.

This chip has a built-in vertical driver.

Features

- Base oscillation frequency 36.81MHz (2340f_H)
- Monitoring readout allowed
- High-speed/low-speed electronic shutter function
- Horizontal driver for CCD image sensor
- Vertical driver for CCD image sensor
- Signal processor IC system clock generation 1170f_H, 780f_H
- Vertical/horizontal sync (SSG) timing generation

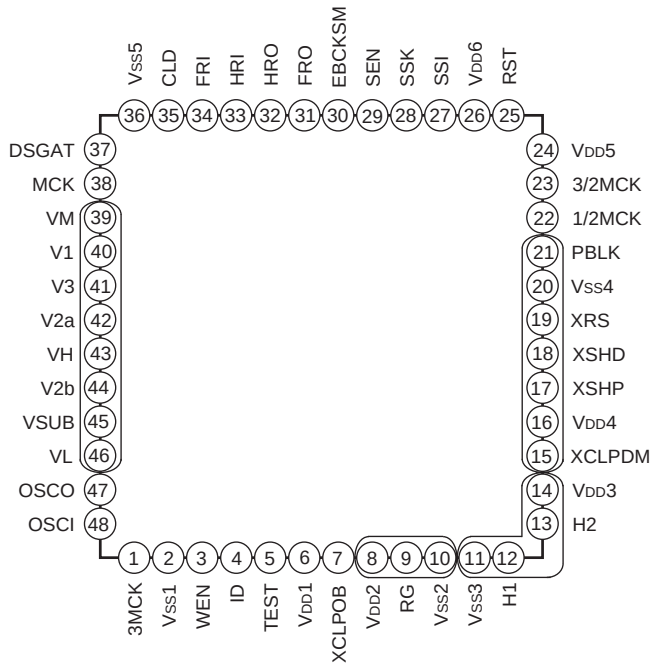
Applications

- Digital still cameras
- Personal computer image input

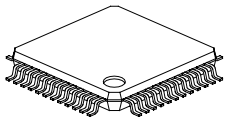
Structure

Silicon gate CMOS IC

Pin Configuration



48 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
	V_M	V_L – 0.5 to +26.0	V
	V_H	V_L – 0.5 to +26.0	V
	V_L	V_L – 0.5 to +26.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage			
	V_{DD}a, V_{DD}b, V_{DD}c, V_{DD}d	3.0 to 3.6	V
	V_M	0.0	V
	V_H	14.5 to 15.5	V
	V_L	–5.0 to –6.0	V
• Operating temperature			
	Topr	–20 to +75	°C

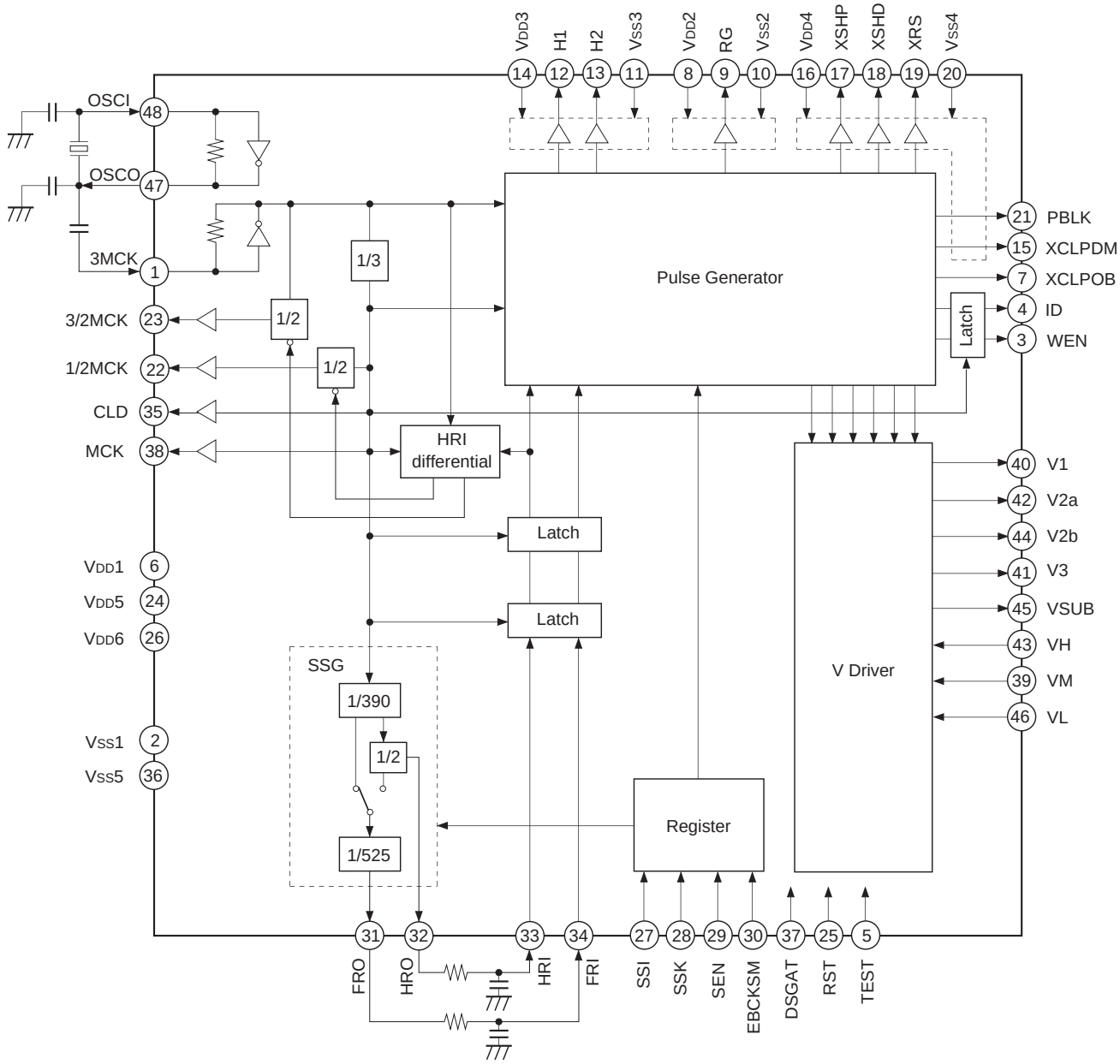
Applicable CCD Image Sensors

ICX098AK (1/4" CCD)

* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

E97819-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	3MCK	I	Internal main clock. (2340f_H)
2	Vss1	—	GND
3	WEN	O	Memory write timing. Stop control possible using the serial interface data.
4	ID	O	Vertical direction line identification pulse output. Stop control possible using the serial interface data.
5	TEST	I	IC test pin; normally fixed to GND. (With pull-down resistor)
6	V_{DD}1	—	3.3V power supply. (Power supply for common logic block)
7	XCLPOB	O	CCD optical black signal clamp pulse output. Stop control possible using the serial interface data.
8	V_{DD}2	—	3.3V power supply. (Power supply for RG)
9	RG	O	CCD reset gate pulse output. (780f_H)
10	Vss2	—	GND
11	Vss3	—	GND
12	H1	O	CCD horizontal register clock output. (780f_H)
13	H2	O	CCD horizontal register clock output. (780f_H)
14	V_{DD}3	—	3.3V power supply. (Power supply for H1/H2)
15	XCLPDM	O	CCD dummy signal clamp pulse output.
16	V_{DD}4	—	3.3V power supply. (Power supply for CDS system)
17	XSHP	O	CCD precharge level sample-and-hold pulse output. (780f_H)
18	XSHD	O	CCD data level sample-and-hold pulse output. (780f_H)
19	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment. (780f_H)
20	Vss4	—	GND
21	PBLK	O	Pulse output for horizontal and vertical blanking interval pulse cleaning.
22	1/2MCK	O	Horizontal direction pixel identification pulse output. Stop control possible using the serial interface data.
23	3/2MCK	O	System clock output for signal processing IC. (1170f_H) Stop control possible using the serial interface data.
24	V_{DD}5	—	3.3V power supply. (Power supply for common logic block)
25	RST	I	Internal system reset input. High: Normal status, Low: Reset status Always input one reset pulse after power-on.
26	V_{DD}6	—	3.3V power supply. (Power supply for common logic block)
27	SSI	I	Serial interface data input for internal mode settings.
28	SSK	I	Serial interface clock input for internal mode settings.
29	SEN	I	Serial interface strobe input for internal mode settings.
30	EBCKSM	I	CHKSUM enable. (With pull-down resistor) High: Sum check invalid, Low: Sum check valid

Pin No.	Symbol	I/O	Description
31	FRO	O	Vertical sync signal output. Stop control possible using the serial interface data.
32	HRO	O	Horizontal sync signal output. Stop control possible using the serial interface data.
33	HRI	I	Horizontal sync signal input.
34	FRI	I	Vertical sync signal input.
35	CLD	O	Clock output for analog/digital conversion IC. (780f_H) Phase adjustment in 60° units possible using the serial interface data.
36	$V_{SS}5$	—	GND
37	DSGAT	I	Control input used to stop drive pulse generation for CCD image sensor, sample-and-hold IC and analog/digital conversion IC. High:Normal status,Low:Stop status Controlled pulse can be changed using the serial interface data.
38	MCK	O	System clock output for signal processor IC. (780f_H)
39	VM	—	GND (GND for vertical driver)
40	V1	O	CCD vertical register clock output. (Binary output)
41	V3	O	CCD vertical register clock output. (Binary output)
42	V2a	O	CCD vertical register clock output. (Ternary output)
43	VH	—	15.0V system power supply. (Power supply for vertical driver)
44	V2b	O	CCD vertical register clock output. (Ternary output)
45	VSUB	O	CCD electronic shutter pulse output.
46	VL	—	–5.5V system power supply. (Power supply for vertical driver)
47	OSCO	O	Inverter output for oscillation.
48	OSCI	I	Inverter input for oscillation.

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{DD}2$	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	$V_{DD}3$	$V_{DD}b$		3.0	3.3	3.6	V
Supply voltage 3	$V_{DD}4$	$V_{DD}c$		3.0	3.3	3.6	V
Supply voltage 4	$V_{DD}1$, $V_{DD}5$, $V_{DD}6$	$V_{DD}d$		3.0	3.3	3.6	V
Supply voltage 5	VH	VH		14.5	15.0	15.5	V
Supply voltage 6	VM	VM		—	0.0	—	V
Supply voltage 7	VL	VL		–6.0	–5.5	–5.0	V
Input voltage 1*1	RST, DSGAT, SSI, SSK, SEN, FRI, HRI	V_{IH1}		0.8V_{DD}d			V
		V_{IL1}				0.2V_{DD}d	V
Input voltage 2 *1, *2	EBCKSM	V_{IH2}		0.8V_{DD}d			V
		V_{IL2}				0.2V_{DD}d	V
Input voltage 3*2	TEST	V_{IH3}		0.7V_{DD}d			V
		V_{IL3}				0.3V_{DD}d	V
Output voltage 1	RG	V_{OH1}	Feed current where I_{OH} = –3.3mA	V_{DD}a – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 2	H1, H2	V_{OH2}	Feed current where I_{OH} = –10.4mA	V_{DD}b – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 7.2mA			0.4	V
Output voltage 3	XSHP, XSHD, XRS, PBLK, XCLPDM	V_{OH3}	Feed current where I_{OH} = –3.3mA	V_{DD}c – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	3/2MCK, MCK, CLD	V_{OH4}	Feed current where I_{OH} = –10.4mA	V_{DD}d – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 7.2mA			0.4	V
Output voltage 5	1/2MCK	V_{OH5}	Feed current where I_{OH} = –3.3mA	V_{DD}d – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 6	XCLPOB, ID, WEN	V_{OH6}	Feed current where I_{OH} = –2.4mA	V_{DD}d – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 7	FRO, HRO	V_{OH7}	Feed current where I_{OH} = –3.6mA	V_{DD}d – 0.8			V
		V_{OL7}	Pull-in current where I_{OL} = 7.2mA			0.4	V
Output voltage 8	VSUB	V_{OH8}	Feed current where I_{OH} = –4.0mA	VH – 0.25			V
		V_{OL8}	Pull-in current where I_{OL} = 5.4mA			VL + 0.25	V
Output voltage 9	V1, V3	V_{OM9}	Feed current where I_{OM} = –5.0mA	VM – 0.25			V
		V_{OL9}	Pull-in current where I_{OL} = 10.0mA			VL + 0.25	V
Output voltage 10	V2a, V2b	V_{OH10}	Feed current where I_{OH} = –7.2mA	VH – 0.25			V
		V_{OM101}	Pull-in current where I_{OM} = 5.0mA			VM + 0.25	V
		V_{OM102}	Feed current where I_{OM} = –5.0mA	VM – 0.25			V
		V_{OL10}	Pull-in current where I_{OL} = 10.0mA			VL + 0.25	V

*1 These input pins do not have protective diodes on the internal power supply side.
*2 These input pins have internal pull-down resistors.
*3 The above table indicates the condition for 3.3V drive of low voltage drive blocks.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DD}d/2$		V
Input voltage	OSCI	V_{IH}		0.7$V_{DD}d$			V
		V_{IL}				0.3$V_{DD}d$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –6.0mA	$V_{DD}d/2$			V
		V_{OL}	Pull-in current where I_{OL} = 6.0mA			$V_{DD}d/2$	V
Feedback resistor	OSCI, OSCO	RFB	V_{IN} = $V_{DD}d$ or Vss	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	3MCK	LVth			$V_{DD}d/2$		V
Input voltage		V_{IH}		0.7$V_{DD}d$			V
		V_{IL}				0.3$V_{DD}d$	V
Input amplification		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

*1 Input voltage is the input voltage characteristics for direct input from an external source. Input amplification is the input amplification characteristics in the case of input through capacitor.

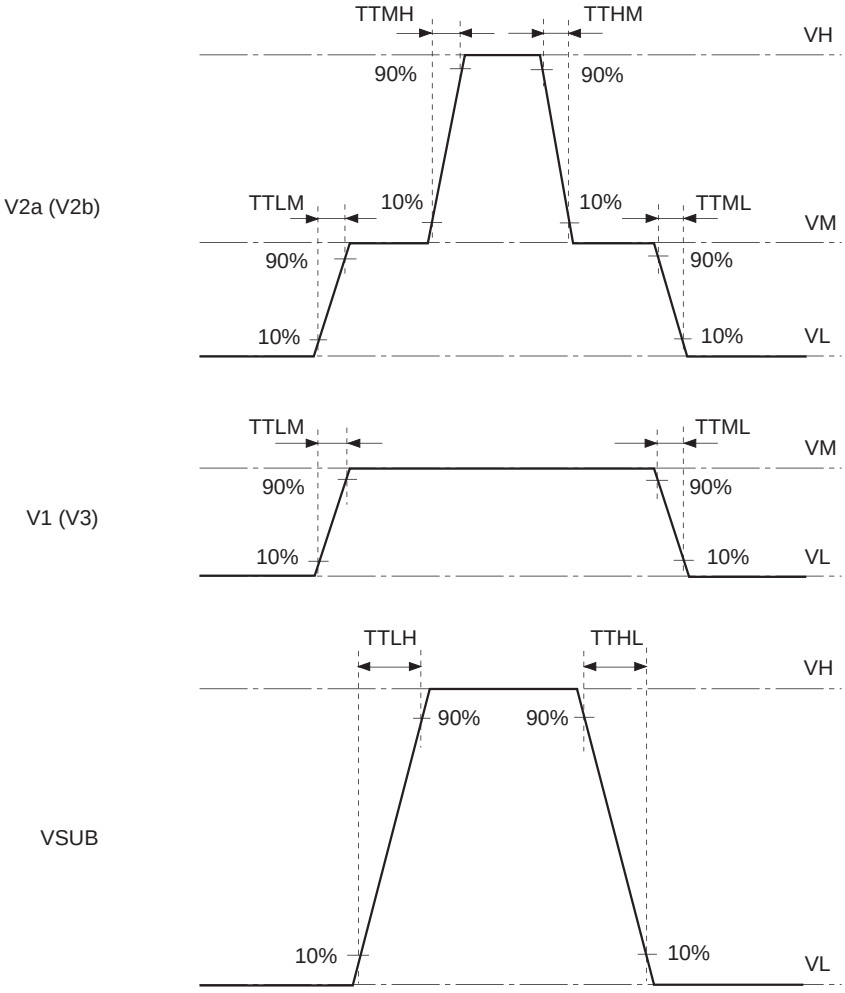
Switching Characteristics (VH = 15.0V, VM = GND, VL = –5.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	—	150	300	ns
	TTMH	VM to VH	—	150	300	ns
	TTLH	VL to VH	—	50	100	ns
Fall time	TTML	VM to VL	—	100	200	ns
	TTHM	VH to VM	—	150	300	ns
	TTHL	VH to VL	—	50	100	ns
Output noise voltage	VCLH		—	—	1.0	V
	VCLL		—	—	1.0	V
	VCMH		—	—	1.0	V
	VCML		—	—	1.0	V

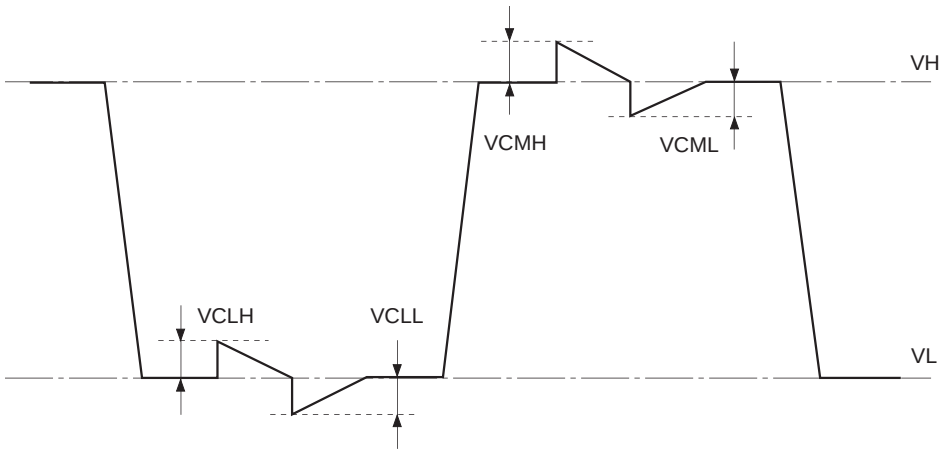
*1 The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.

*2 For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.

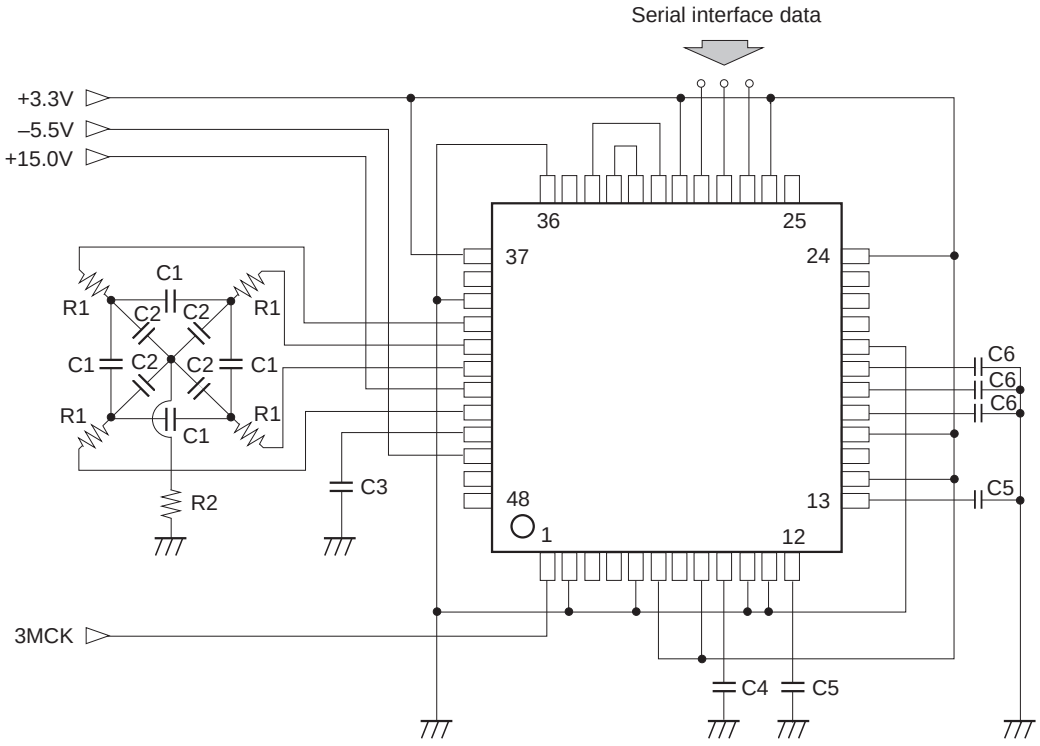
Switching Waveforms



Waveform Noise



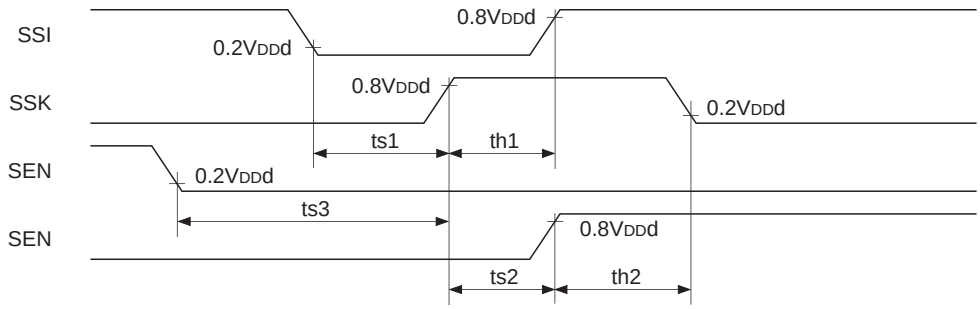
Measurement Circuit



R1: 68W
R2: 15W
C1: 450pF
C2: 2200pF
C3: 500pF
C4: 30pF
C5: 100pF
C6: 10pF

AC Characteristics

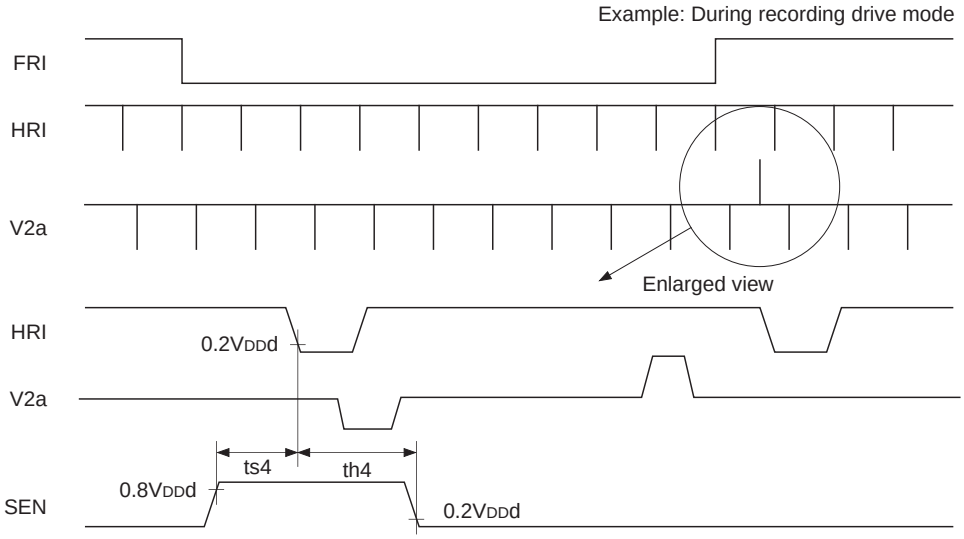
1) AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SSK	20			ns
th1	SSI hold time, activated by the rising edge of SSK	20			ns
ts2	SSK setup time, activated by the rising edge of SEN	20			ns
th2	SSK hold time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SSK	20			ns

2) Serial interface clock internal loading characteristics



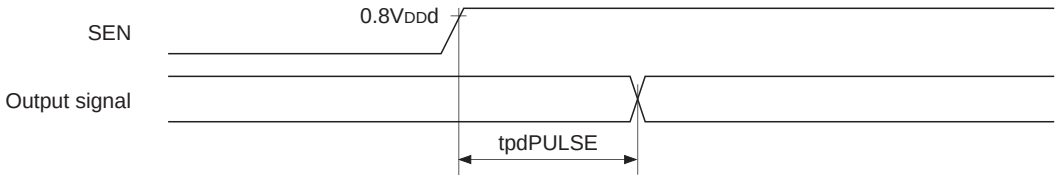
Note) Be sure to maintain a constantly high SEN logic level near the falling edge of HRI immediately before the readout period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts4	SEN setup time, activated by the falling edge of HRI	0			ns
th4	SEN hold time, activated by the falling edge of HRI	0			ns

3) Serial interface clock output variation characteristics

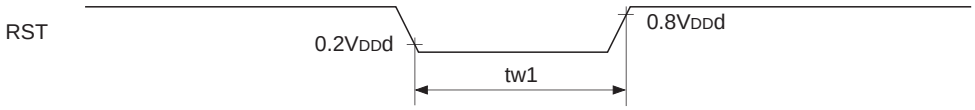
Normally, the serial interface data is loaded to the CXD2450R at the timing shown in 2) above. However, one exception to this is when the data such as SSGSEL and STB is loaded to the CXD2450R and controlled at the rising edge of SEN. For STB, see control data D62 to D63 STB in "Description of Operation".



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		100	ns

4) RST loading characteristics

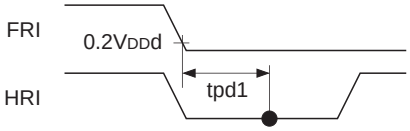


(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

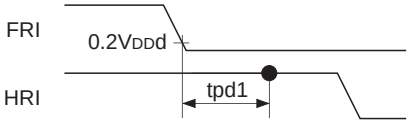
5) Phase discrimination characteristics using FRI and HRI input

When the HRI logic level is low tpd1 after the falling edge of FRI



The field is discriminated as an ODD field .

When the HRI logic level is high tpd1 after the falling edge of FRI

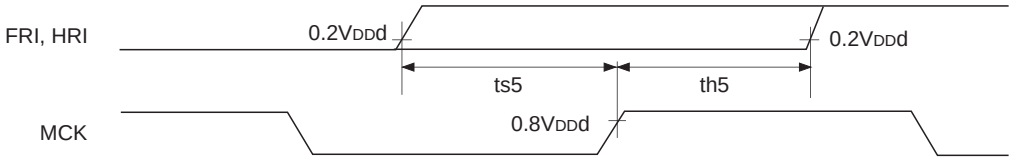


The field is discriminated as an EVEN field .

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Field discrimination clock phase, activated by the falling edge of FRI	1100		1300	ns

6) FRI and HRI loading characteristics

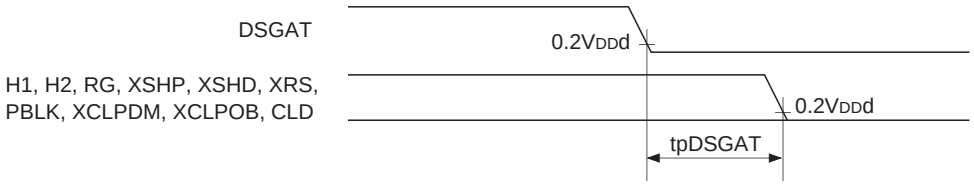


MCK load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Miin.	Typ.	Min.	Unit
ts5	FRI and HRI setup time, activated by the rising edge of MCK	10			ns
th5	FRI and HRI hold time, activated by the rising edge of MCK	0			ns

7) Output timing characteristics using DSGAT

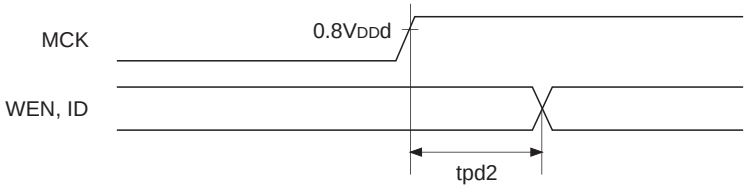


However, V2a, V2b and VSUB are fixed to the voltage level applied to the VH pin, and V1 and V3 are fixed to the voltage level applied to the VM pin.
H1 and H2 load capacitance = 100pF, RG load capacitance = 20pF,
XSHP, XSHD, XRS, PBLK, XCLPDM, XCLPOB and CLD load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Miin.	Typ.	Min.	Unit
tpDSGAT	Time until the above outputs go low after the fall of DSGAT			100	ns

8) Output variation characteristics

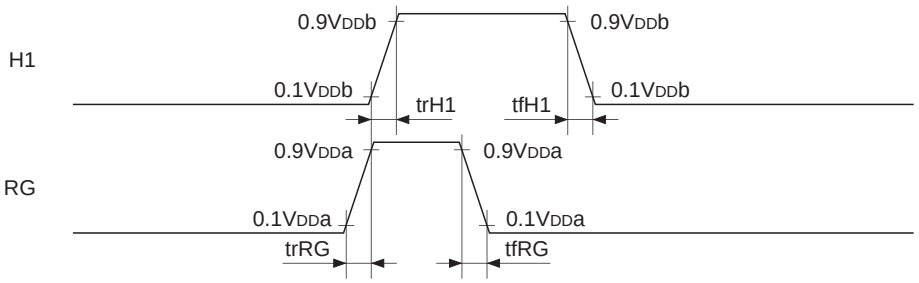


WEN and ID load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Miin.	Typ.	Min.	Unit
tpd2	Time until the above outputs change after the rise of MCK	20		40	ns

9) H1 and RG waveform characteristics



$V_{DD}b$ = 3.3V, Topr = 25°C, H1 and H2 load capacitance = 100pF, RG load capacitance = 20pF
(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
trH1	H1 rise time		10		ns
tfH1	H1 fall time		10		ns
trRG	RG rise time		3		ns
tfRG	RG fall time		3		ns

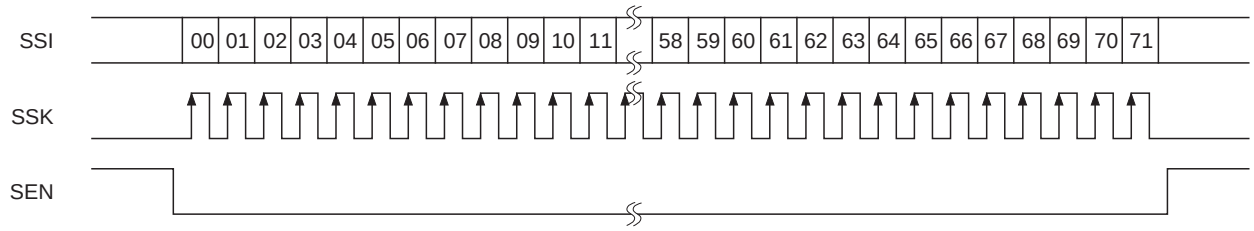
10) I/O pin capacitance

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
C_{IN}	Input pin capacitance			9	pF
C_{OUT}	Output pin capacitance			11	pF
$C_{I/O}$	I/O pin capacitance			11	pF

Description of Operation

Pulses output from the CXD2450R are controlled by the RST and DSGAT pins and by the serial interface data shown below. The details of control by the serial interface data and a description of operation are as follows.



The CXD2450R basically loads and reflects the serial interface data sent in the above format in the readout portion at the falling edge of HRI. Here, readout portion specifies the horizontal interval during which V2a and V2b take the ternary level.

There are two types of serial interface data: drive control data and phase adjustment data. Hereafter, these data are distinguished by referring to the former as control data and the latter as adjustment data.

An example of the initialization data for the CXD2450R control data is shown below. This data is based on the Application Circuit Block Diagram, so care should be taken as there are some differences from the RST pin initialization data. Concretely, the internal SSG operates, the XCLPOB and ID pulses are generated, and the 3/2MCK pulse is stopped. This data shows the values when the EBCKSM pin is low and D64 to D71 CHKSUM is valid.

MSB															LSB
D71	D70	D69	D68	D67	D66	D65	D64	D63	D62	D61	D60	D59	D58	D57	D56
1	0	1	0	1	1	0	1	0	0	0	0	0	0	1	0
MSB															LSB
D55	D54	D53	D52	D51	D50	D49	D48	D47	D46	D45	D44	D43	D42	D41	D40
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MSB															LSB
D39	D38	D37	D36	D35	D34	D33	D32	D31	D30	D29	D28	D27	D26	D25	D24
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB															LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB							LSB								
D07	D06	D05	D04	D03	D02	D01	D00								
1	0	0	0	0	0	0	1								

The adjustment data does not normally need to be set. However, when adjustment is difficult due to the system configuration or for other reasons, the data considered most appropriate at that time should be set as the initialization data.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	When a reset
D00 to D07	CHIP	Chip switching	See D00 to D07 CHIP.		All 0
D08 to D15	CTGRY	Category switching	See D08 to D15 CTGRY.		All 0
D16 to D17	SMD	Electronic shutter mode setting	See D16 to D35 Electronic shutter mode.		All 0
D18 to D25	Shut.FRM	Electronic shutter vertical interval setting	See D16 to D35 Electronic shutter mode.		All 0
D26 to D35	Shut.HD	Electronic shutter horizontal interval setting	See D16 to D35 Electronic shutter mode.		All 0
D36 to D47	—	—	—	—	All 0
D48	EXPOSE	Recording exposure setting switching	OFF	ON	0
D49 to D50	—	—	—	—	All 0
D51	PSMT	Drive mode switching	Monitoring	Recording	0
D52	SSGSEL	Internal SSG operation switching	OFF	ON	0
D53	WENSEL	WEN pulse operation switching	ON	OFF	0
D54	CLPSEL	XCLPOB pulse operation switching	OFF	ON	0
D55	IDSEL	ID pulse operation switching	OFF	ON	0
D56	HMCKSEL	1/2MCK pulse operation switching	OFF	ON	0
D57	TMCKSEL	3/2MCK pulse operation switching	ON	OFF	0
D58	HMCKREV	1/2MCK pulse reset polarity switching	Positive polarity	Negative polarity	0
D59	TMCKREV	3/2MCK pulse reset polarity switching	Negative polarity	Positive polarity	0
D60 to D61	DSG	Pulse generation control	See D60 to D61 DSG table.		All 0
D62 to D63	STB	IC pin status control	See D62 to D63 STB table.		All 0
D64 to D71	CHKSUM	Check sum bit	See D64 to D71 CHKSUM.		All 0

Detailed Description of Each Data

D00 to D07 CHIP

The serial interface data is loaded to the CXD2450R when D00 and D07 are 1. However, this assumes that either the EBCKSM pin is low and D64 to D71 CHKSUM is satisfied or the EBCKSM pin is high.

MSB							LSB	Function
D07	D06	D05	D04	D03	D02	D01	D00	
1	0	0	0	0	0	0	1	Loading to the CXD2450R

Note that when SEN is shared with other ICs and identification is performed using CHIP-ID, the CXD2450R data must be positioned immediately before the load timing, that is to say at the very end.

D08 to D15 CTGRY

Of the data provided to the CXD2450R by the serial interface, the CXD2450R loads D16 and subsequent data to the control data register side when D08 is 0, and to the adjustment data register side when D08 is 1. However, this assumes that the CXD2450R is selected by CHIP and that either the EBCKSM pin is low and D64 to D71 CHKSUM is satisfied or the EBCKSM pin is high.

MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D09	D08	
0	0	0	0	0	0	0	0	Loading to the control data register side
0	0	0	0	0	0	0	1	Loading to the adjustment data register side

Note that the CXD2450R cannot apply both categories simultaneously during the same vertical interval. Also, care should be taken as the data is overwritten even if the same category is applied.

D16 to D35 Electronic shutter mode

The CXD2450R's electronic shutter mode can be switched as follows by SMD D16 to D17. Handling of the data from D18 to D35 differs according to the mode, and is explained in detail below.

D17	D16	Description of operation
X	0	VSUB stopped mode
0	1	High-speed/low-speed shutter mode
1	1	HTSG control mode

The electronic shutter data is expressed as shown in the table below using Shut.HD as an example.

MSB									LSB
D35	D34	D33	D32	D31	D30	D29	D28	D27	D26
0	1	1	1	0	0	0	0	1	1
↓			↓				↓		
1			C				3		

→ Shut.HD is expressed as 1C3h.

[VSUB stopped mode]

During this mode, the data from D18 to D35 is invalid. The shutter speed is 1/60 s during monitoring drive mode, and 1/30 s during recording drive mode.

[High-speed/low-speed shutter mode]

During this mode, the data has the following meanings.

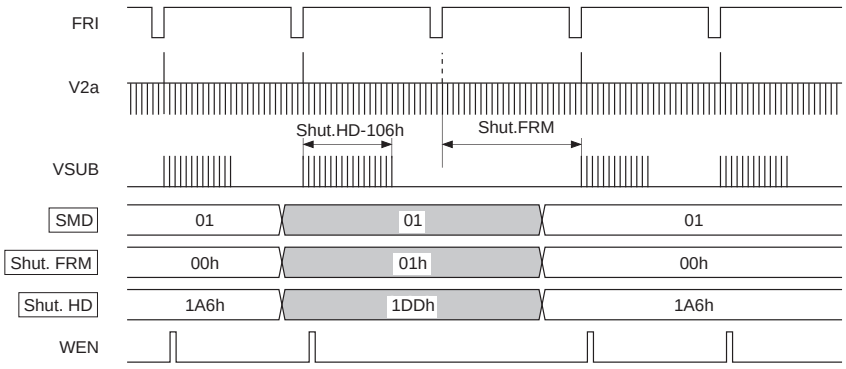
Symbol	Data	Description
Shut.FRM	D18 to D25	Shutter speed data (number of vertical intervals) specification
Shut.HD	D26 to D35	Shutter speed data (number of horizontal intervals) specification

The CXD2450R does not distinguish between the high-speed shutter and low-speed shutter modes. The interval during which Shut.FRM and Shut.HD are specified together is the shutter speed. At this time, Shut.FRM controls the ternary level output at V2a and V2b, and Shut.HD controls the VSUB output. Concretely, when specifying high-speed shutter, Shut.FRM is set to 00h. (See the figure.) During low-speed shutter, or in other words when Shut.FRM is set to 01h or higher, the serial interface data is not loaded until this interval is finished.
However, care should be taken as the vertical interval indicated here is set in 1/60s units when the drive mode is monitoring drive mode and 1/30s units during recording mode. For monitoring drive mode, care should be taken as the Shut.HD value has an offset. This is so that the CXD2450R can obtain basically the same exposure time for the same Shut.HD value during high-speed shutter independent of the drive mode.

Formula for calculating the electronic shutter speed: [Shut.FRM/Shut.HD] (unit: µs)

Monitoring drive mode:

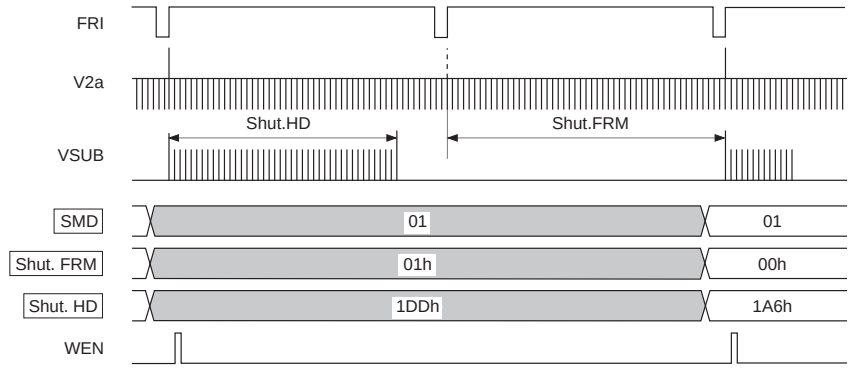
$T = Shut.FRM * 1.66834 * 10^4 + \{(20Ch - Shut.HD) * 780 + 447\} * 81.5 * 10^{-3}$ (000h ≤ Shut.HD ≤ 20Ch)



During monitoring drive mode/low-speed shutter mode

Recording drive mode:

$T = Shut.FRM * 3.33667 * 10^4 + \{(20Ch - Shut.HD) * 780 + 447\} * 81.5 * 10^{-3}$ (000h ≤ Shut.HD ≤ 20Ch)



During recording drive mode/low-speed shutter mode

Electronic shutter speed table [Shut.FRM/Shut.HD]

Shut.FRM	Shut.HD	Shutter speed (s)	Calculation results (s)	Shut.FRM	Shut.HD	Shutter speed (s)	Calculation results (s)
00h	20Ch	1/27000	1/27450	00h	107h*1	1/60	1/60
00h	20Bh	1/10000	1/10000	01h	20Ch	1/60*2	1/60
00h	209h	1/4500	1/4403	01h	1D8h	1/50*2	1/50
00h	205h	1/2000	1/2077	02h	20Ch	1/30*2	1/30
00h	1FDh	1/1000	1/1010	07h	18Bh	1/8*2	1/8
00h	1EDh	1/500	1/498	09h	109h	1/6*2	1/6
00h	1CEh	1/250	1/251	00h	0D2h	1/50*3	1/50
00h	18Fh	1/125	1/125	00h	083h	1/40*3	1/40
00h	16Fh	1/100	1/100	00h	000h	1/30*3	1/30

*1 One VSUB pulse is generated for odd fields and two for even fields.

*2 These are the settings during monitoring drive mode.

*3 These are the settings during recording drive mode.

Note) Input prohibited data:

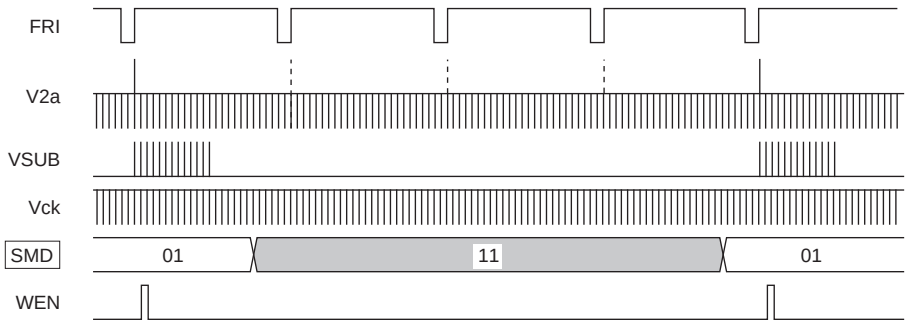
Monitoring drive mode 000h to 106h

Recording drive mode and monitoring drive mode 20Dh to 3FFh

[HTSG control mode]

During this mode, the data from D18 to D35 is invalid.

The ternary level outputs at V2a and V2b are controlled, and the shutter speed is the value obtained by adding the shutter speed specified in the preceding vertical interval to the vertical period during which V2a and V2b are stopped as shown in the figure.



During HTSG control mode

D48 EXPOSE

0: No operation

1: VSUB for recording exposure is generated.

This control specification is such that one VSUB pulse is always generated during the horizontal interval immediately following the readout portion even if the electronic shutter speed is set to 1/60s (SMD = 00). This mode is closely related to D51 PSMT, so see D51 regarding the control.

D51 PSMT

0: Driving is controlled in accordance with monitoring drive mode under the assumption that the vertical/horizontal sync signals are input.

1: Driving is controlled in accordance with recording drive mode under the assumption that the vertical/horizontal sync signals are input.

See the timing charts for the vertical/horizontal sync signals in accordance with each mode.
Note that when switching from monitoring drive to recording drive mode, the pixels decimated thus far must be cleaned.
Concretely, this operation is supported by generating VSUB, but the CXD2450R facilitates this control by using D48 EXPOSE. (See the figure.)

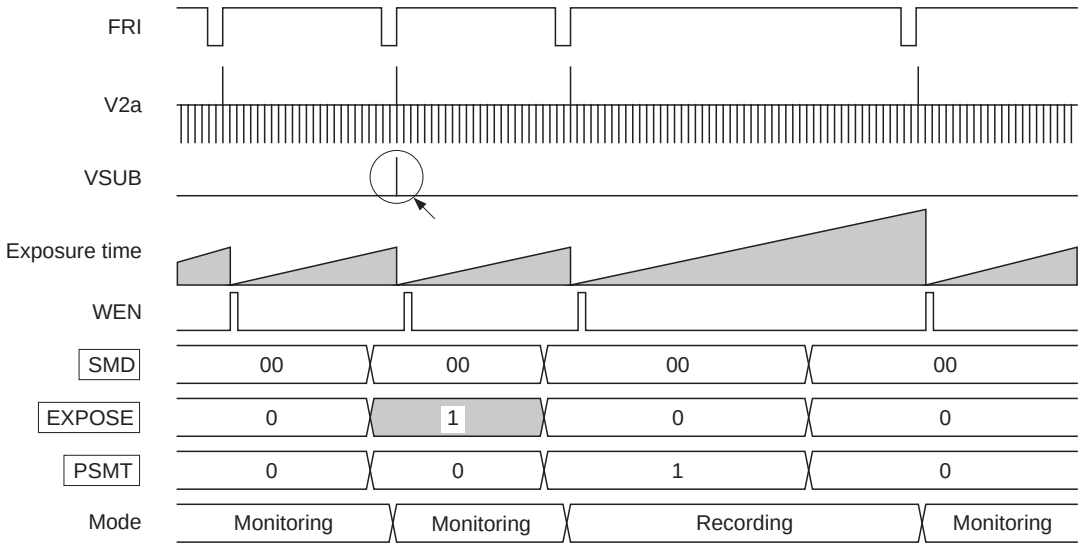


Image of switching from monitoring drive mode to recording drive mode

D52 SSGSEL

0: Internal SSG functions are stopped.

1: Internal SSG functions operate, and FRO and HRO are generated.

When generation is stopped, these pulses are fixed low.

D53 WENSEL

0: WEN is generated.

1: WEN generation is stopped.

When generation is stopped, operation is the same as for D52 SSGSEL.

D54 CLPSEL
0: XCPOB generation is stopped.
1: XCPOB is generated.

When generation is stopped, operation is the same as for D52 SSGSEL.

D55 IDSEL
0: ID generation is stopped.
1: ID is generated.

When generation is stopped, operation is the same as for D52 SSGSEL.

D56 HMCKSEL
0: 1/2MCK generation is stopped.
1: 1/2MCK is generated.

When generation is stopped, operation is the same as for D52 SSGSEL.

D57 TMCKSEL
0: 3/2MCK is generated.
1: 3/2MCK generation is stopped.

When generation is stopped, operation is the same as for D52 SSGSEL.

D58 HMCKREV
0: 1/2MCK reset when positive polarity.
1: 1/2MCK reset when negative polarity.

D59 HMCKREV
0: 3/2MCK reset when negative polarity.
1: 3/2MCK reset when positive polarity.

D60 to D61 DSG
The CXD2450R can apply stop control to the CCD pulses and pulses for the sample-and-hold and analog/digital conversion ICs by setting the DSGAT pin low. Conversely, when the DSGAT pin is set high, the controlled pulses can be switched as follows using the serial interface data.

D61	D60	Operating mode
0	0	No control performed
0	1	CCD pulse stop control
1	0	Sample-and-hold and analog/digital conversion IC pulse stop control
1	1	CCD pulse and sample-and-hold and analog/digital conversion IC pulse stop control

Here, CCD pulses refer to the H1, H2, RG, V1, V2a, V2b, V3 and VSUB pulses. Sample-and-hold and analog/digital conversion IC pulses refer to the XSHP, XSHD, XRS, PBLK, XCLPOB, XCLPDM and CLD pulses. See 7) Output timing characteristics using DSGAT of "AC Characteristics" for the stop control status of each pulse.

D62 to D63 STB

This switches the operating mode as shown below. However, the IC pin status control bit is loaded to the CXD2450R and controlled immediately at the rise of the SEN input.

D63	D62	Symbol	Operating mode
X	0	CAMERA	Normal operating mode
0	1	SLEEP	Sleep mode*1
1	1	STNBY	Standby mode

*1 Mode for the status which does not require CCD drive when playing back recorded data within the system.

The pin status during each mode is shown in the table below.

Pin	Symbol	CAMERA	SLEEP	STNBY	Pin	Symbol	CAMERA	SLEEP	STNBY
1	3MCK	ACT	ACT	ACT	25	RST	ACT	ACT	ACT
2	Vss1	—			26	V_{DD}6	—		
3	WEN	ACT	L	L	27	SSI	ACT	ACT	ACT
4	ID	ACT	L	L	28	SSK	ACT	ACT	ACT
5	TEST	—			29	SEN	ACT	ACT	ACT
6	V_{DD}1	—			30	EBCKSM	ACT	ACT	ACT
7	XCLPOB	ACT	L	L	31	FRO	ACT	ACT	L
8	V_{DD}2	—			32	HRO	ACT	ACT	L
9	RG	ACT	L	L	33	HRI	ACT	ACT	ACT
10	Vss2	—			34	FRI	ACT	ACT	ACT
11	Vss3	—			35	CLD	ACT	L	L
12	H1	ACT	L	L	36	Vss5	—		
13	H2	ACT	L	L	37	DSGAT	ACT	ACT	ACT
14	V_{DD}3	—			38	MCK	ACT	ACT	L
15	XCLPDM	ACT	L	L	39	VM	—		
16	V_{DD}4	—			40	V1	ACT	VM	VM
17	XSHP	ACT	L	L	41	V3	ACT	VM	VM
18	XSHD	ACT	L	L	42	V2a	ACT	VH	VH
19	XRS	ACT	L	L	43	VH	—		
20	Vss4	—			44	V2b	ACT	VH	VH
21	PBLK	ACT	L	L	45	VSUB	ACT	VH	VH
22	1/2MCK	ACT	L	L	46	VL	—		
23	3/2MCK	ACT	ACT	L	47	OSCO	ACT	ACT	ACT
24	V_{DD}5	—			48	OSCI	ACT	ACT	ACT

Note) ACT means that the circuit is operating. L indicates a low output level in the controlled status. Also, VH and VM indicate the voltage levels applied to VH (Pin 43) and VM (Pin 39), respectively, in the control status.

D64 to D71 CHKSUM

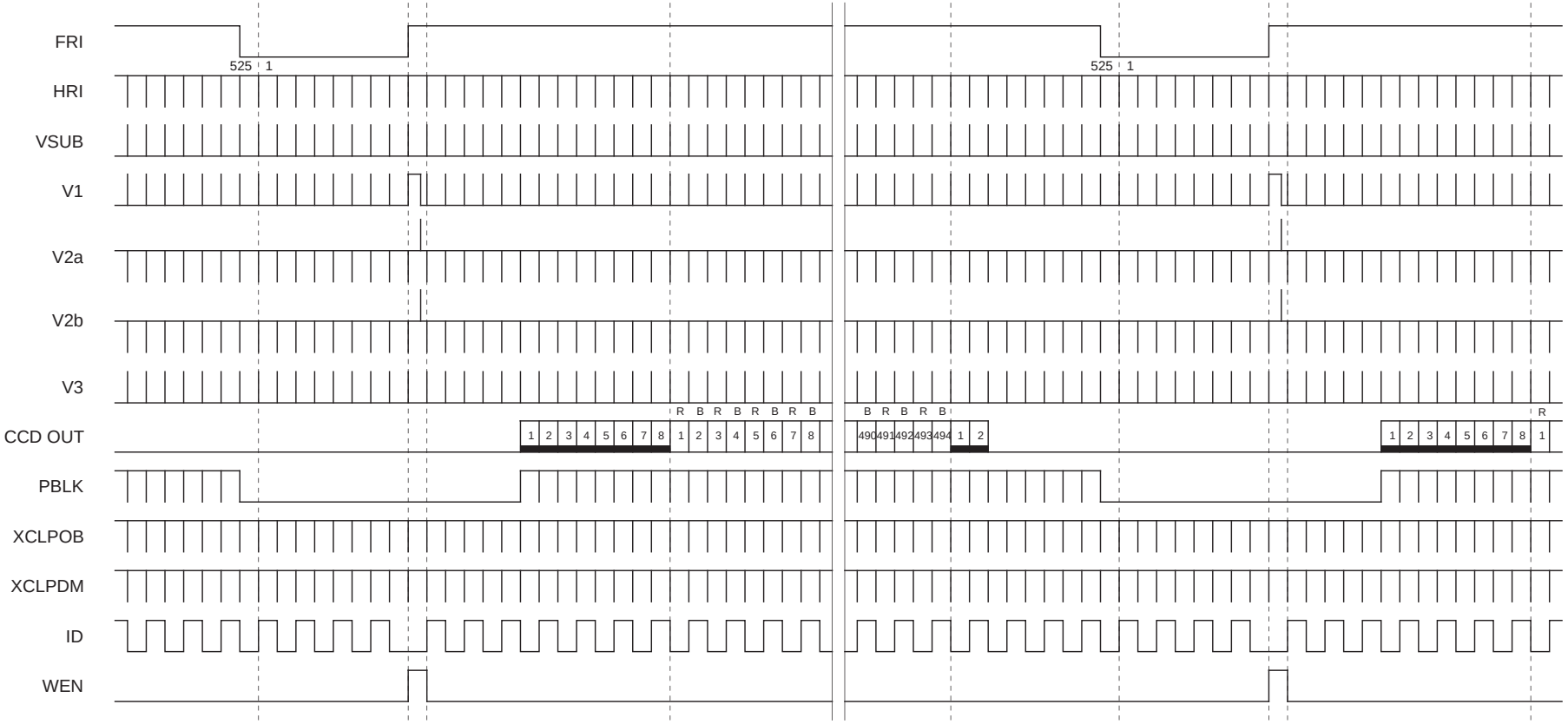
This is the check sum bit. Apply the data shown below.

	MSB							LSB	
	D07	D06	D05	D04	D03	D02	D01	D00	
	D15	D14	D13	D12	D11	D10	D09	D08	
	D23	D22	D21	D20	D19	D18	D17	D16	
	D31	D30	D29	D28	D27	D26	D25	D24	
	D39	D38	D37	D36	D35	D34	D33	D32	
	D47	D46	D45	D44	D43	D42	D41	D40	
	D55	D54	D53	D52	D51	D50	D49	D48	
	D63	D62	D61	D60	D59	D58	D57	D56	
+)	D71	D70	D69	D68	D67	D66	D65	D64	→ CHKSUM
	0	0	0	0	0	0	0	0	→ Reflected when the total is 0.

Chart-1 Vertical Direction Timing Chart

MODE (Base oscillation frequency: 2340f_H)
Recording drive mode

Applicable CCD image sensor:
ICX098AK

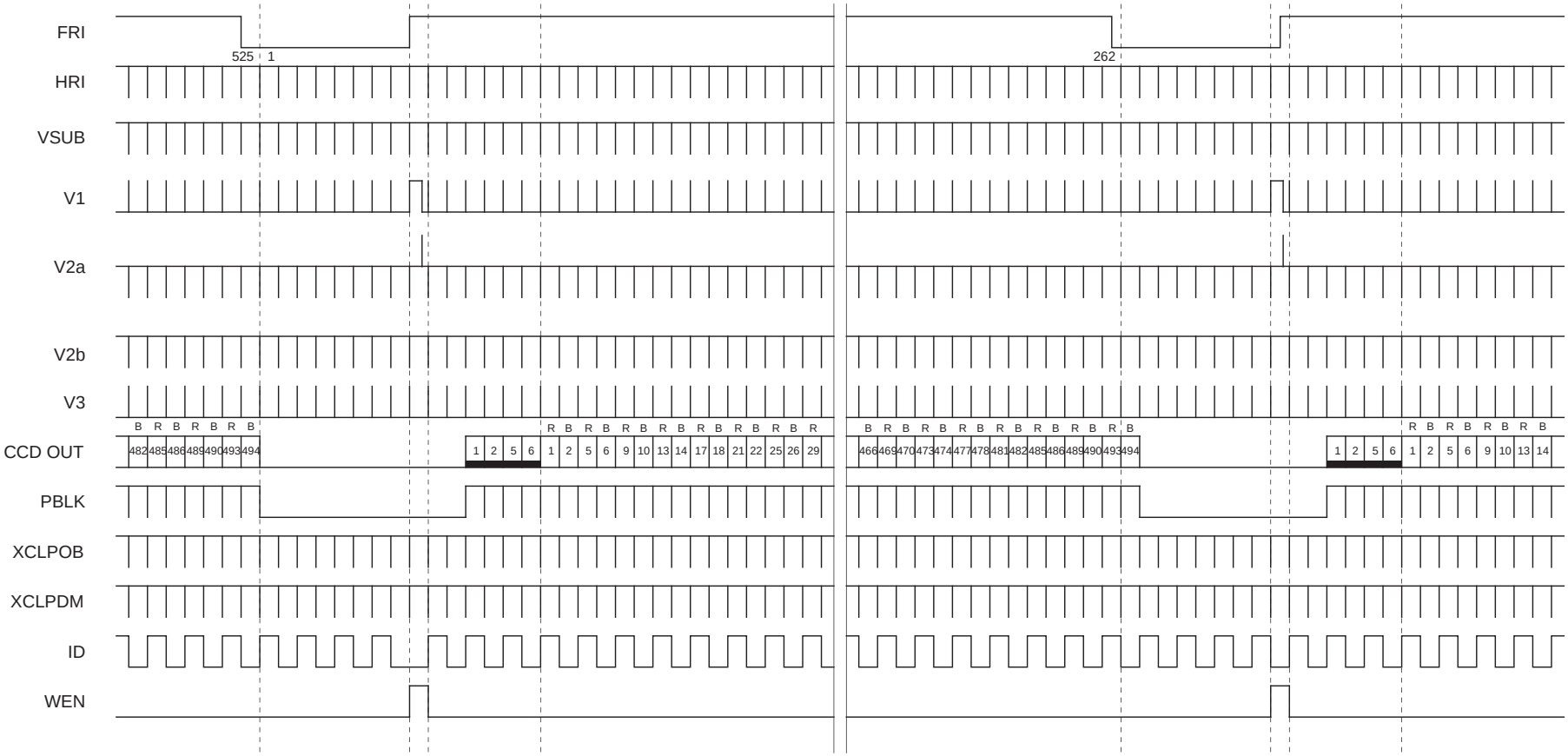


* The number of VSUB pulses is determined by the serial interface data. This chart shows the case where Shut.HD = 20Ch and VSUB pulses are generated over the entire horizontal interval.
* In addition to the phase relationship between FRI and HRI shown above, the phases may also be offset by 1/2 horizontal interval. In any case, the readout interval is the 9th HRI fall counted from the fall of FRI.
* Note that R and B of CCDOUT indicate lines containing these components, and do not mean the lead pixel component of that line.

Chart-2 Vertical Direction Timing Chart

MODE (Base oscillation frequency: 2340f_H)
Monitoring drive mode

Applicable CCD image sensor:
ICX098AK

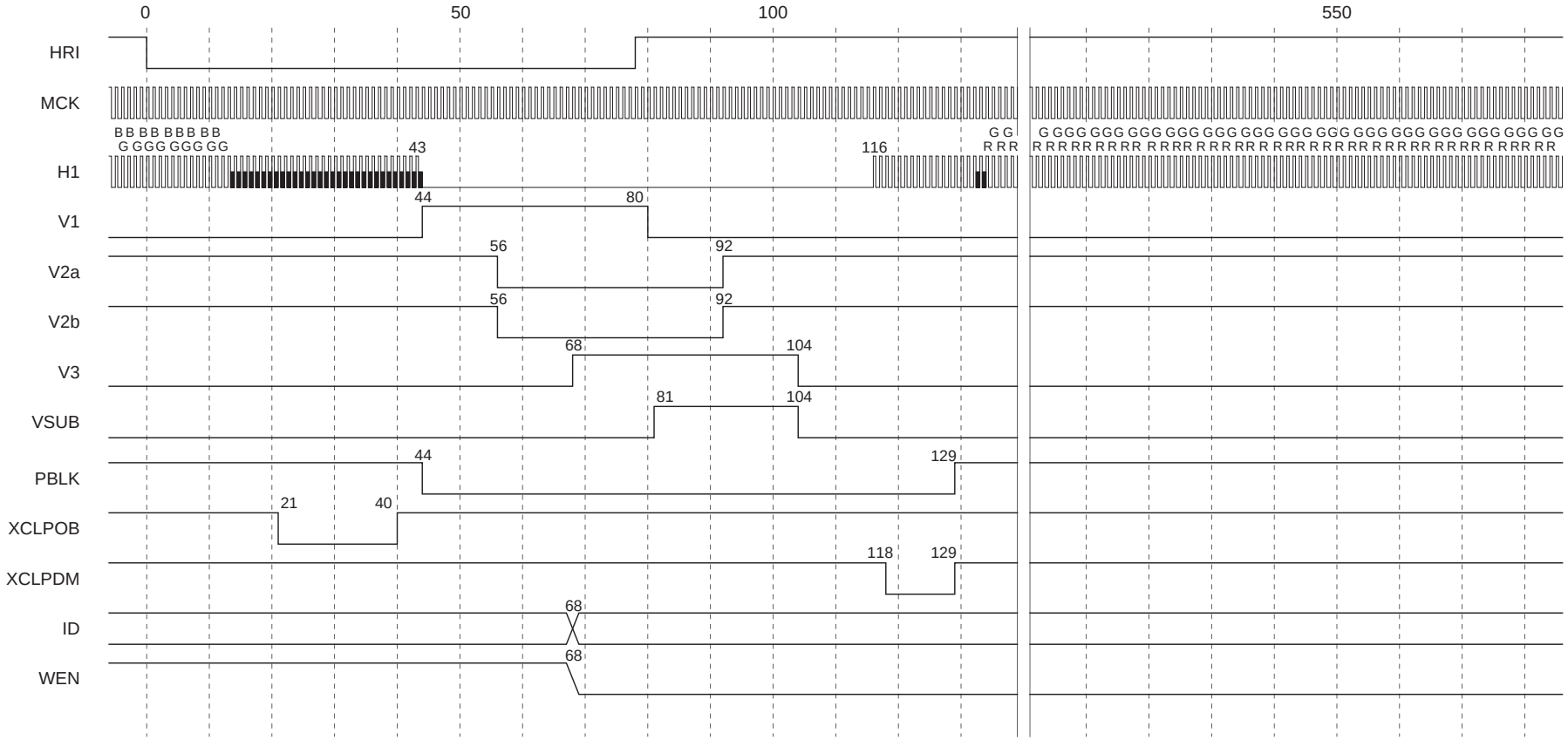


* The number of VSUB pulses is determined by the serial interface data. This chart shows the case where Shut.HD = 20Ch and VSUB pulses are generated over the entire horizontal interval.
* Note that R and B of CCDOUT indicate lines containing these components, and do not mean the lead pixel component of that line.

Chart-3 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340f_H)
Recording drive mode

Applicable CCD image sensor:
ICX098AK

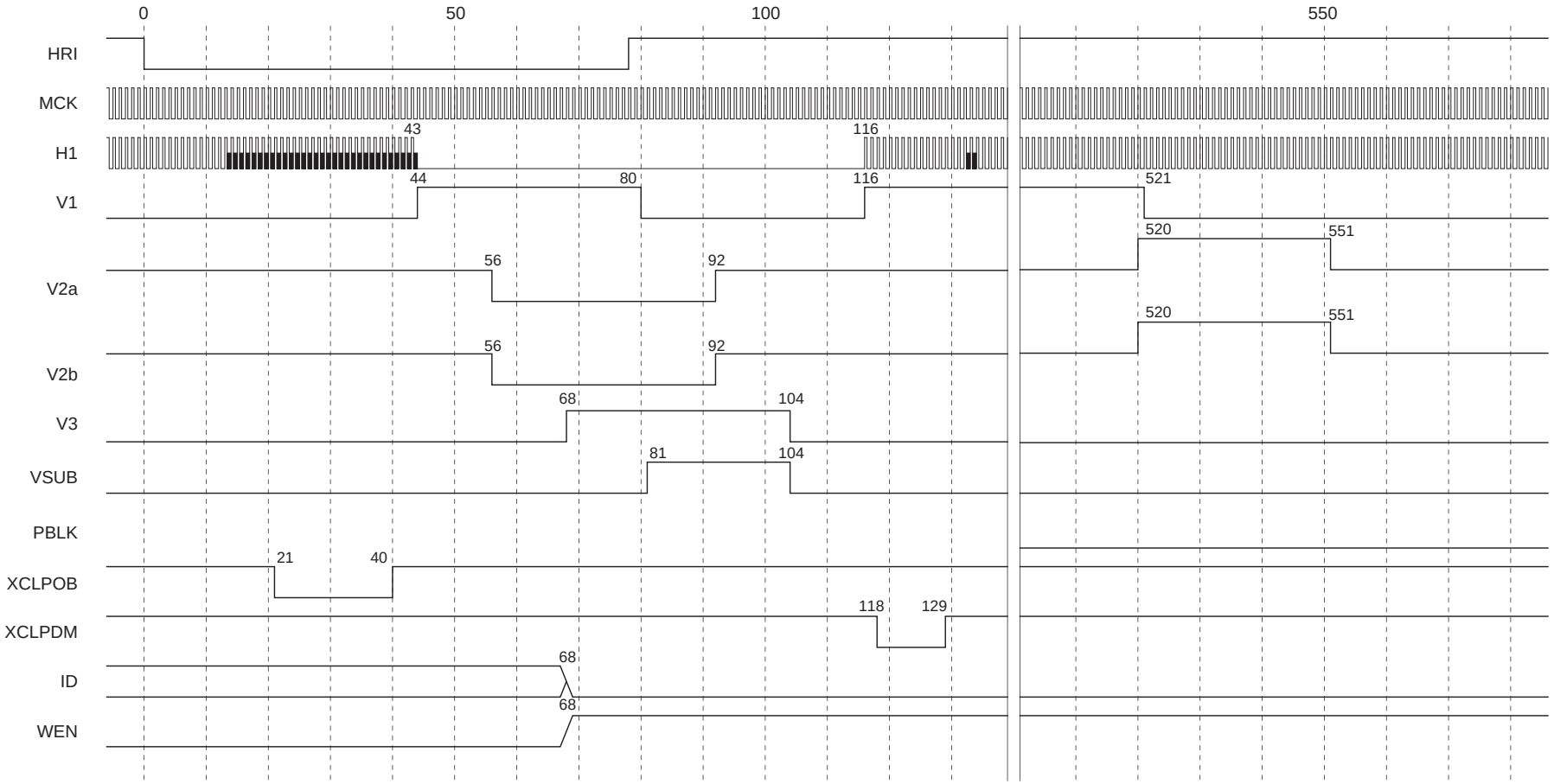


* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates the actual CXD2450R load timing.
* The numbers at the output pulse transition points indicate the count at the MCK (780f_H) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4µs. This chart shows an interval of 78ck (6.3µs).
* VSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the rise of V3.
* WEN is output during the horizontal interval shown in Chart-1. The transition timing is the same as that for ID.
* R, G and B of H1 indicate the output pixel color. In addition to the lines starting from R and G shown above, there are also lines starting from G and B.

Chart-4 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340f_H)
Recording drive mode (readout portion)

Applicable CCD image sensor:
ICX098AK

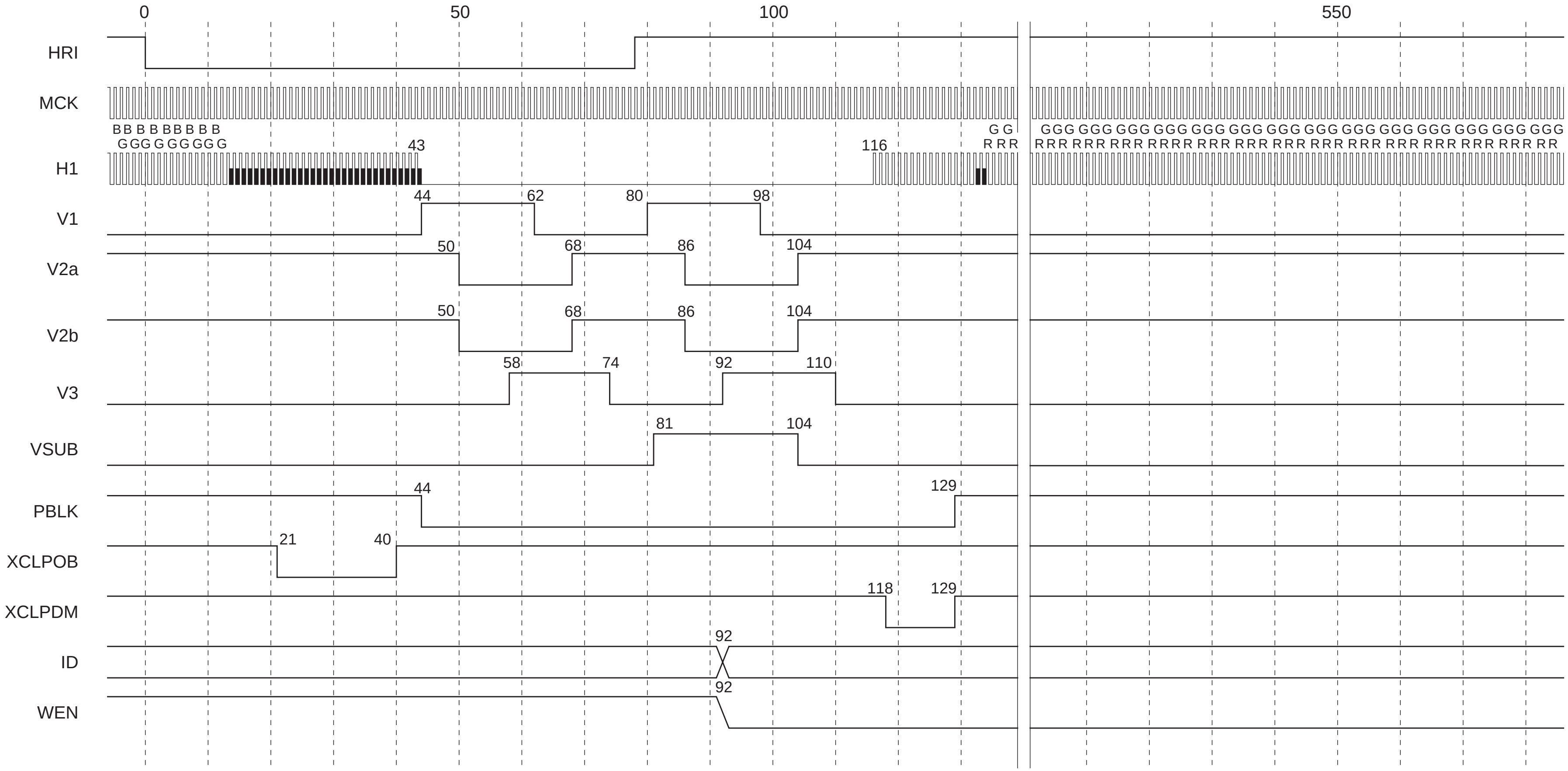


* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates the actual CXD2450R load timing.
* The numbers at the output pulse transition points indicate the count at the MCK (780f_H) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4µs. This chart shows an interval of 78ck (6.3µs).
* VSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the rise of V3. ID is reset low at this timing during the readout horizontal interval.
* WEN is output during the horizontal interval shown in Chart-1. The transition timing is the same as that for ID.

Chart-5 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340fH)
Monitoring drive mode

Applicable CCD image sensor:
ICX098AK

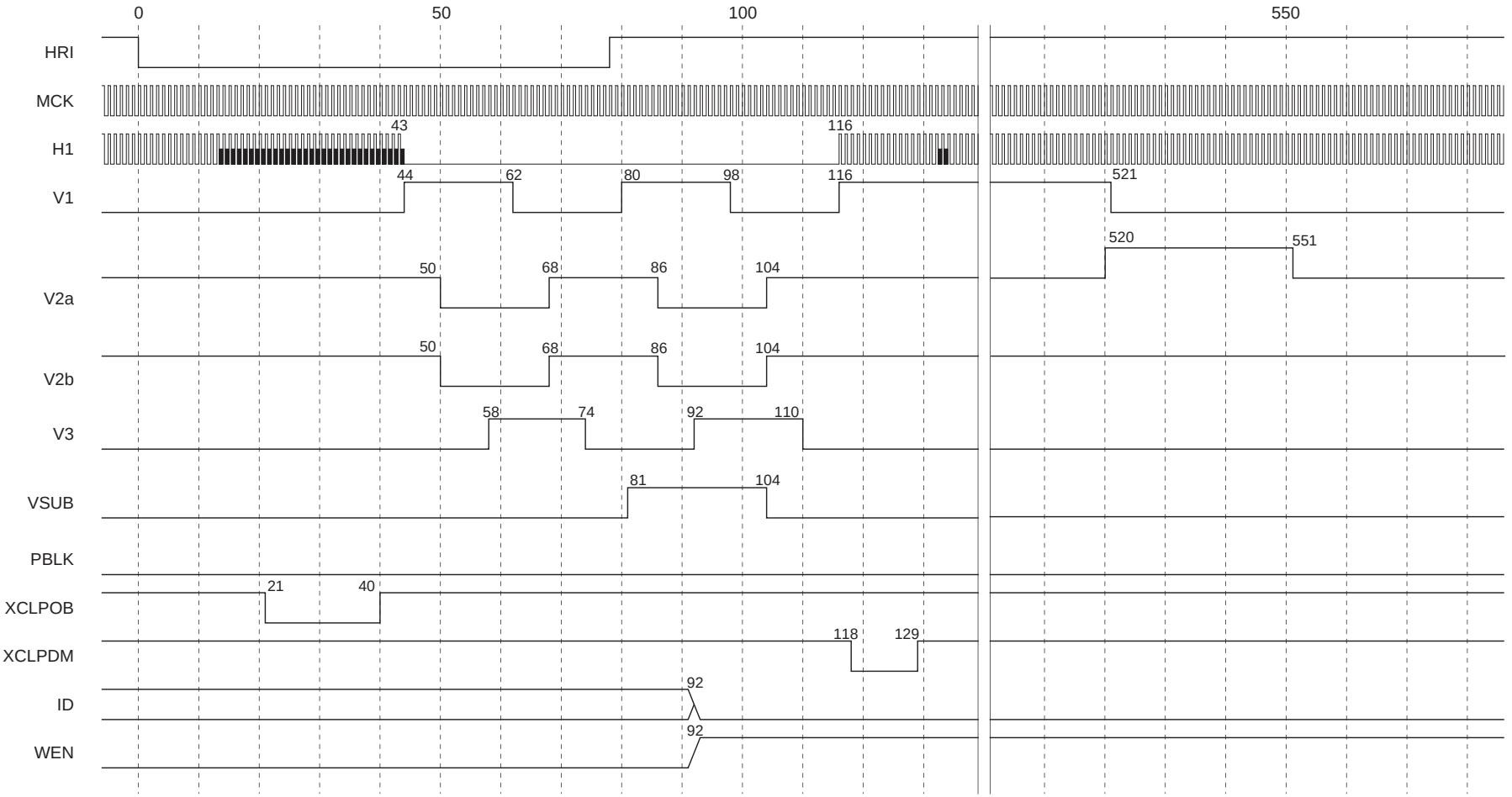


* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates the actual CXD2450R load timing.
* The numbers at the output pulse transition points indicate the count at the MCK (780fH) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4µs. This chart shows an interval of 78ck (6.3µs).
* VSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the rise of V3.
* WEN is output during the horizontal interval shown in Chart-2. The transition timing is the same as that for ID.
* R, G and B of H1 indicate the output pixel color. In addition to the lines starting from R and G shown above, there are also lines starting from G and B.

Chart-6 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340f_H)
Monitoring drive mode (readout portion)

Applicable CCD image sensor:
ICX098AK

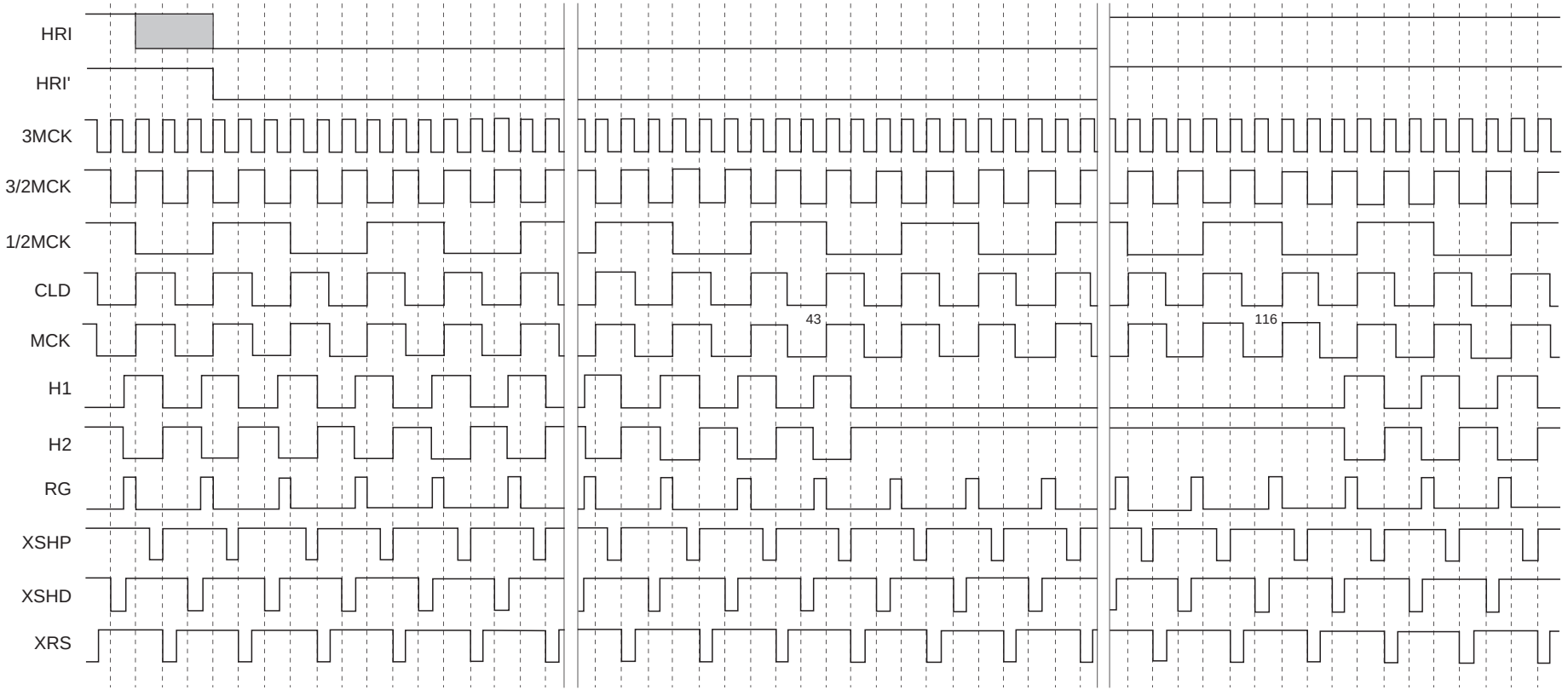


* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates the actual CXD2450R load timing.
* The numbers at the output pulse transition points indicate the count at the MCK (780f_H) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4µs. This chart shows an interval of 78ck (6.3µs).
* VSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the rise of V3. ID is reset low at this timing during the readout horizontal interval.
* WEN is output during the horizontal interval shown in Chart-2. The transition timing is the same as that for ID.

Chart-7 High-speed Phase Timing Chart

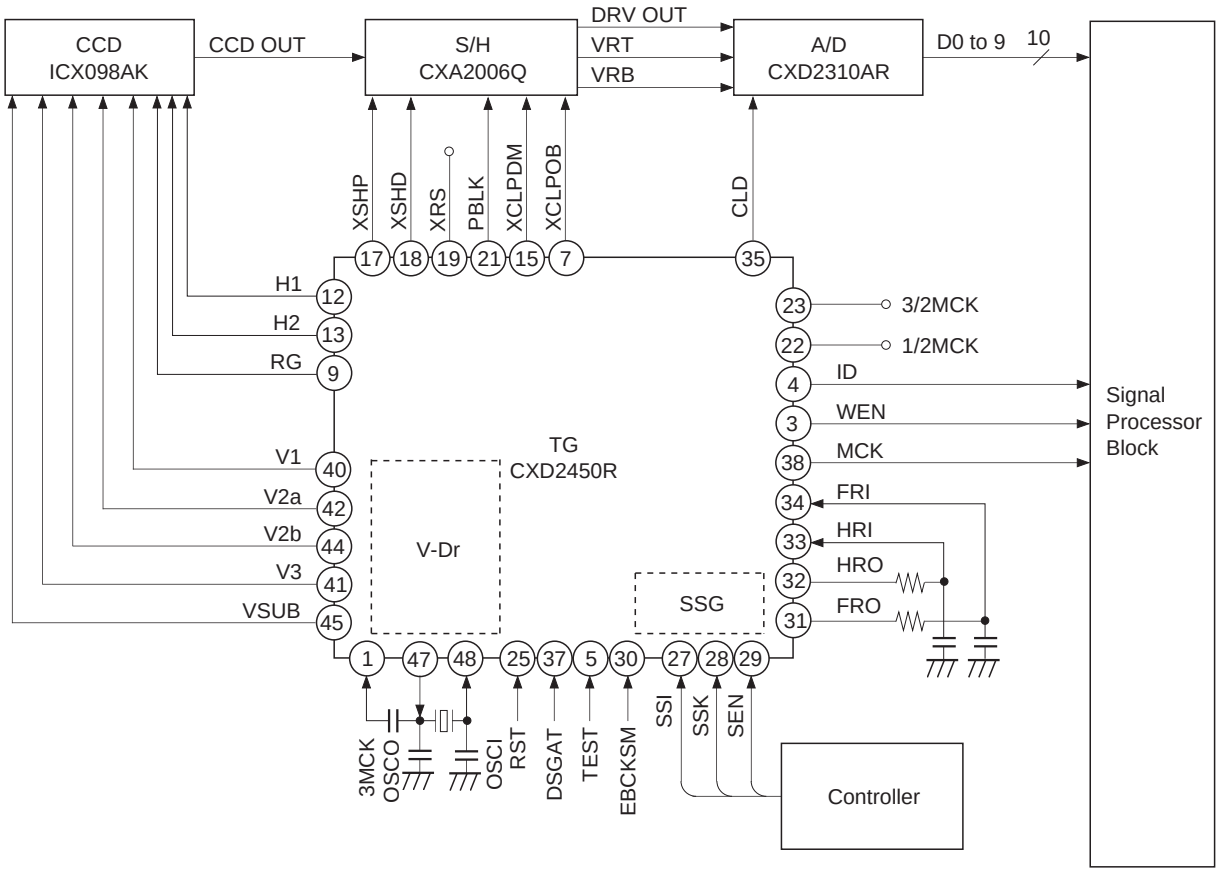
MODE (Base oscillation frequency: 2340f_H)

Applicable CCD image sensor:
ICX098AK



* HRI' indicates the HRI which is the actual CXD2450R load timing.
* The 3/2MCK and 1/2MCK polarities can be inverted by the serial interface data. This chart indicates the status in which 3/2MCK is negative polarity and 1/2MCK is positive polarity.

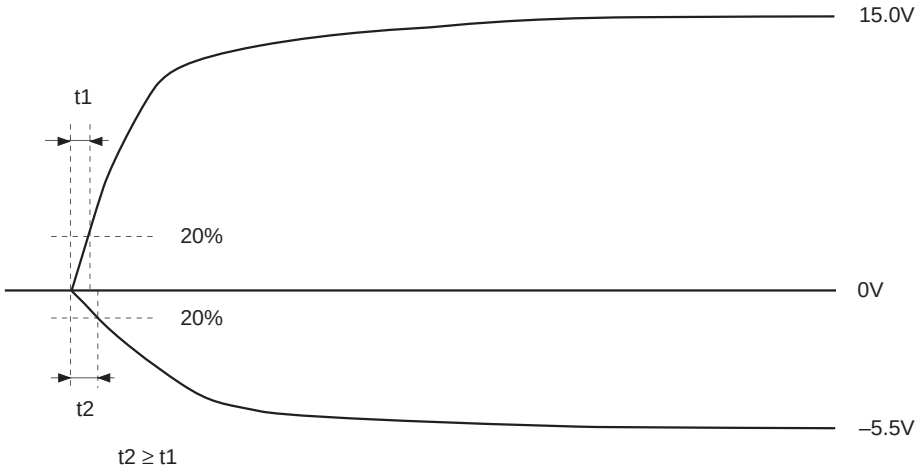
Application Circuit Block Diagram



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

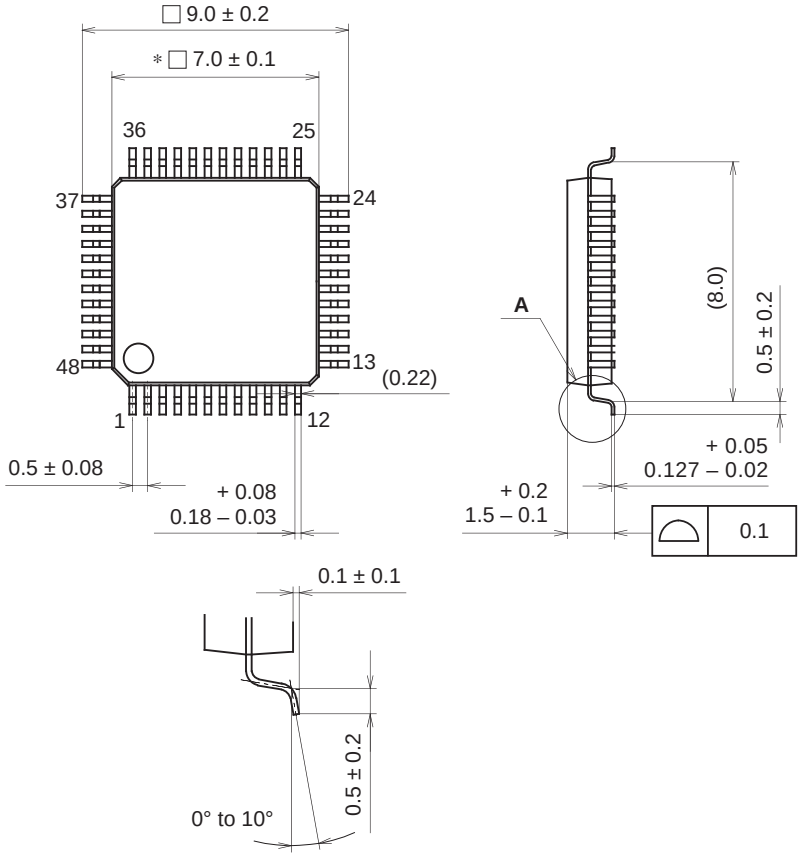
Notes for Power-on

Of the three –5.5V, +15.0V and +3.3V power supplies, be sure to start up the –5.5V and +15.0V power supplies in the following order to prevent the VSUB pin of the CCD image sensor from going to negative potential.



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: "∗" Dimensions do not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	QFP048-P-0707
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE WEIGHT	0.2g