SONY

CXD2510Q

CD Digital Signal Processor

Description

The CXD2510Q is a digital signal processor LSI for CD players and is equipped with the following functions.

- Wide frame jitter margin (±28 frames) due to a built-in 32K RAM
- Bit clock, which strobes the EFM signal, is generated by the digital PLL
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
- Quadruple-speed, double-speed and variable pitch playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub Q data error correction
- Digital spindle servo (built-in oversampling filter)
- 16-bit traverse counter
- Asymmetry compensation circuit
- Serial bus-based CPU interface
- Error correction monitor signals are output from a new CPU interface.
- Servo auto sequencer
- Fine search which performs high-precision track jumps
- Digital audio interface output
- Digital level meter, peak meter
- Bilingual compatible

Features

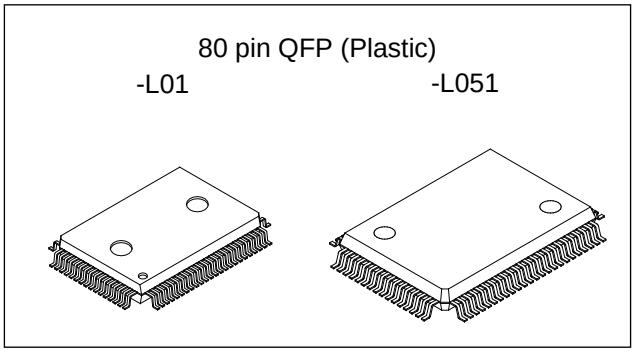
- All digital signals processed with a single chip during playback
- High-integrated mounting possible due to a built-in RAM

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
		(V_{SS} – 0.3V to V_{DD} + 0.3V)	
• Output voltage	V_O	–0.3 to +7.0	V
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage difference			
	Vss – AVss	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V



Recommended Operating Conditions

• Supply voltage	V_{DD}*	4.50 to 5.50	V
• Operating temperature	Topr	–20 to +75	°C

* The V_{DD} (min.) for the CXD2510Q varies according to the playback speed and built-in VCO selection. The V_{DD} (min.) is 4.50 V when high speed VCO and quadruple-speed playback are selected (variable pitch off). The V_{DD} (min.) for the CXD2510Q under various conditions are as shown in the following table.

Playback speed	V_{DD} (min.) [V]	
	VCO high-speed	VCO normal-speed
× 4	4.50	—
× 2*1	4.00	—
× 2	3.40	4.00
× 1	3.40	3.40
× 1*2	3.40	3.40

Dashes indicate that there is no assurance of the processor operating. All values are for variable pitch off.

*1 When the internal operation of the LSI is set to normal-speed playback and the operating clock of the signal processor is doubled, double-speed playback results.

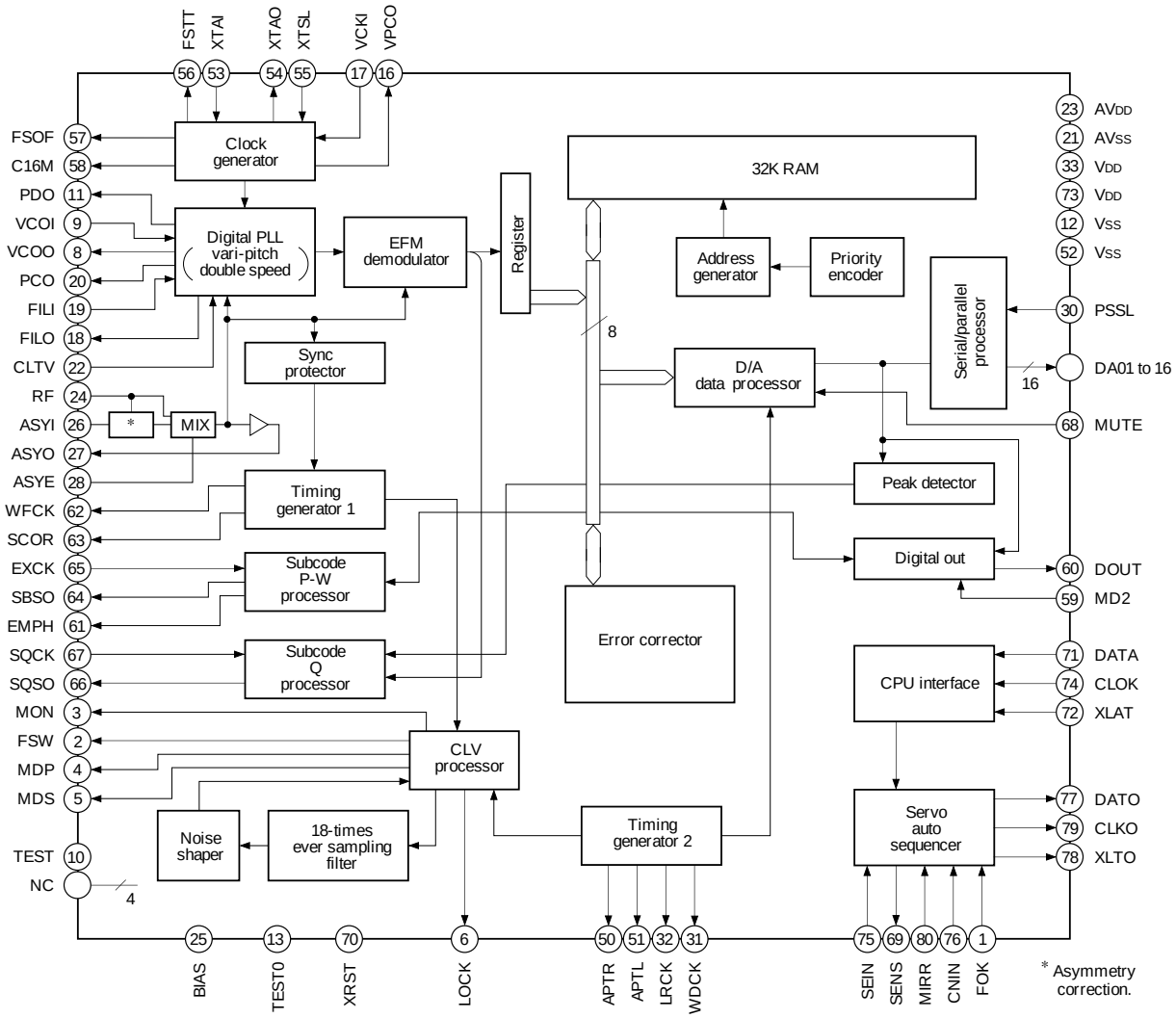
*2 When the internal operation of the LSI is set to double-speed mode and the crystal oscillating frequency is halved in low power consumption mode, normal-speed playback results.

Input/output Capacitances

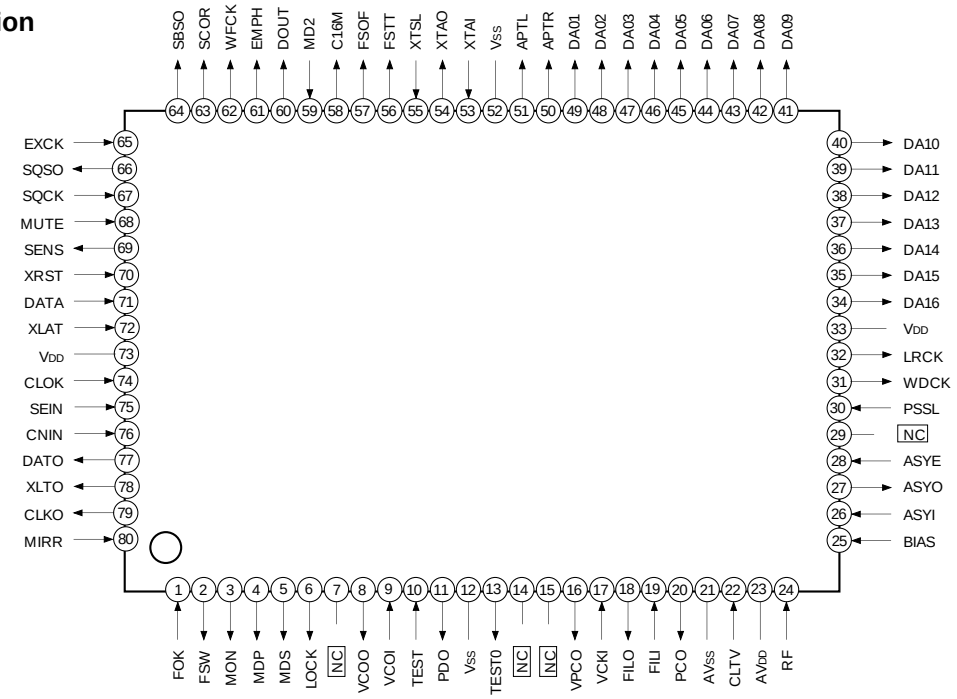
• Input capacitance	C_I	12 (max.)	pF
• Output capacitance	C_O	12 (max.)	pF
		for high impedance	
Note) Measurement conditions		V_{DD} = V_I = 0V	
		f_M = 1MHz	

E94412A11

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
2	FSW	O	Z, 0	Spindle motor output filter switching output.
3	MON	O	1, 0	Spindle motor on/off control output.
4	MDP	O	1, Z, 0	Spindle motor servo control.
5	MDS	O	1, Z, 0	Spindle motor servo control.
6	LOCK	O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
7	NC	—		
8	VCOO	O	1, 0	Analog EFM PLL oscillation circuit output.
9	VCOI	I		Analog EFM PLL oscillation circuit input. f_{LOCK} = 8.6436MHz.
10	TEST	I		TEST pin. Normally GND.
11	PDO	O	1, Z, 0	Analog EFM PLL charge pump output.
12	Vss			GND
13	TEST0	—		TEST output pin. Normally open.
14	NC	—		
15	NC	—		
16	VPCO	O	1, Z, 0	Variable pitch PLL charge pump output.
17	VCKI	I		Variable pitch clock input from the external VCO. fc center = 16.9344MHz.
18	FILO	O	Analog	Master PLL filter output.
19	FILI	I		Master PLL filter input.
20	PCO	O	1, Z, 0	Master PLL charge pump output.
21	AVss			Analog GND.
22	CLTV	I		Master VCO control voltage input.
23	AV_{DD}			Analog power supply (5V).
24	RF	I		EFM signal input.
25	BIAS	I		Constant current input of the asymmetry circuit.
26	ASYI	I		Asymmetry comparator voltage input.
27	ASYO	O	1, 0	EFM full-swing output (low = Vss, high = V_{DD}).
28	ASYE	I		Low: asymmetry circuit off; high: asymmetry circuit on
29	NC	—		
30	PSSL	I		Audio data output mode switching input. Low: serial output; high: parallel output.
31	WDCK	O	1, 0	D/A interface for 48-bit slot. Word clock f = 2Fs.
32	LRCK	O	1, 0	D/A interface for 48-bit slot. LR clock f = Fs.
33	V_{DD}			Power supply (5V).

Pin No.	Symbol	I/O		Description
34	DA16	O	1, 0	DA16 (MSB) output when PSSL = 1. 48-bit slot serial data (two's complement, MSB first) when PSSL = 0.
35	DA15	O	1, 0	DA15 output when PSSL = 1. 48-bit slot bit clock when PSSL = 0.
36	DA14	O	1, 0	DA14 output when PSSL = 1. 64-bit slot serial data (two's complement, LSB first) when PSSL = 0.
37	DA13	O	1, 0	DA13 output when PSSL = 1. 64-bit slot bit clock when PSSL = 0.
38	DA12	O	1, 0	DA12 output when PSSL = 1. 64-bit slot LR clock when PSSL = 0.
39	DA11	O	1, 0	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
40	DA10	O	1, 0	DA10 output when PSSL = 1. XUGF output when PSSL = 0.
41	DA09	O	1, 0	DA09 output when PSSL = 1. XPLCK output when PSSL = 0.
42	DA08	O	1, 0	DA08 output when PSSL = 1. GFS output when PSSL = 0.
43	DA07	O	1, 0	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
44	DA06	O	1, 0	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
45	DA05	O	1, 0	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
46	DA04	O	1, 0	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
47	DA03	O	1, 0	DA03 output when PSSL = 1. MNT2 output when PSSL = 0.
48	DA02	O	1, 0	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
49	DA01	O	1, 0	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
50	APTR	O	1, 0	Aperture compensation control output. This pin outputs a high signal when the right channel is used.
51	APTL	O	1, 0	Aperture compensation control output. This pin outputs a high signal when the left channel is used.
52	Vss			GND
53	XTAI	I		16.9344MHz crystal oscillation circuit input. Also the 33.8688MHz input.
54	XTAO	O	1, 0	16.9344MHz crystal oscillation circuit output.
55	XTSL	I		Crystal selector input. The crystal is low for 16.9344MHz, and high for 33.8688MHz.
56	FSTT	O	1, 0	2/3 frequency divider output for Pins 53 and 54. This pin does not change with the variable pitch.
57	FSOF	O	1, 0	1/4 frequency divider output for Pins 53 and 54. This pin does not change with the variable pitch.
58	C16M	O	1, 0	16.9344MHz output. This pin changes simultaneously with the variable pitch.
59	MD2	I		Digital-out on/off control. High: on; low: off
60	DOUT	O	1, 0	Digital-out output.
61	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
62	WFCK	O	1, 0	WFCK (write frame clock) output.
63	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	1, 0	Sub P to W serial output.
65	EXCK	I		SBSO readout clock input.

Pin No.	Symbol	I/O		Description
66	SQSO	O	1, 0	Sub Q 80-bit and PCM peak and level data 16-bit output.
67	SQCK	I		SQSO readout clock input.
68	MUTE	I		High: mute; low: release
69	SENS	—	1, Z, 0	SENS output to CPU.
70	XRST	I		System reset. Reset when low.
71	DATA	I		Serial data input from CPU.
72	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
73	V_{DD}			Power supply (5V).
74	CLOK	I		Serial data transfer clock input from CPU.
75	SEIN	I		SENS input from SSP.
76	CNIN	I		Track jump count signal input.
77	DATO	O	1, 0	Serial data output to SSP.
78	XLTO	O	1, 0	Serial data latch output to SSP. Latched at the falling edge.
79	CLKO	O	1, 0	Serial data transfer clock output to SSP.
80	MIRR	I		Mirror signal input.

Notes)

- The 64-bit slot is an LSB first, two's complement output, and the 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µ.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

Electrical Characteristics

DC Characteristics (V_{DD} = AV_{DD} = 5.0V ± 10%, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –1mA	V_{DD} – 0.5		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 1mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –1mA	V_{DD} – 0.5		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 2mA	0		0.4	V	
Output voltage (3)	Low level output voltage	V_{OL} (3)	I_{OL} = 2mA	0		0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*7
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current		I_{LI}	V_I = 0 to 5.50V	–5		5	µA	*1, 2, 3
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.50V	–5		5	µA	*8

Applicable pins

*1 XTSL, DATA, XLAT, MD2, PSSL

*2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, MIRR, VCKI, ASYE

*3 CLTV, FILI, RF

*4 MDP, PDO, PCO, VPCO

*5 ASYO, DOUT, FSTT, FSOF, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO, CLKO, XLTO, SENS, MDS, DA01 to DA16, APTR, APTL, LRCK, WFCK

*6 FSW

*7 FILO

*8 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

AC Characteristics

1. XTAI pin, VCOI pin

(1) When using self-oscillation

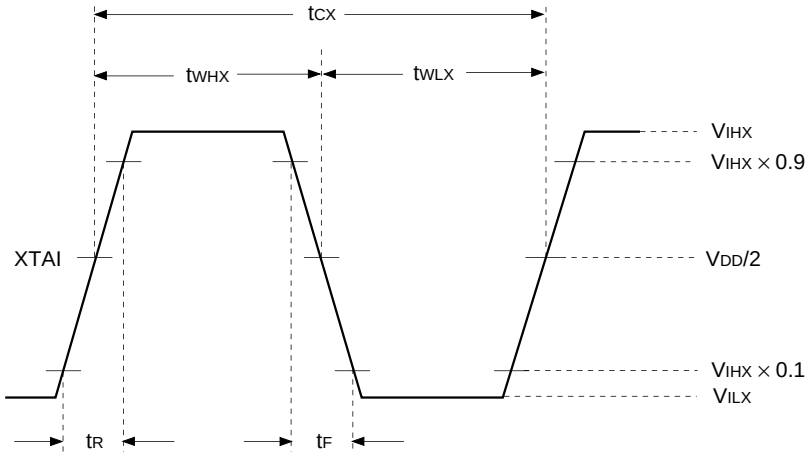
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(2) When inputting pulses to XTAI and VCOI

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1,000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(3) When inputting sine waves to XTAI and VCOI pins via a capacitor

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

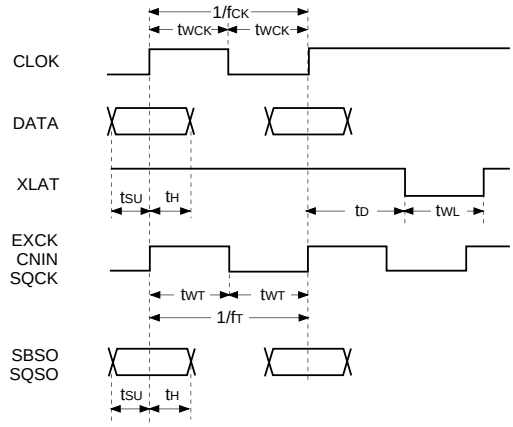
Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

2. CLOK, DATA, XLAT, CNIN, SQCK EXCK pins

(V_{DD} = AV_{DD} = 5.0V ± 10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65	MHz
EXCK SQCK pulse width	t_{WT}	750			ns
CNIN freqency *	f_T			65	kHz
CNIN pulse width *	t_{WT}	7.5			µs

* When $44 and $45 are excuted.



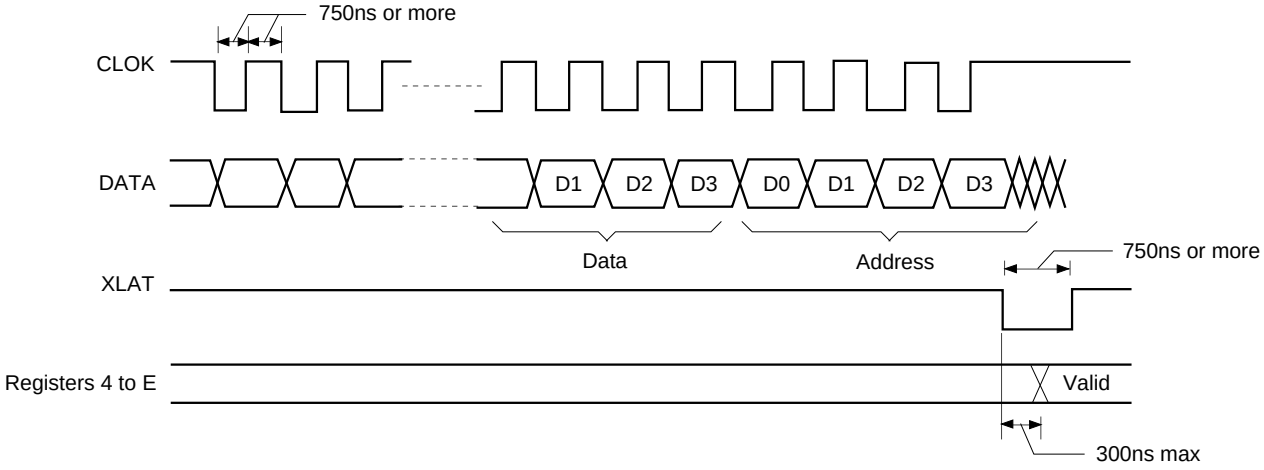
Description of Functions

§1. CPU Interface and Instructions

• CPU interface

This interface uses DATA, CLOK, and XLAT to set the modes.

The interface timing chart is shown below.



• Information on each address and the data is provided in Table 1-1.

• The internal registers are initialized by a reset when XRST = 0; the initialization data is shown in Table 1-2.

Command Table

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0	—	—	—	—
5	Blind (A, E), Overflow (C, G) Brake (B)	0	1	0	1	TR3	TR2	TR1	TR0	—	—	—	—	—	—	—	—	—	—	—	—
6	Sled_kick, brake (D) Kick (F)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT Mute	D.out Mute-F	WSEL	VCO SEL	ASHS	SOCT	0	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	DCLV ON-OFF	DSPB ON-OFF	ASEQ ON-OFF	DPLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	Vari Up	Vari Down	Mute	ATT	PCT1	PCT2	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	0	Gain DCLV0	0	0	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWM MD	TB	TP	Gain CLVS	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-1.

Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C, G) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	Sled_kick, brake (D) Kick (F)	0	1	1	0	0	1	1	1	0	0	0	0	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Servo coefficient setting	1	1	0	0	0	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-2.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
FineSearch	0	1	0	RXF
Focus-On	0	1	1	1
1 TrackJump	1	0	0	RXF
10 TrackJump	1	0	1	RXF
2N TrackJump	1	1	0	RXF

RXF = 0 Forward

RXF = 1 Reverse

- When the FOCUS-ON command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the TRACK JUMP commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

Max. timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To invalidate the MAX timer, set the MAX timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequence track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequencer track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N track jump is executed, and the jump count setting when fine search is executed for auto sequence.

- The maximum track count is 65,535, but note that with 2N track jumps the maximum track jump count is determined by the mechanical limitations of the optical system.
- When N is from 0 to 15, the number of 2N track jumps is counted according to the signals input from the CNIN pin. When N is 16 or over, it is counted according to the signals input from the MIRR pin.

$8X commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	CDROM	DOUT Mute	D.out Mute-F	WSEL	VCO SEL	ASHS	SOCT	0

Command bit	C2PO timing	Processing
CDROM = 1	See the Timing Chart 1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See the Timing Chart 1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output
0	0	0	0	off	0dB
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		–∞dB
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	0dB	0dB
1	0	0	1		–∞dB
1	0	1	0	–∞dB	0dB
1	0	1	1		–∞dB
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Processing	Use
VCOSEL = 0	The built-in VCO is set to normal-speed.	Used for normal-speed and double-speed (double correction) playback.
VCOSEL = 1	The built-in VCO is set to high-speed.	Used for quadruple-speed and double-speed (quadruple correction) playback.

Command bit	Function	Use
ASHS = 0	The command transfer rate to SSP is set to normal-speed.	Used for normal-speed and double-speed (double correction) playback.
ASHS = 1	The command transfer rate to SSP is set to half-speed.	Used for quadruple-speed and double-speed (quadruple correction) playback.

Command bit	Function
SOCT = 0	Sub Q is output from the SQSO pin.
SOCT = 1	Each output signal is output from the SQSO pin. Input the readout clock to SQCK. (See the Timing Chart 2-4.)

$9X commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0

Command bit	CLV mode	Contents	
DCLV on/off = 0	During CLVS mode	FSW = low, MON = high, MDS = Z; MDP = servo control signal, carrier frequency of 230Hz at T_B = 0, and 460Hz at T_B = 1.	
	During CLVP mode	FSW = Z, MON = high; MDS = speed control signal, carrier frequency of 7.35kHz; MDP = phase control signal, carrier frequency of 1.8kHz.	
DCLV on/off = 1 (FSW, MON not required)	During CLVS and CLVP modes	When DCLV PWM and MD = 1	MDS = PWM polarity signal, carrier frequency of 132kHz. MDP = PWM absolute value output (binary), carrier frequency of 132kHz.
		When DCLV PWM and MD = 0	MDS = Z MDP = ternary PWM output, carrier frequency of 132kHz.

When DCLV on/off = 1 for the Digital CLV servo, the sampling frequency of the internal digital filter switches simultaneously with the CLVP/CLVS switching.

Therefore, the cut-off frequency for the CLVS is fc = 70Hz when T_B = 0, and fc = 140Hz when T_B = 1.

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error correction quadruple correction, variable pitch possible.
DSPB = 1	Double-speed playback, C2 error correction double correction, variable pitch prohibited.

FLFC is normally 0.

SENS output

Microcomputer serial register value (latching not required)	ASEQ = 0	ASEQ = 1
$0X	Z	SEIN (FZC)
$1X	Z	SEIN (A.S)
$2X	Z	SEIN (T.Z.C)
$3X	Z	SEIN (SSTOP)
$4X	Z	XBUSY
$5X	Z	FOK
$6X	Z	SEIN (Z)
$AX	GFS	GFS
$BX	COMP	COMP
$CX	COUT	COUT
$EX	$\overline{OV64}$	$\overline{OV64}$
$7X, 8X, 9X, DX, FX	Z	0

Description of SENS signals

SENS output	Meaning
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the played back frame sync is obtained with the correct timing.
COMP	Measures the number of tracks set with Reg B. High when Reg B is latched, low when the initial Reg B number is input by CNIN.
COUT	Measures the number of tracks set with Reg B. High when Reg B is latched, toggles each time the Reg B number is input by CNIN. While $44 and $45 are being executed, toggles with each CNIN 8-count instead of the Reg B number.
$\overline{OV64}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.

Command bit	Meaning
DPLL = 0*	RFPLL is analog. PDO, VCOI and VCOO are used.
DPLL = 1	RFPLL is digital. PDO is impedance.

* External parts for Pins 18 to 20 are required even when analog PLL is selected.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO:

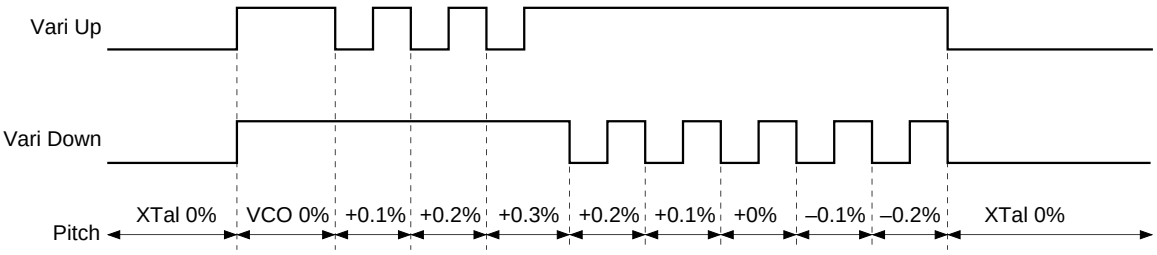
The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

$AX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Audio CTRL	Vari Up	Vari Down	Mute	ATT	PCT1	PCT2	0	0



Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off.
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When MUTE pin = 1.
(3) When register 8 D.out mute = 1 and the Digital out is on (MD2 pin = 1).
(4) When GFS stays low for over 35ms (at normal speed).
(5) When register 9 BiliGL MAIN = Sub = 1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1ms time limit.

Command bit		Meaning	PCM Gain	ECC correction ability
PCT1	PCT2			
0	0	Normal mode	× 0dB	C1: double; C2: quadruple
0	1	Level meter mode	× 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	× 0dB	C1: double; C2: double

Description of level meter mode (see the Timing Chart 1-4.)

- When this LSI is set to this mode, it can possess digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits of data are Sub Q data (see §2. Subcode Interface). The last 16 bits are LSB first 15-bit PCM data (absolute values). The final bit is PCM data. However, it is high when generated by the left channel and low when generated by the right channel.
- PCM data is reset and the L/R flag is reversed after one readout.
  The maximum value for this status is then measured until the next readout.

Description of peak meter mode (see the Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the LSI internal register is reset.
  In other words, the PCM maximum value detection register is not reset by the readout.
- To reset the PCM maximum value register, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Relative time operates as normal.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (–∞) for this mode.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set when the traverse status is monitored by the SENS output COMP and COUT.

$CX commands

Command	Data 1				Data 2				Explanation
	D3	D2	D1	D0	D3	D2	D1	D0	
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	0	Gain DCLV0	0	0	Valid only when DCLV = 1.
CLV CTRL ($DX)				Gain CLVS					Valid when DCLV = 1 or 0.

The spindle servo gain is externally set when DCLV = 1.

- CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note) When DCLV = 0, the CLVS gain is as follows.
When Gain CLVS = 0, GCLVS = –12dB.
When Gain CLVS = 1, GCLVS = 0dB.

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV0	GDCLV
0	0dB
1	+6dB

$DX commands

Command	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS

See the $CX commands

Command bit	Explanation (See the Timing Chart 1-6.)
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output.

Command bit	Explanation
TB = 0	Bottom hold in CLVS and CLVH modes at a cycle of RFCK/32.
TB = 1	Bottom hold in CLVS and CLVH modes at a cycle of RFCK/16.
TP = 0	Peak hold in CLVS mode at a cycle of RFCK/4.
TP = 1	Peak hold in CLVS mode at a cycle of RFCK/2.

Note) Peak hold is performed at 34kHz in CLVH mode.

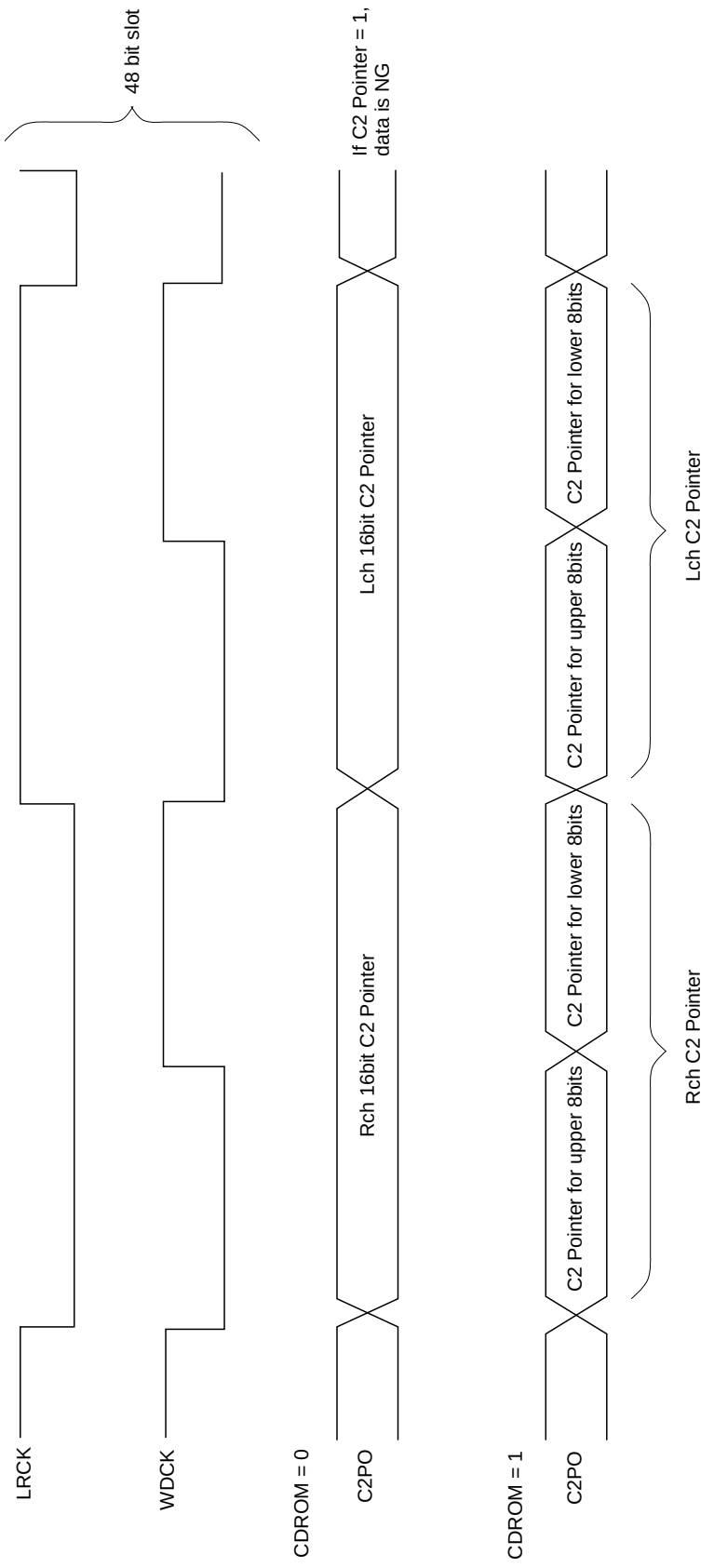
$EX commands

Command	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0

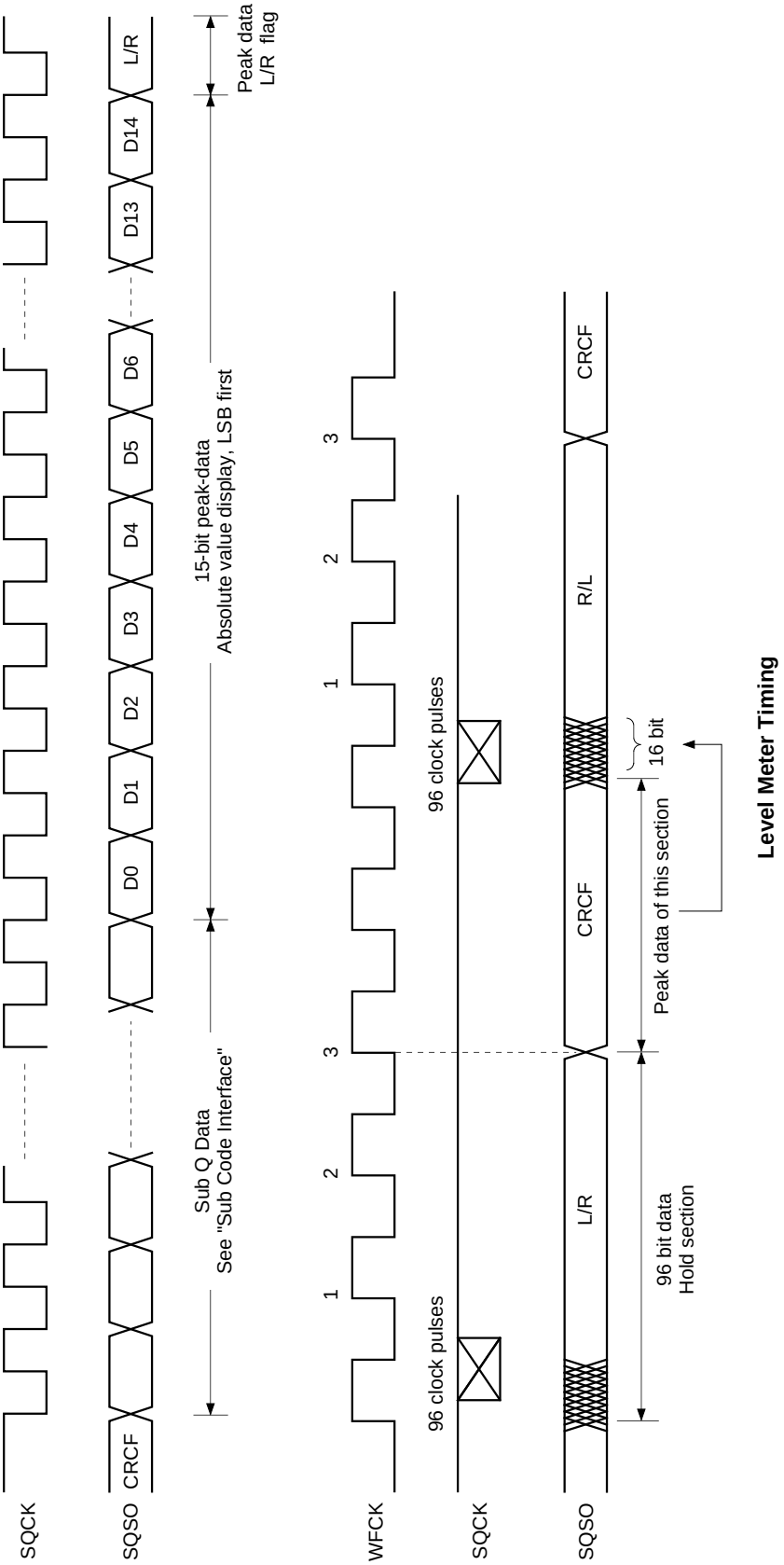
CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See the Timing Chart 1-7.
1	0	0	0	KICK	See the Timing Chart 1-8.
1	0	1	0	BRAKE	See the Timing Chart 1-9.
1	1	1	0	CLVS	
1	1	0	0	CLVH	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP : Spindle motor stop mode.
KICK : Spindle motor forward rotation mode.
BRAKE : Spindle motor reverse rotation mode.
CLVS : Rough servo mode. When the RF-PLL circuit lock is disengaged, this mode is used to pull the disc rotations within the RF-PLL capture range.
CLVP : PLL servo mode.
CLVA : Automatic CLVS/CLVP switching mode. This mode is normally used during playback.

Timing Chart 1-3

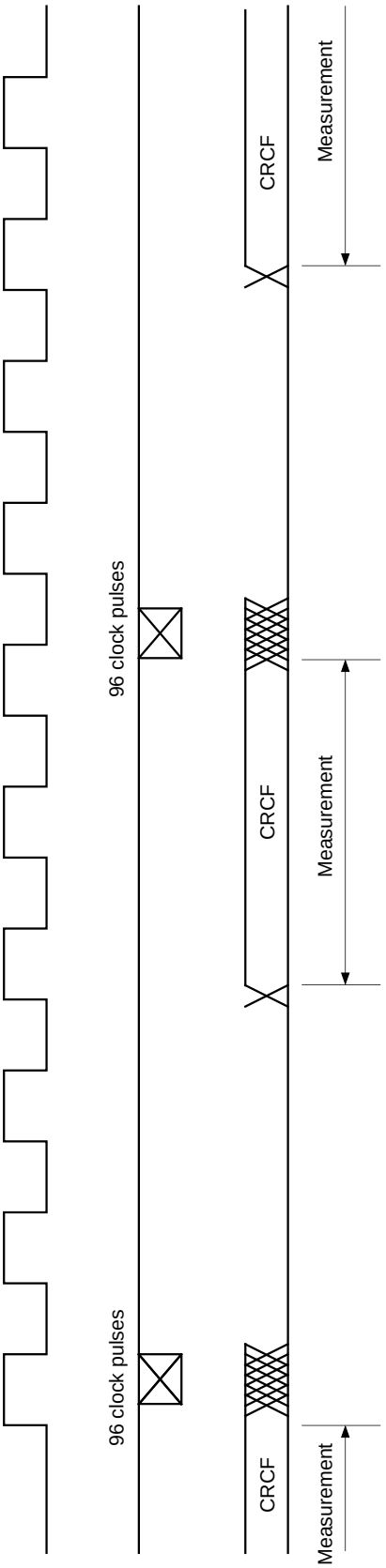


Timing Chart 1-4



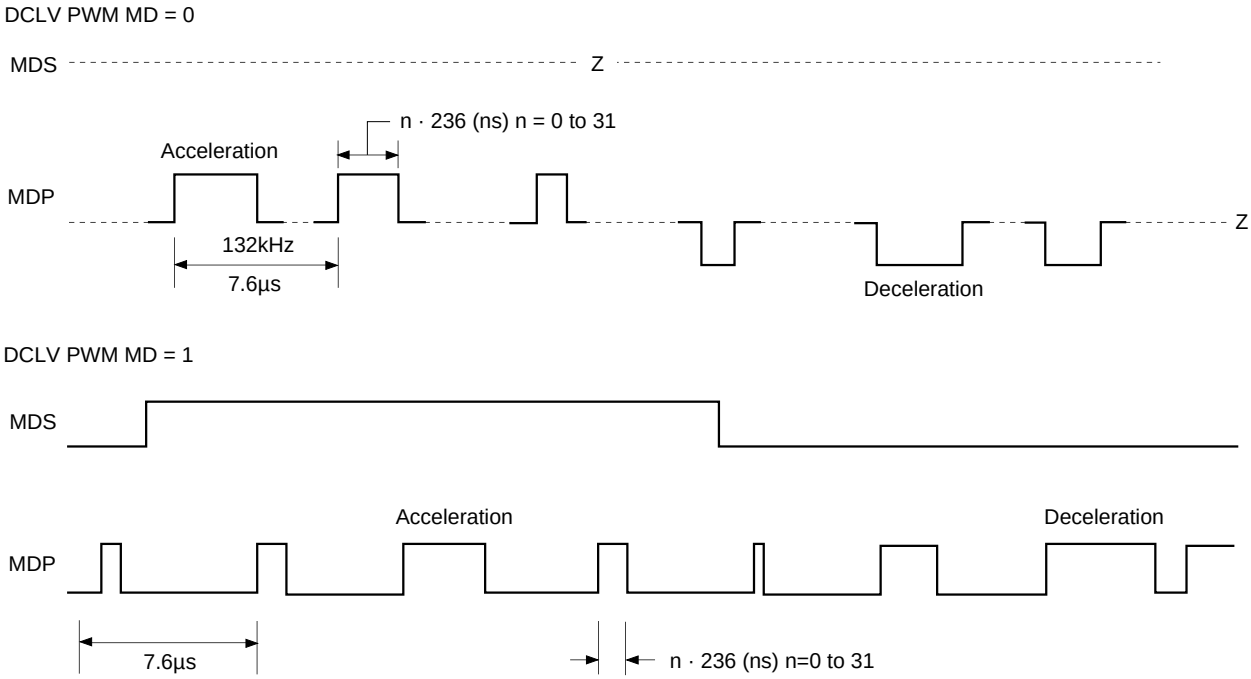
Level Meter Timing

Timing Chart 1-5



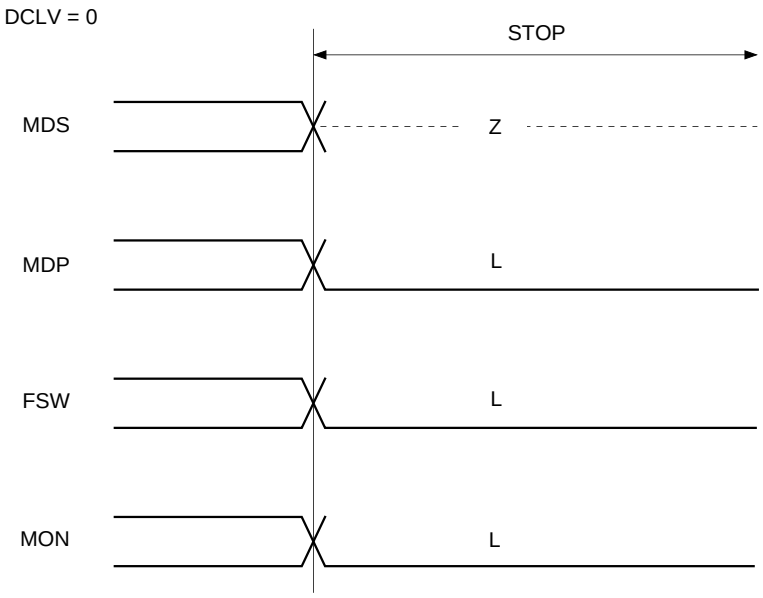
Peak Meter Timing

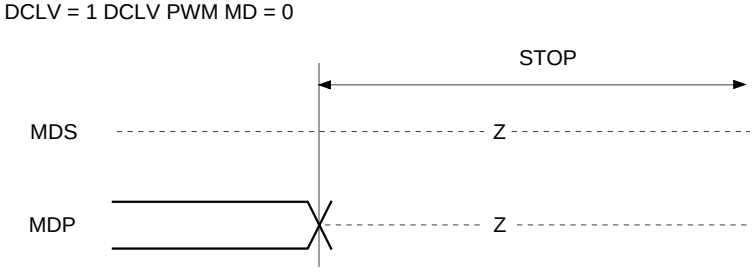
Timing Chart 1-6



Output Waveforms with DCLV = 1

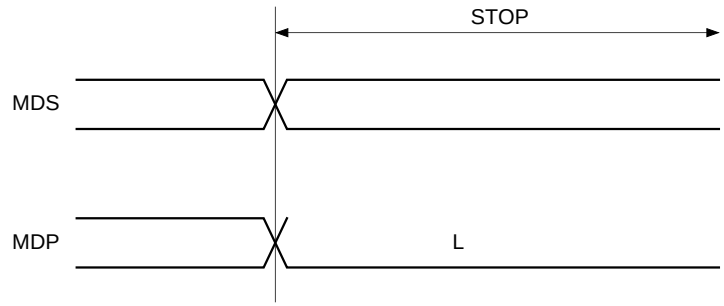
Timing Chart 1-7





FSW and MON are the same as for DCLV = 0

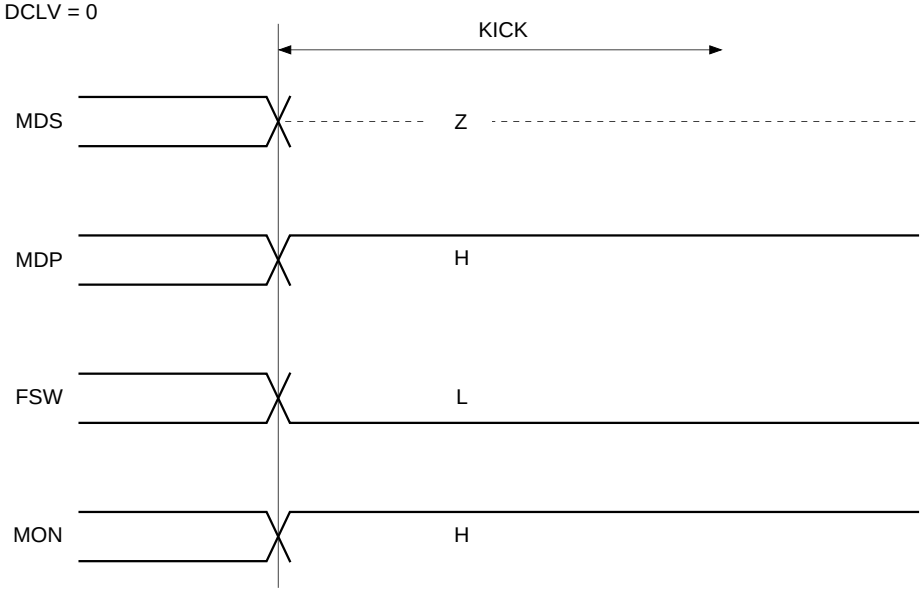
DCLV = 1 DCLV PWM MD = 1



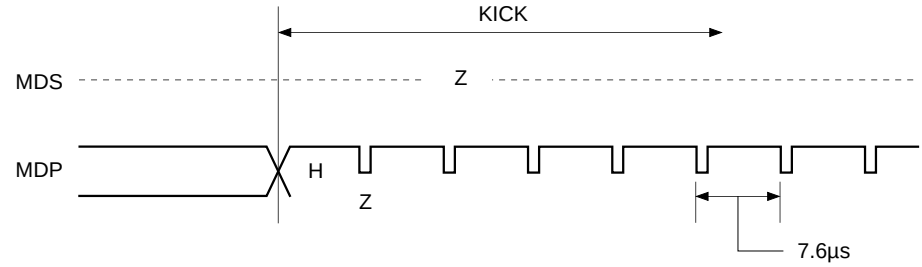
FSW and MON are the same as for DCLV = 0

Timing Chart 1-8

DCLV = 0

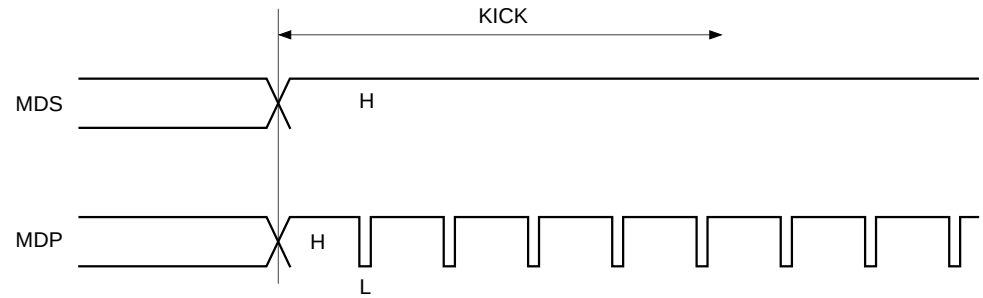


DCLV = 1 DCLV PWM MD = 0



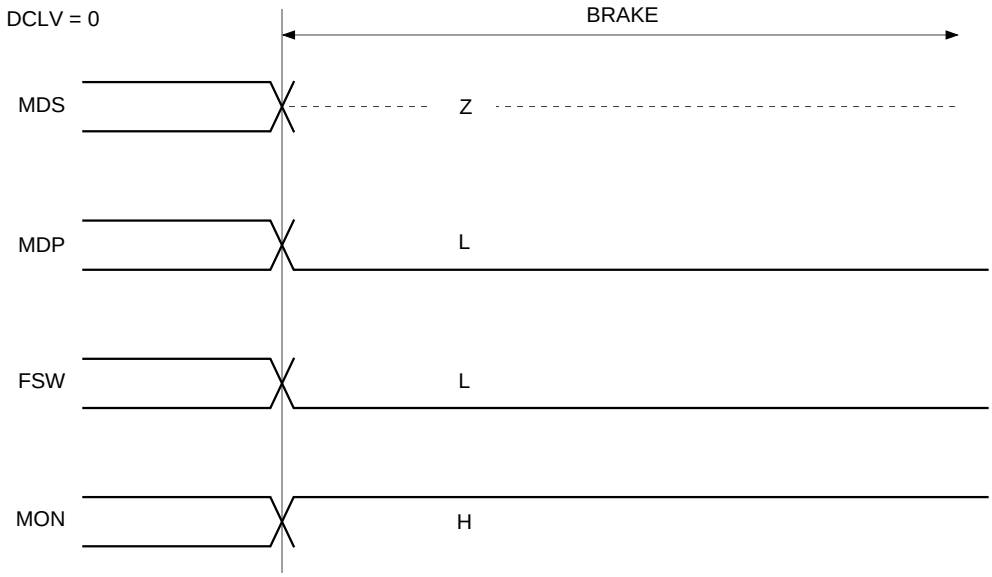
FSW and MON are the same as for DCLV = 0

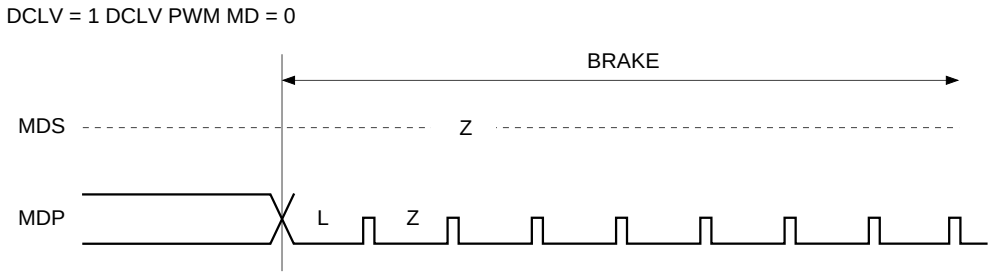
DCLV = 1 DCLV PWM MD = 1



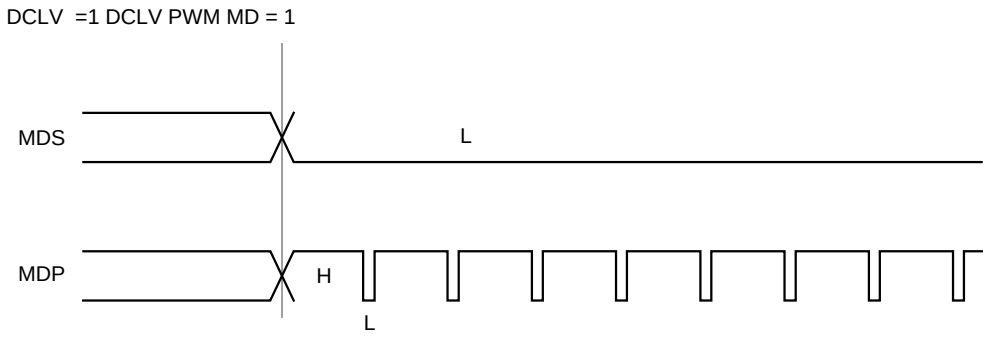
FSW and MON are the same as for DCLV = 0

Timing Chart 1-9





FSW and MON are the same as for DCLV = 0



FSW and MON are the same as for DCLV = 0

§2. Subcode Interface

This section explains the subcode interface.
There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read from SBSO by inputting EXCK.
Sub Q can be read out after the CRC check of the 80 bits of information in the subcode frame.
This is accomplished, after checking SCOR and CRCF, by inputting 80 clock pulses to SQCK and reading data from the SQSO pin.

§2-1. P to W Subcode Read

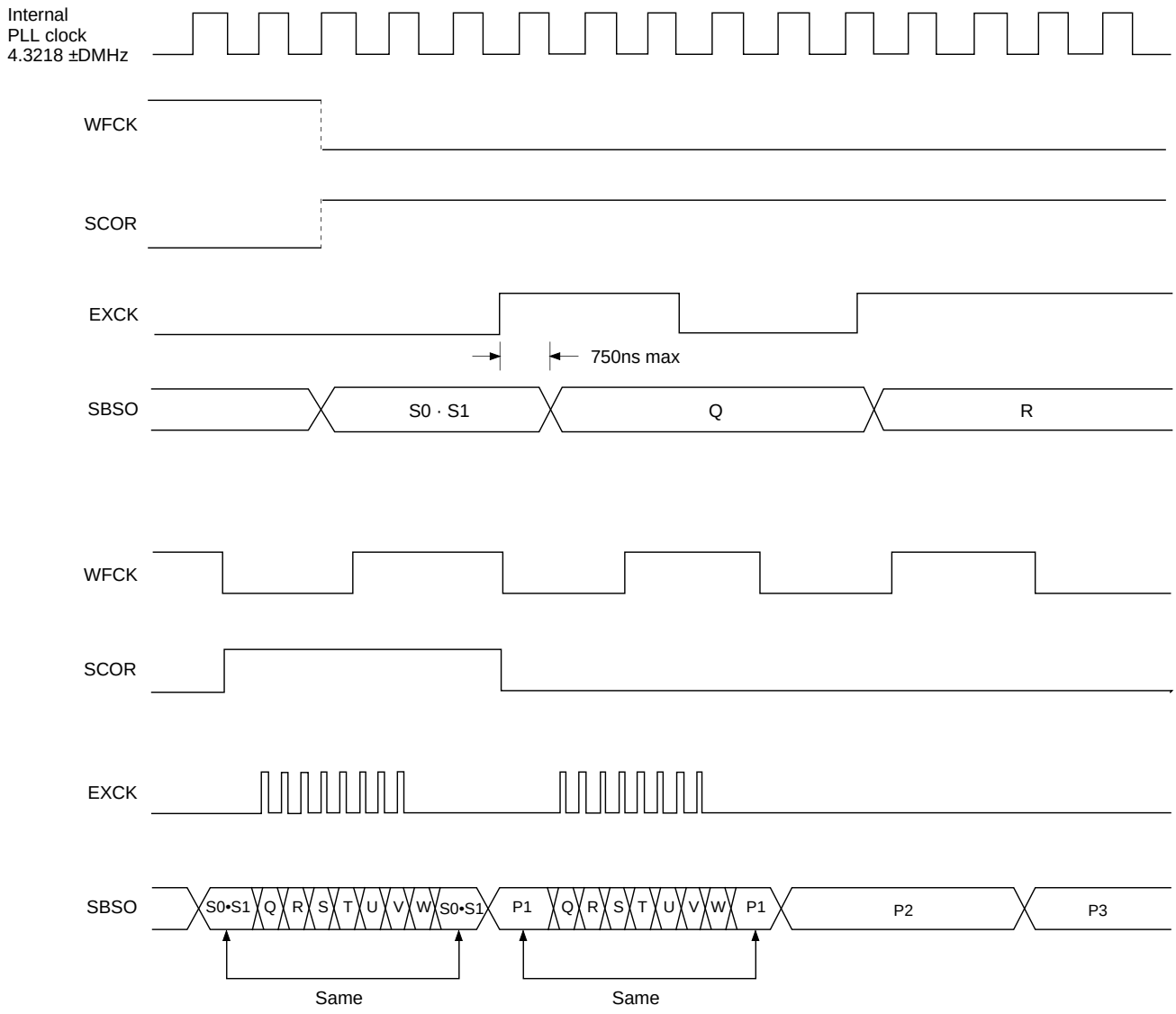
Data can be read out by inputting EXCK immediately after WFCK falls. (See the Timing Chart 2-1.)

§2-2. 80-bit Sub Q read

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

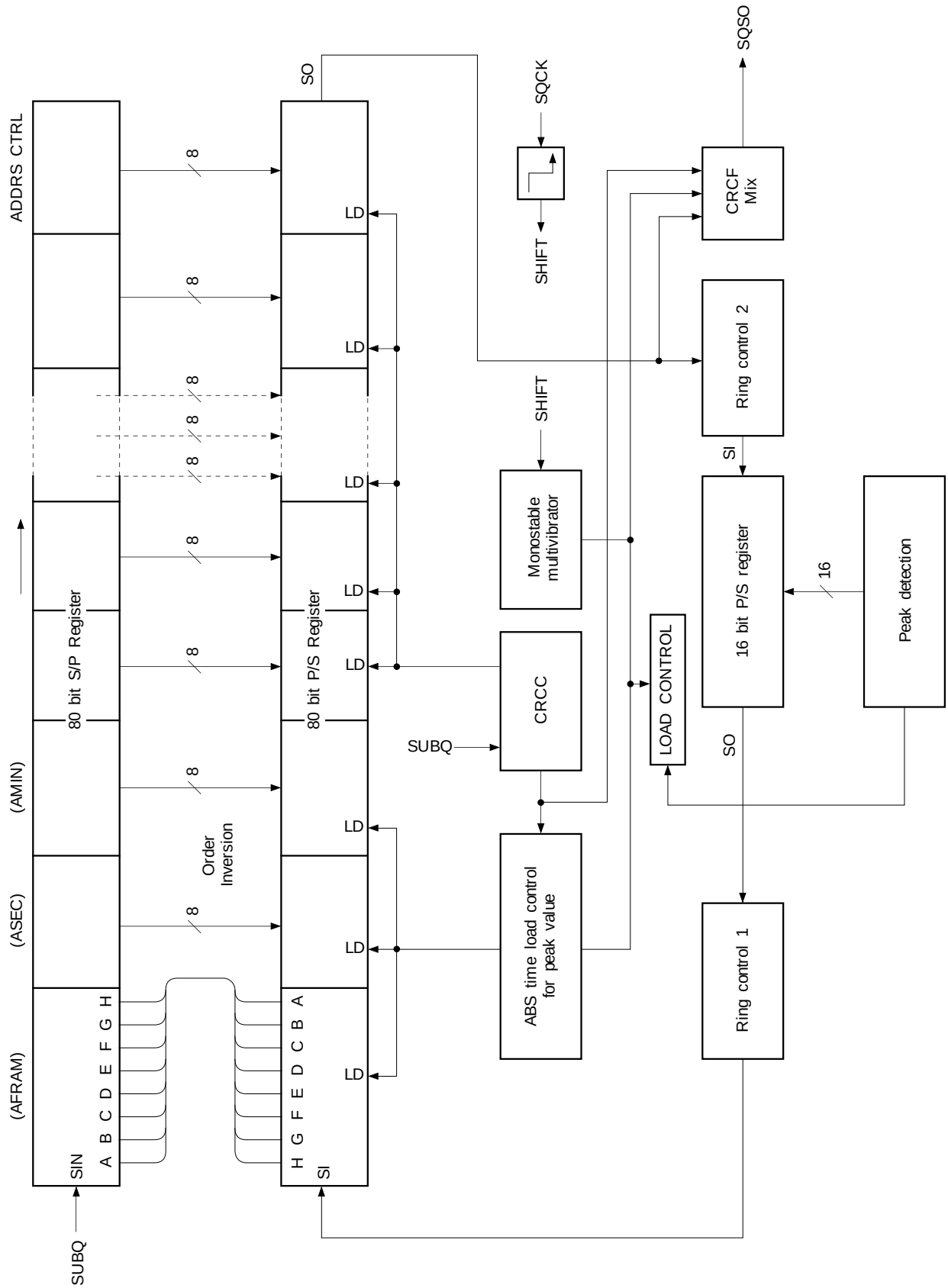
- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.
  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- In the CXD2510Q, when 80-bit data is loaded, the order of the MSB and LSB is inverted for each byte. As a result, although the sequence of bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the fact that the 80-bit data has been loaded is confirmed, SQCK is input so that the data can be read. In this LSI, the SQCK input is detected, and the retriggerable monostable multivibrator is reset during low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration that SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than the monostable multivibrator time constant, the register will not be rewritten by CRCOK and others.
- In this LSI, the previously mentioned peak detection register can be connected to the shift-in of the 80-bit P/S register.
  Input and output for ring control 1 are shorted in peak meter or level meter mode.
  Ring control 2 is shorted in peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result, the 96-bit clock must be input in peak meter mode.
- In addition, as previously mentioned, the absolute time after peak is generated is stored in the memory in peak meter mode.
  Fig. 2-3 shows the Timing Chart.
- Although a clock is input from the SQCK pin to actually perform these operations, the high and low intervals for this clock should be between 750ns and 120µs.

Timing Chart 2-1

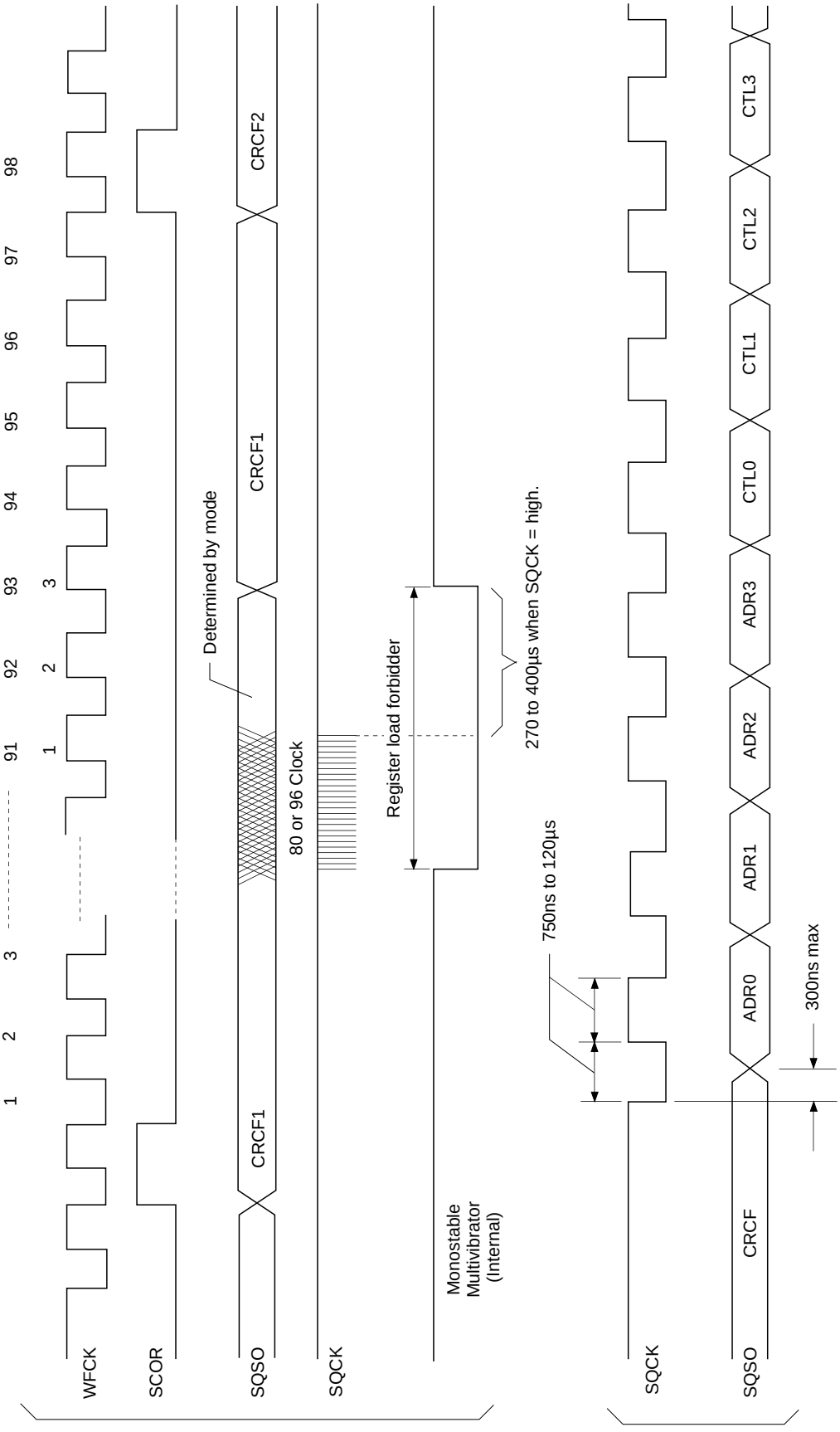


Subcode P.Q.R.S.T.U.V.W Read Timing

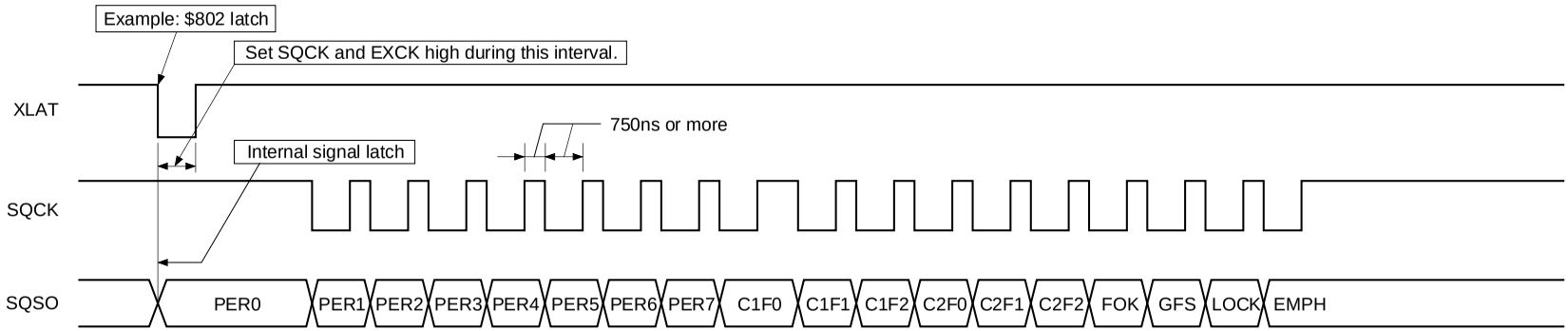
Block Diagram 2-2



Timing Chart 2-3



Timing Chart 2-4



Signal	Explanation
PER0 to PER7 *	RF jitter amount (used to adjust the focus bias). 8bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460 Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
EMPH	Outputs a high signal when the playback disc has emphasis.

* RF jitter amount, PER0 to PER7 is output in binary code.When RF jitter amount is little, value of binary code is small.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors ; C1 pointer reset
0	0	1	One C1 error corrected ; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors ; C1 pointer set
1	0	1	One C1 error corrected ; C1 pointer set
1	1	0	Two C1 errors corrected ; C1 pointer set
1	1	1	C1 correction impossible ; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors ; C2 pointer set
0	0	1	One C2 error corrected ; C2 pointer reset
0	1	0	Two C2 errors corrected ; C2 pointer reset
0	1	1	Three C2 errors corrected ; C2 pointer reset
1	0	0	Four C2 errors corrected ; C2 pointer reset
1	0	1	—
1	1	0	C2 correction impossible ; C1 pointer copy
1	1	1	C2 correction impossible ; C2 pointer set

§3. Description of Other Functions

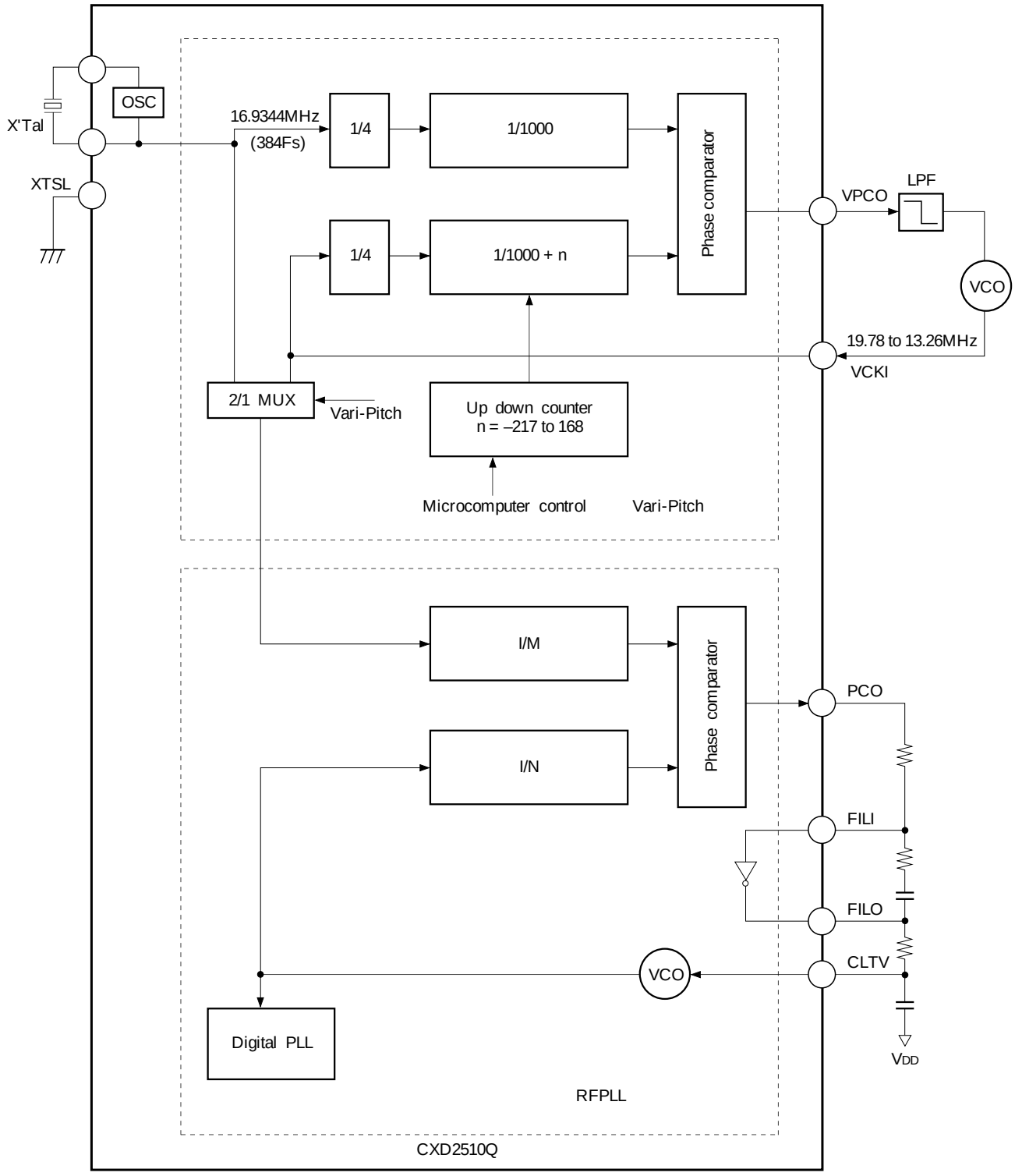
§3-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 3-1.
The CXD2510Q has a built-in three-stage PLL.

- The first-stage PLL regenerates the variable pitch.
  LPF and VCO are necessary as external parts.
  The minimum variable amount of the pitch is 0.1%. The output of this first-stage PLL is used as a reference for all clocks within the LSI. Input the XTAO output to the VCKI pin when variable pitch is not used.
- The second-stage PLL regenerates a high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock, and has a ±150kHz (normal state) or more capture range.
- The digital PLL has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off .
- High-frequency components such as 3T and 4T may contain deviations. In such a case, turning the secondary loop off yields better playability.
  However, in this case the capture range becomes 50kHz.

Block Diagram 3-1



§3-2. Frame Sync Protection

- In a CD player operating at normal speed, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to know which data is the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD2510Q, window protection and forward protection/backward protection have been adopted for frame sync protection. The adoption of these functions achieves very powerful frame sync protection.
  There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. In other words, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If frame sync cannot be detected for 13 frames or more, the window is released and the frame sync is resynchronized.
  In addition, immediately after the window is released and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window is released immediately.

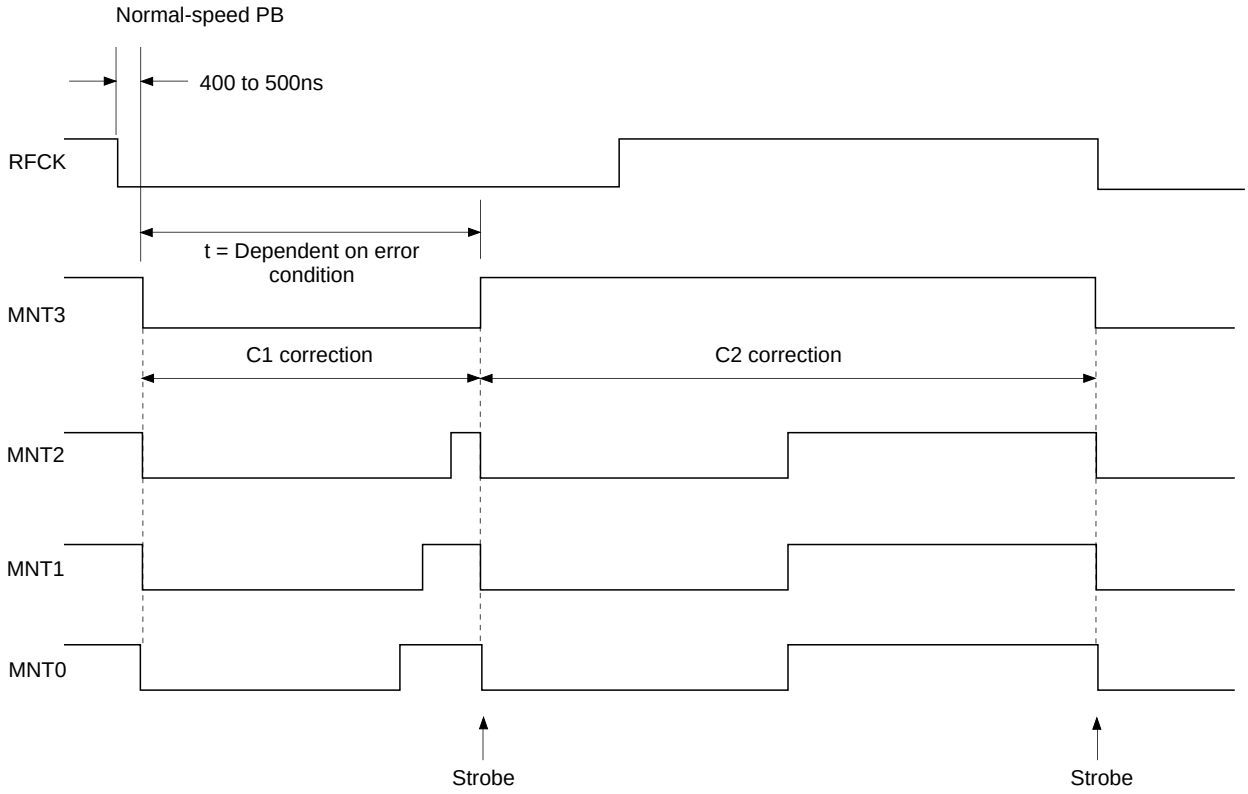
§3-3. Error correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD2510Q uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored outside the LSI.
  See the Table 3-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description
0	0	0	0	No C1 errors ; C1 pointer reset
0	0	0	1	One C1 error corrected ; C1 pointer reset
0	0	1	0	—
0	0	1	1	—
0	1	0	0	No C1 errors ; C1 pointer set
0	1	0	1	One C1 error corrected ; C1 pointer set
0	1	1	0	Two C1 errors corrected ; C1 pointer set
0	1	1	1	C1 correction impossible ; C1 pointer set
1	0	0	0	No C2 errors ; C2 pointer reset
1	0	0	1	One C2 error corrected ; C2 pointer reset
1	0	1	0	Two C2 errors corrected ; C2 pointer reset
1	0	1	1	Three C2 errors corrected ; C2 pointer reset
1	1	0	0	Four C2 errors corrected ; C2 pointer reset
1	1	0	1	—
1	1	1	0	C2 correction impossible ; C1 pointer copy
1	1	1	1	C2 correction impossible ; C2 pointer set

Table 3-2.

Timing Chart 3-3



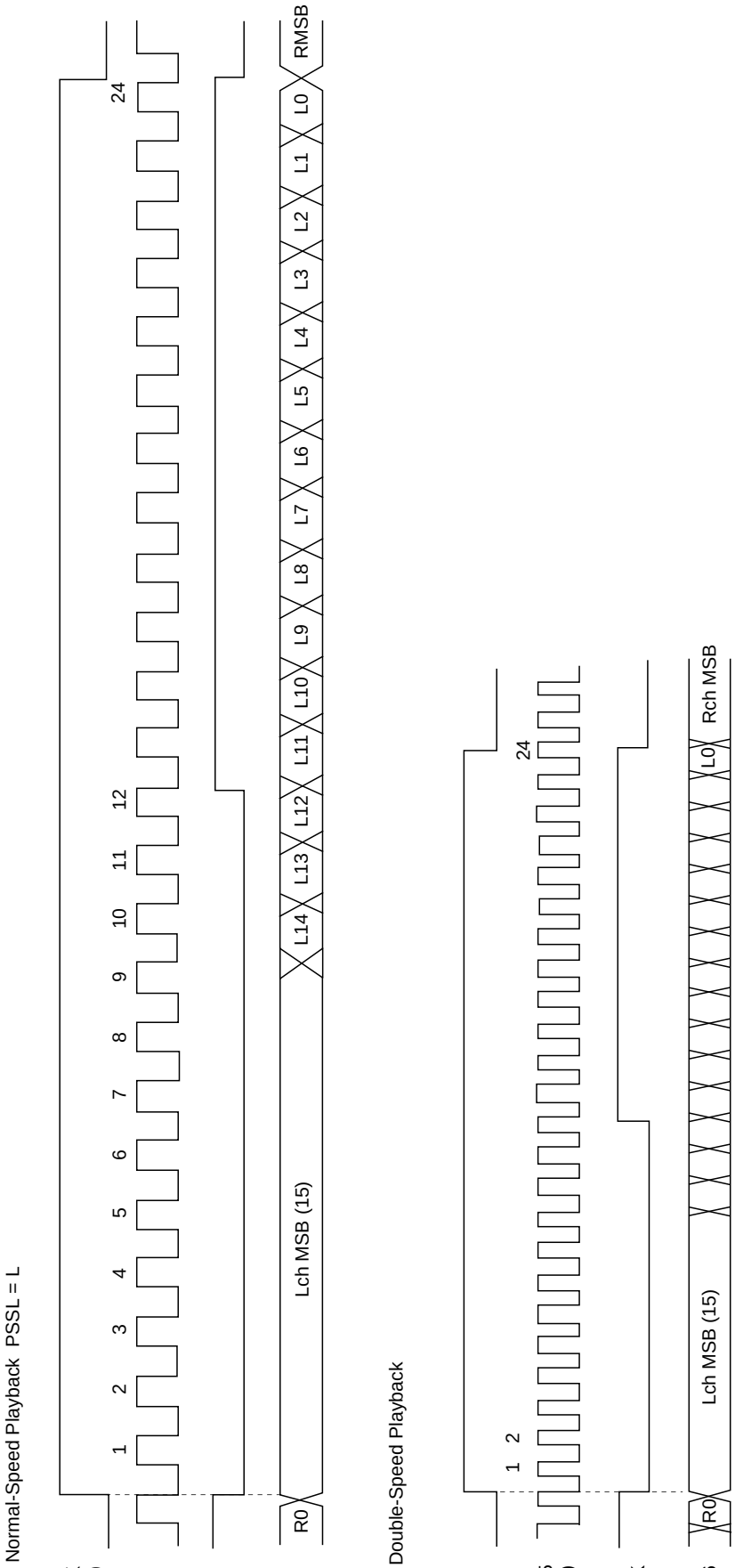
§3-4. DA Interface

- The CXD2510Q has two modes as DA interfaces.

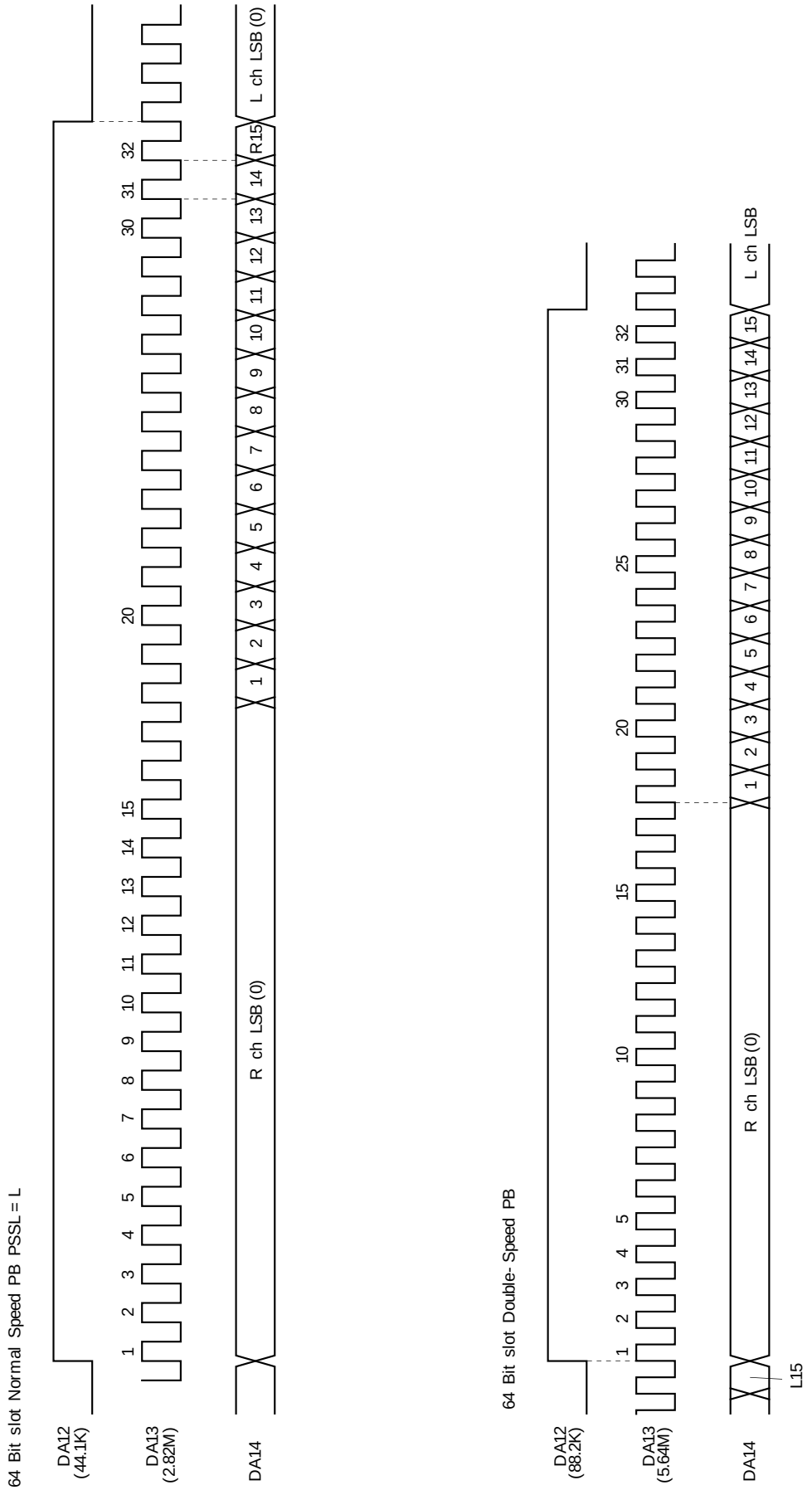
a) 48-bit slot interface
This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.
When LRCK is high, the data is for the left channel.

b) 64-bit slot interface
This interface includes 64 cycles of the bit clock within one LRCK cycle, and is LSB first.
When LRCK is low, the data is for the left channel.

Timing Chart 3-4



Timing Chart 3-5



§3-5. Digital Out

There are three digital out formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2510Q supports type 2 form 1.

In addition, regarding the clock accuracy of the channel status, level III is set automatically when the crystal clock is used and level II is variable pitch. In addition, Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bit 0 to 3).

DOUT is output when the crystal is 34MHz, the variable pitch is reset, and DSPB = 1. Therefore, set MD2 to 0 and turn DOUT off.

bit 0 to 3 -Sub Q control bits that matched twice with CRCOK

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

bit 0 to 3 – Sub Q control bits that matched twice with CRCOK

bit29 – Varipitch: 1 X'Tal: 0

Table 3-6.

§3-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1 track jump, 2N track jumps, and fine search are executed automatically.

SSP (servo signal processor LSI) is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the SSP, but can be sent to the CXD2510Q.

In addition, when using the auto sequence, connect the CPU, RF and SSP as shown in Fig. 3-7, and turn the A.SEQ of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is designed to prevent the transfer of erroneous data to the SSP when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built in as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See §1-2, $4X commands concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.
Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

Focus search up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 3-8. The auto focus is executed after focus search up, and the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

Connection diagram for using the auto sequencer (example)

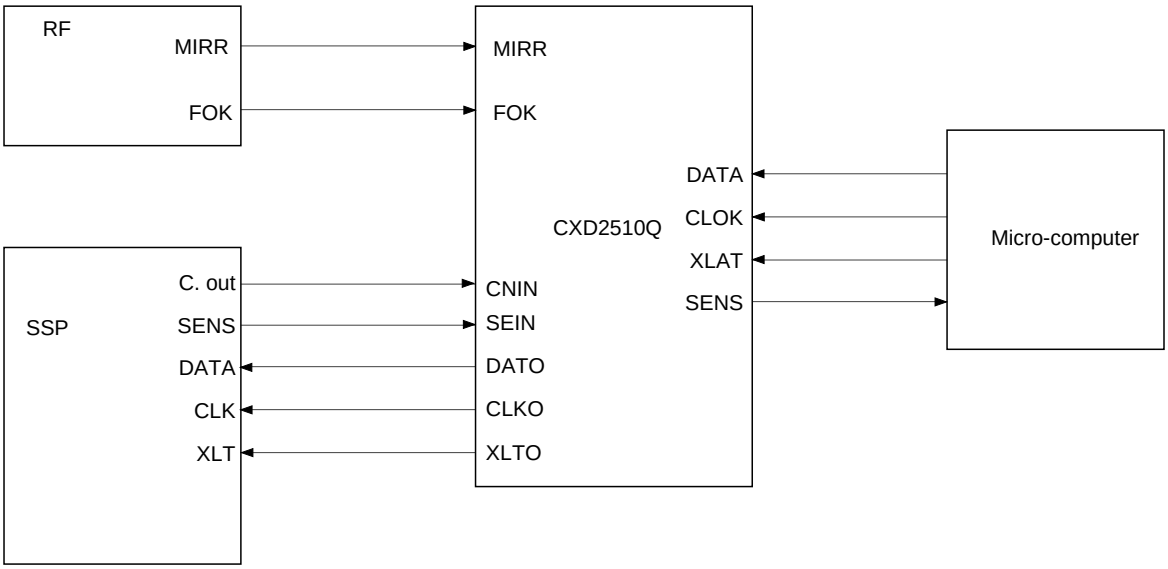


Fig. 3-7.

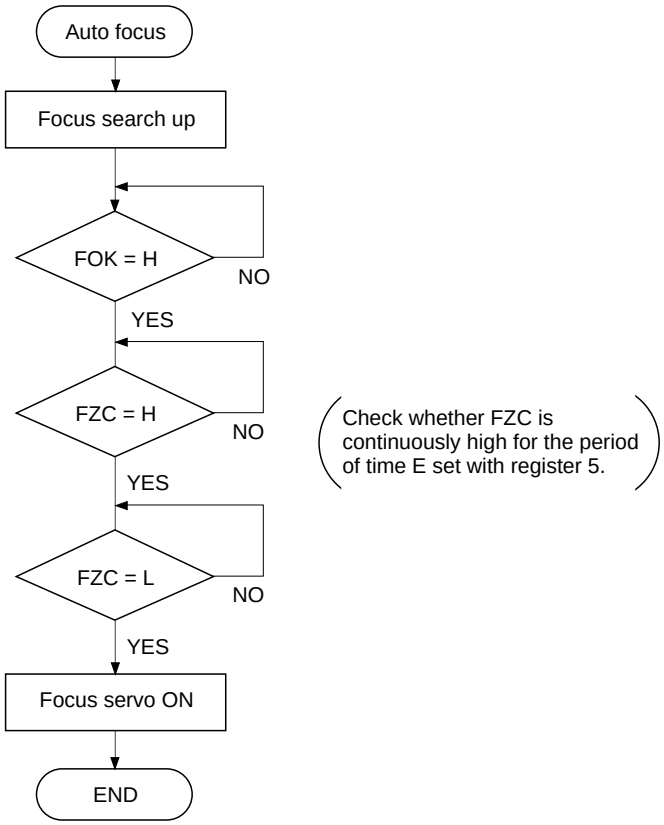


Fig. 3-8. (a) Auto Focus Flow Chart

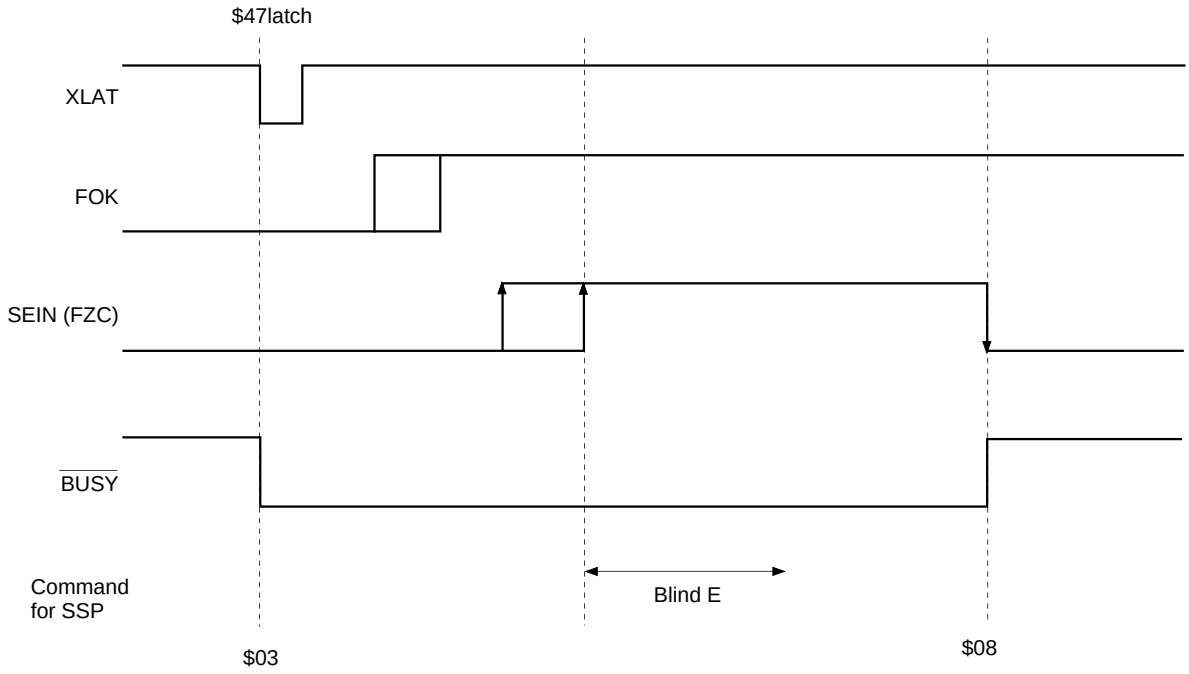


Fig. 3-8. (b) Auto Focus Timing Chart

(b) Track jump

1, 10, and 2N-track jumps are performed respectively. Always use this when focus, tracking, and sled servo are on. Note that tracking gain up and braking on ($17) should be sent beforehand because they are not performed.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 3-9. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 3-10. The principal difference between the 10-track jump and the 1-track jump is whether to kick the sled or not. In addition, after kicking the actuator, when 5 tracks have been counted through CNIN, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the CNIN cycle becoming longer than the overflow C set in register 5), the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 3-11. The track jump count "N" is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. CNIN is used for counting the number of jumps when N is less than 16, and MIRR is used when N is 16 or higher.

  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set in register 6.

- Fine search

  When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 3-12. The one difference from a 2N-track jump is that a higher precision is achieved by controlling the traverse speed. The track jump count is set in register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F in register 6 and overflow G in register 5. After N tracks have been counted through CNIN, the brake is applied to the actuator and sled. This is performed by turning the tracking servo for the actuator on, and by kicking the sled in the opposite direction. The cancel command $40 is sent from the CPU when track jump is terminated.

  Set overflow G to the speed required to slow up just before the track jump terminates. The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump. (Set the target track count N-α for the traverse monitor counter which is set in register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.)

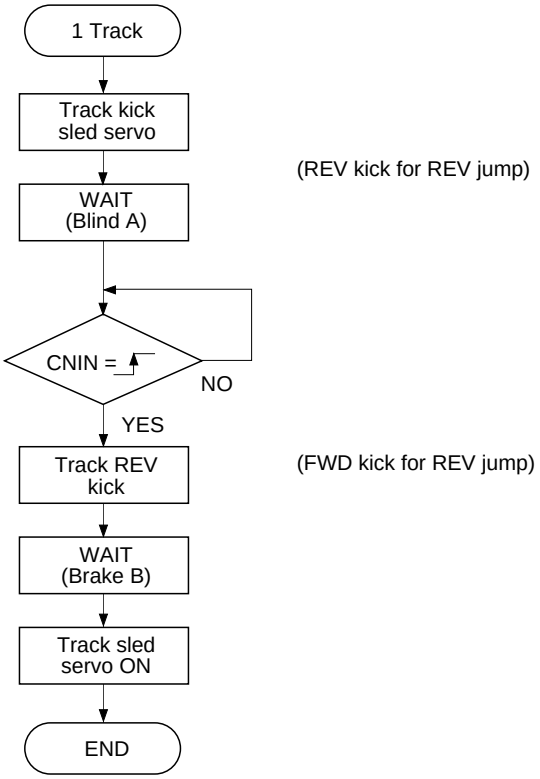


Fig. 3-9. (a) 1-Track Jump Flow Chart

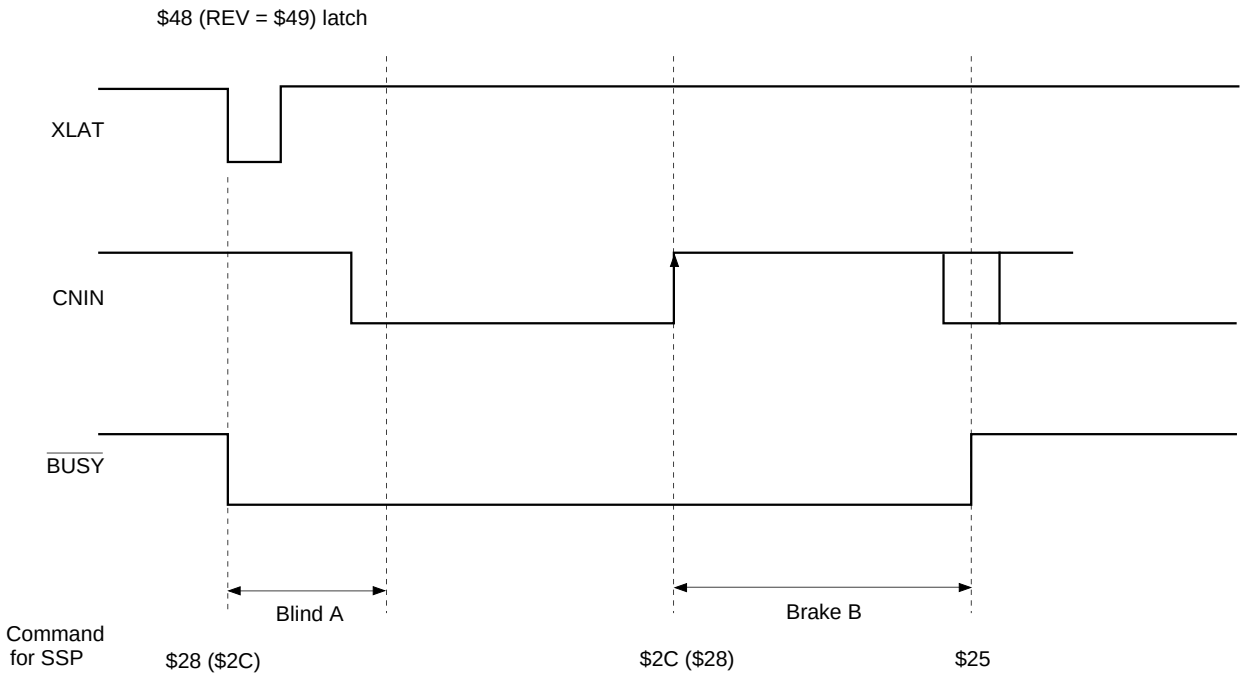


Fig. 3-9. (b) 1-Track Jump Timing Chart

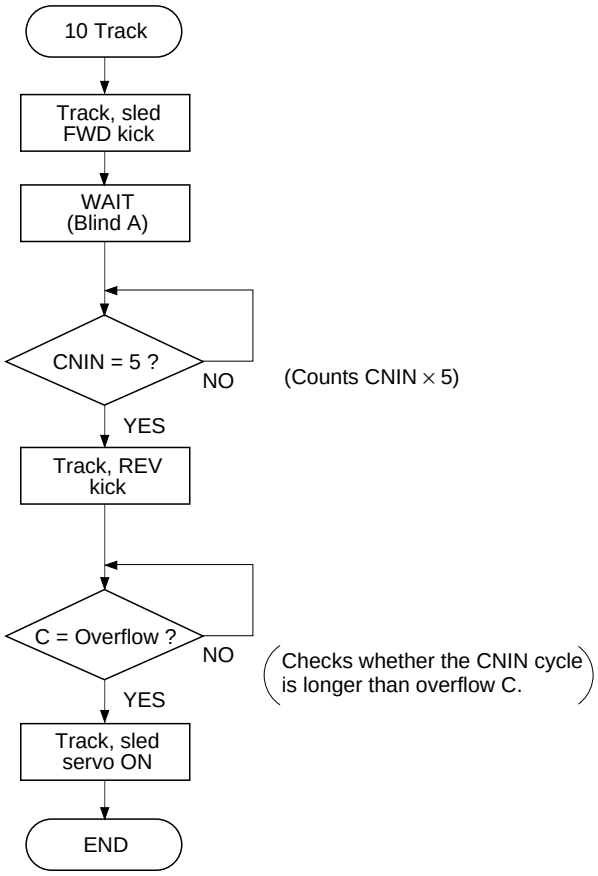


Fig. 3-10. (a) 10-Track Jump Flow Chart

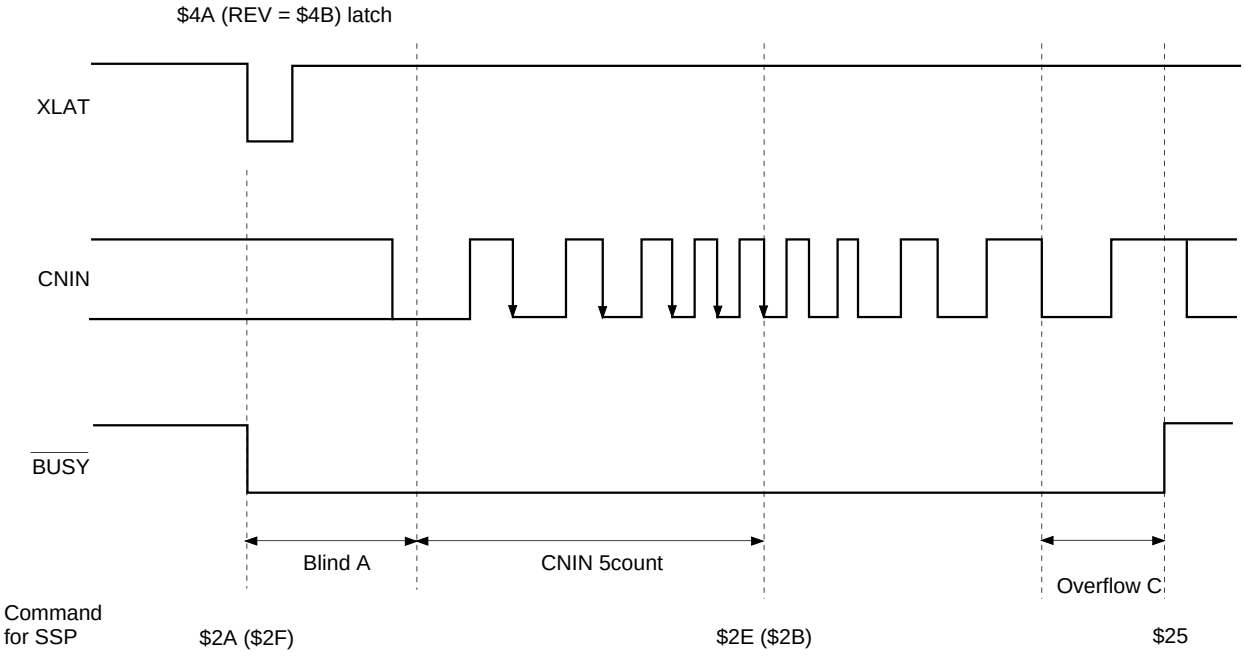


Fig. 3-10. (b) 10-Track Jump Timing Chart

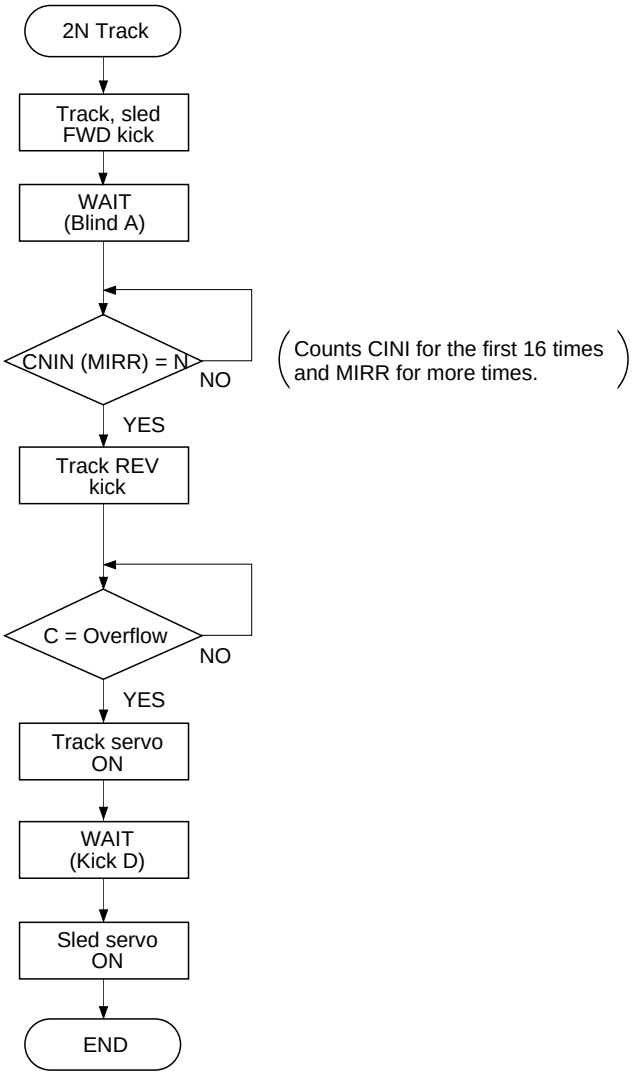


Fig. 3-11. (a) 2N-Track Jump Flow Chart

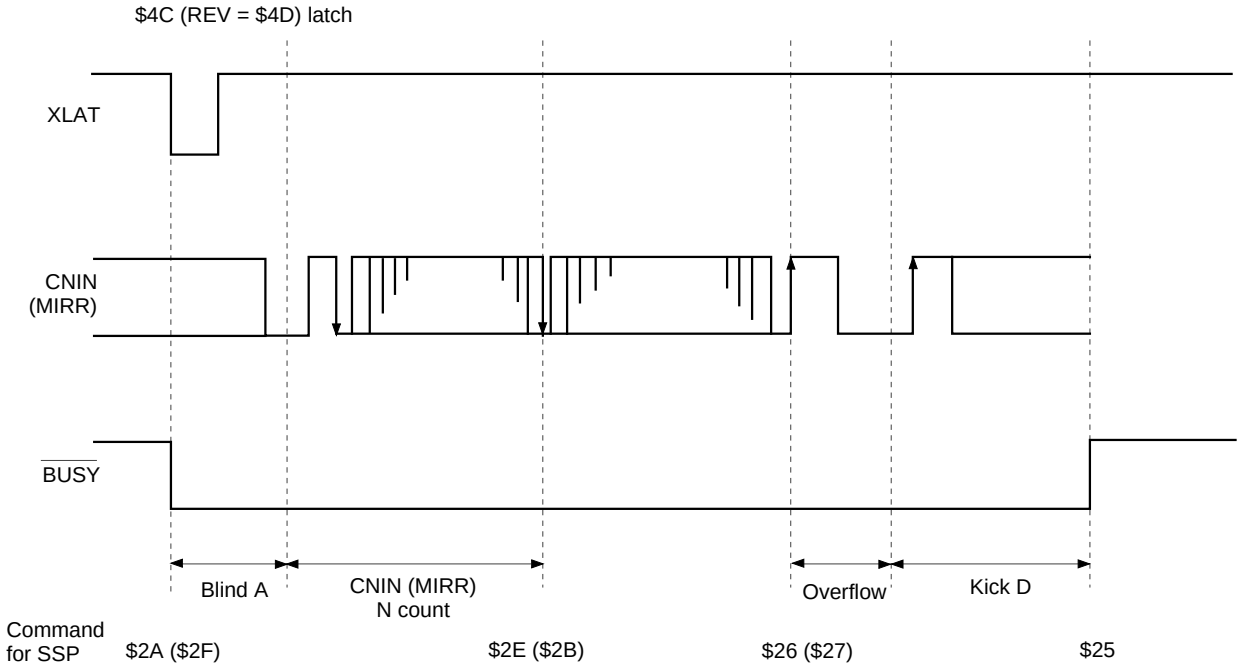


Fig. 3-11. (b) 2N-Track Jump Timing Chart

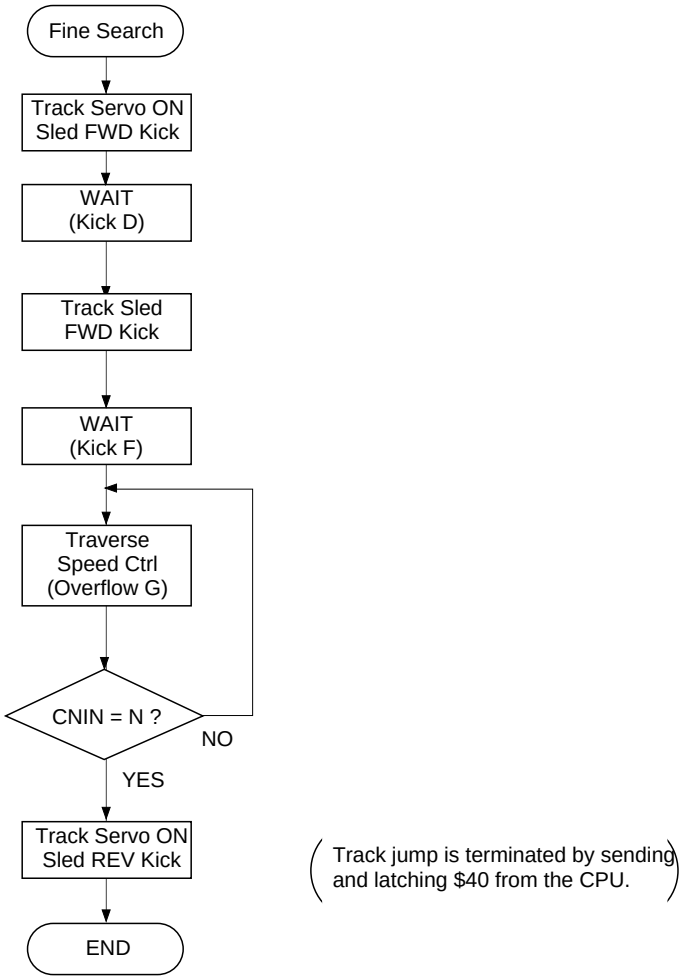


Fig. 3-12. (a) Fine Search Flow Chart

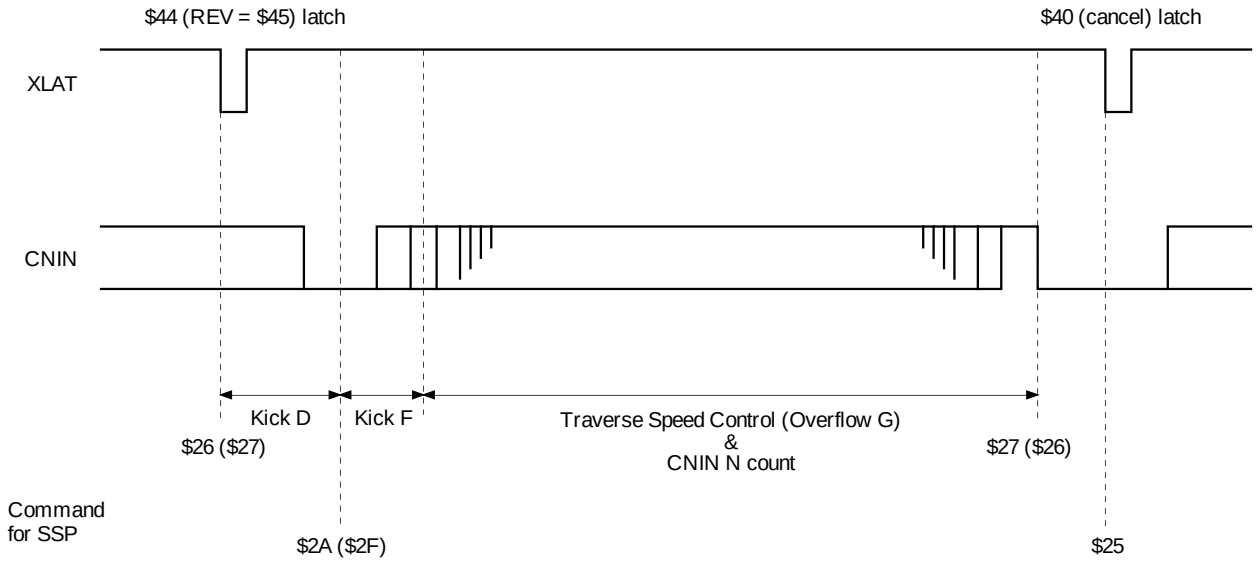
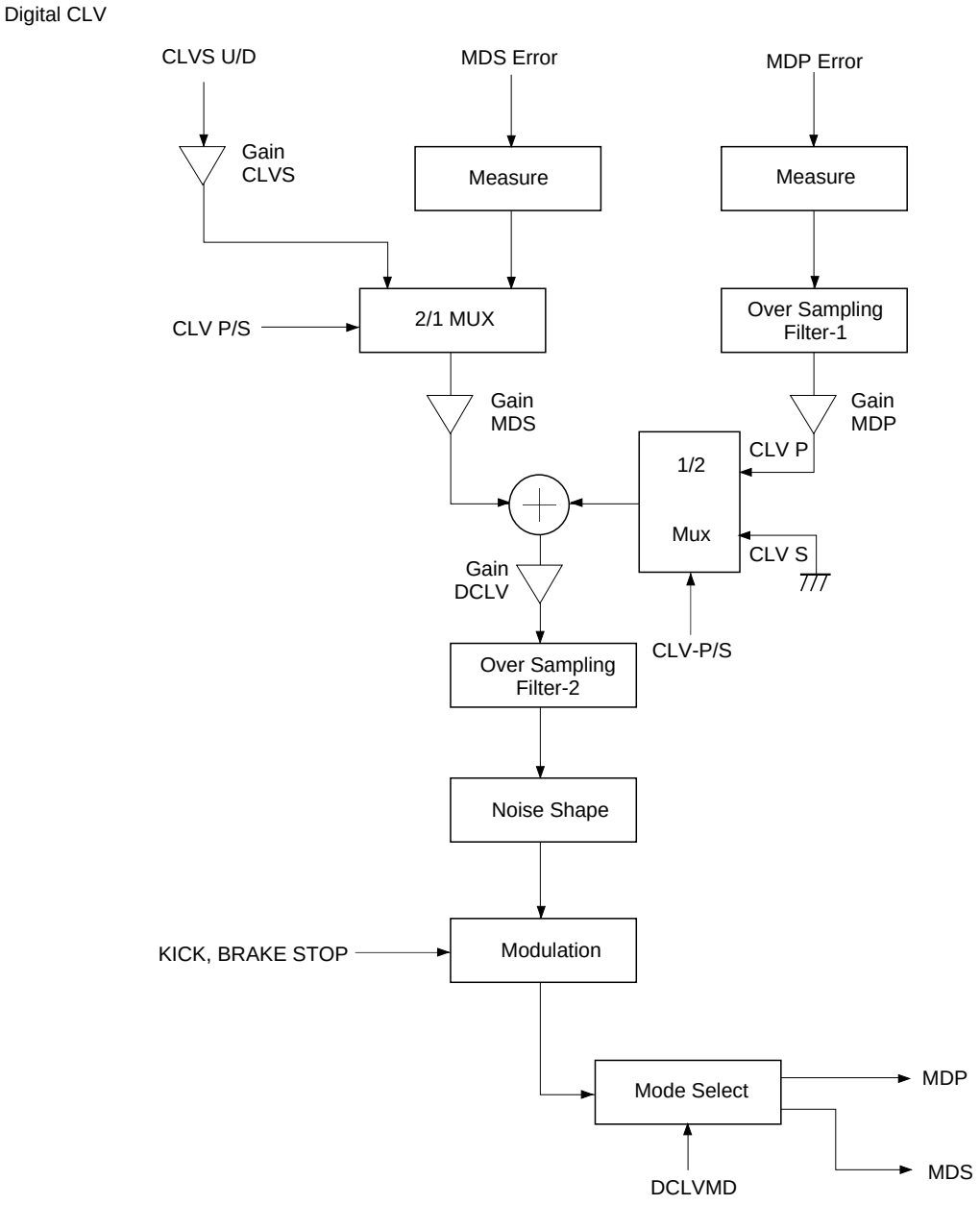


Fig. 3-12. (b) Fine Search Timing Chart

§3-7. Digital CLV

Fig. 3-13 shows the block diagram. Digital CLV makes PWM output in CLVS, CLVP and other modes with the MDS error or MDP error signal sampling frequency increased to 130kHz during normal-speed operation. In addition, the digital spindle servo can set the gain.



CLVS U/D: Up/down signal from the CLV-S servo.
MDS error: Frequency error for CLV-P servo.
MDP error: Phase error for CLV-P servo.

Fig. 3-13. Block Diagram

§3-8. Asymmetry Compensation

Fig. 3-14 shows the block diagram and circuit example.

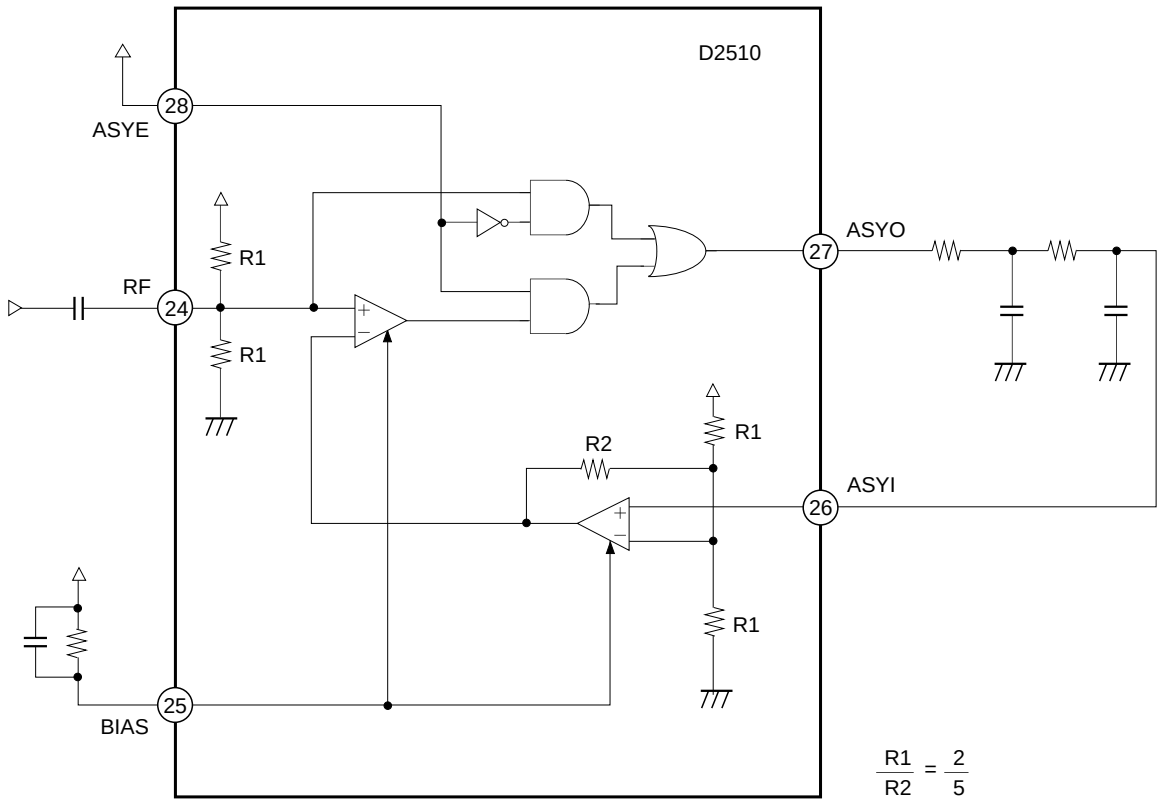


Fig. 3-14. Example of an Asymmetry Compensation Application Circuit

§3-9. Playback Speed

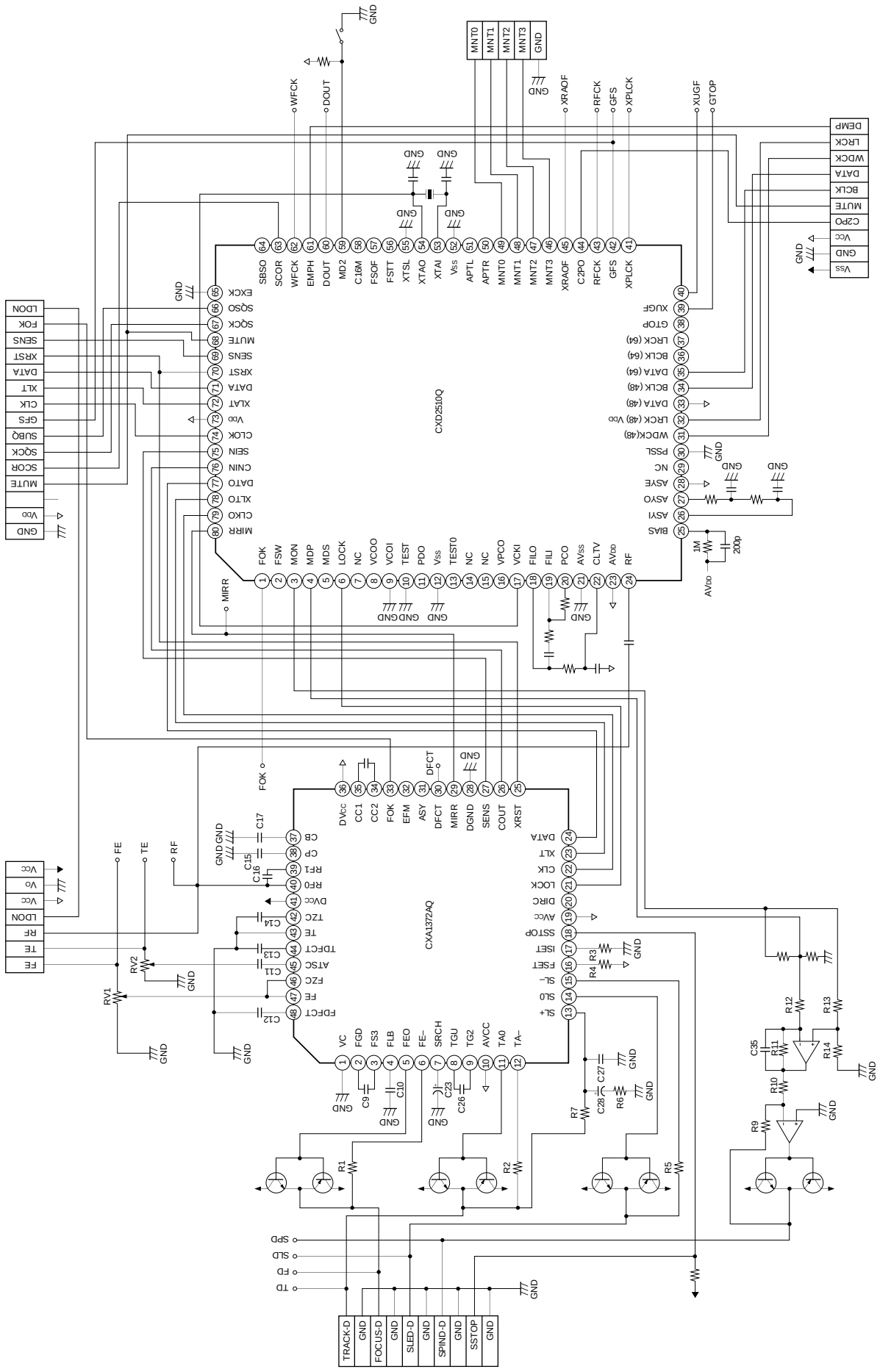
In the CXD2510Q, the following playback modes can be selected through different combinations of the crystal, XTSL pin, double-speed command (DSPB), VCO selection command (VCOSEL) and command transfer rate selector (ASHS). Also, the minimum operating voltage changes according to the playback mode. (See the Recommended Operating Conditions.)

Playback modes

Mode	X'tal	XTSL	DSPB	VCOSEL	ASHS	Playback speed	Error correction
1	768Fs	1	0	0/1	0	× 1	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	× 2	C1: double; C2: double
3	768Fs	0	0	1	1	× 2	C1: double; C2: quadruple
4	768Fs	0	1	1	1	× 4	C1: double; C2: double
5	384Fs	0	0	0/1	0	× 1	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	× 2	C1: double; C2: double
7	384Fs	1	1	0/1	0	× 1	C1: double; C2: double

However, Fs = 44.1kHz.

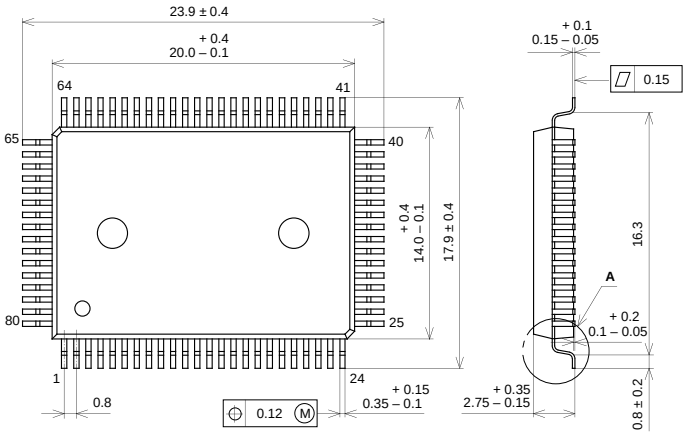
Application Circuit

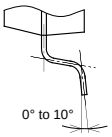


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





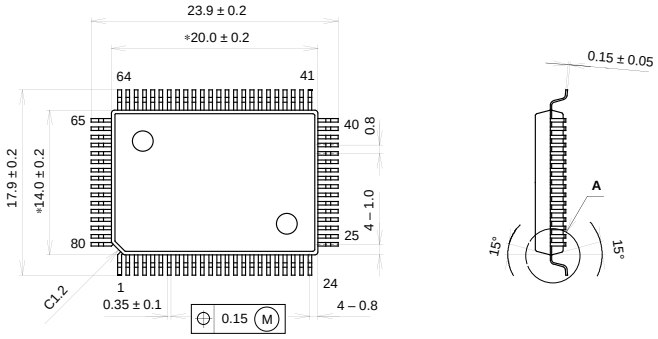
DETAIL **A**

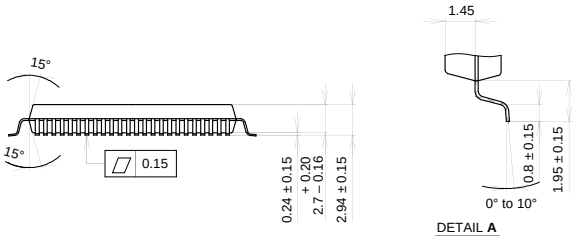
SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g

QFP 80PIN (PLASTIC)





DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	QFP-80P-L051
EIAJ CODE	∗QFP080-P-1420-AH
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.6g