SONY

CXG1014N

1.5 GHz Low Noise Amplifier/Down Conversion Mixer

Description

The CXG1014N is a low noise amplifier/down conversion mixer MMIC, designed using the Sony's GaAs J-FET process.

Features

- Low noise
  NF=1.85 dB (Typ.) at 1.49 GHz
  (low noise amplifier)
- Low distortion
  Input IP3=+2 dBm (Typ.) at 1.49 GHz
  (mixer)
- Low LO input power operation –15 dBm
- Single 3.0 V power supply operation
- 16-pin SSOP package

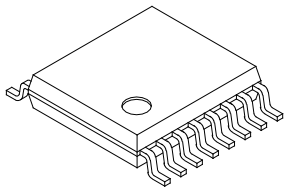
Applications

1.5 GHz Japan digital cellular telephones

Structure

GaAs J-FET MMIC

16 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Power dissipation	P_D	150	mW
• Current consumption			
I_{DD} (low noise amplifier)		20	mA
I_{DD} (LO amplifier)		10	mA
I_{DD} (mixer, IF amplifier)		20	mA
• Input power	P_{IN}	+5	dBm

Operating Condition

Supply voltage	3.0	V

E97408-TE

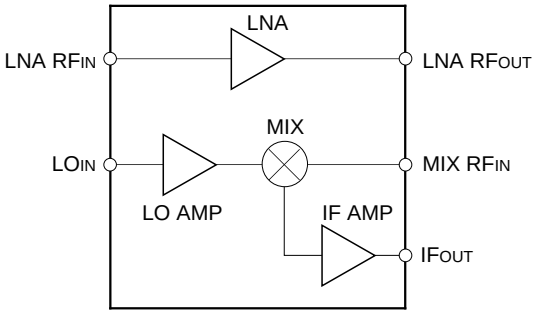
Electrical Characteristics

V_{DD}=3.0 V, f_{RF}=1.49 GHz, f_{LO}=1.62 GHz, P_{LO}=–15 dBm, when 50 Ω I/O matching; unless otherwise specified

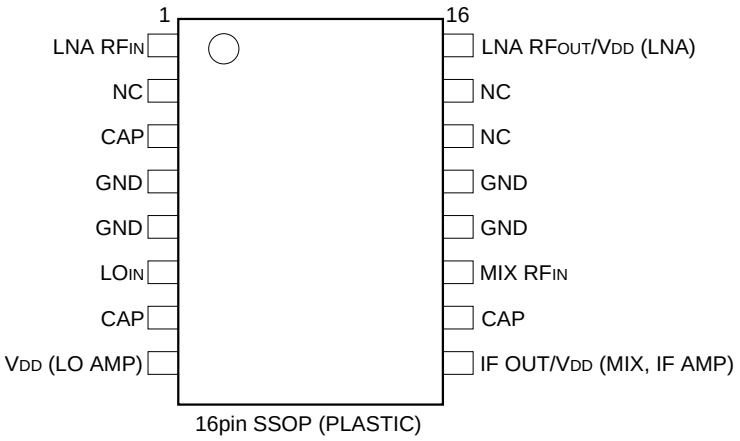
(Ta=25 °C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement condition
Low noise amplifier	Current consumption	I_{DD}	—	2.2	3.0	mA	When no signal
	Power gain	G_P	14	16	18	dB	
	Noise figure	NF	—	1.85	2.6	dB	
	Input IP3	IIP3	–7.5	–3.5	—	dBm	
	Isolation	I_{SO}	30	35	—	dB	
Mixer	Current consumption	I_{DD}	—	3.8	5.5	mA	When no signal
	Conversion gain	G_C	6	8	10	dB	
	Noise figure	NF	—	8.5	10.5	dB	
	Input IP3	IIP3	–2	2	—	dBm	
	LO to RF leak level	P_{LK}	—	–17	–12	dBm	

Block Diagram

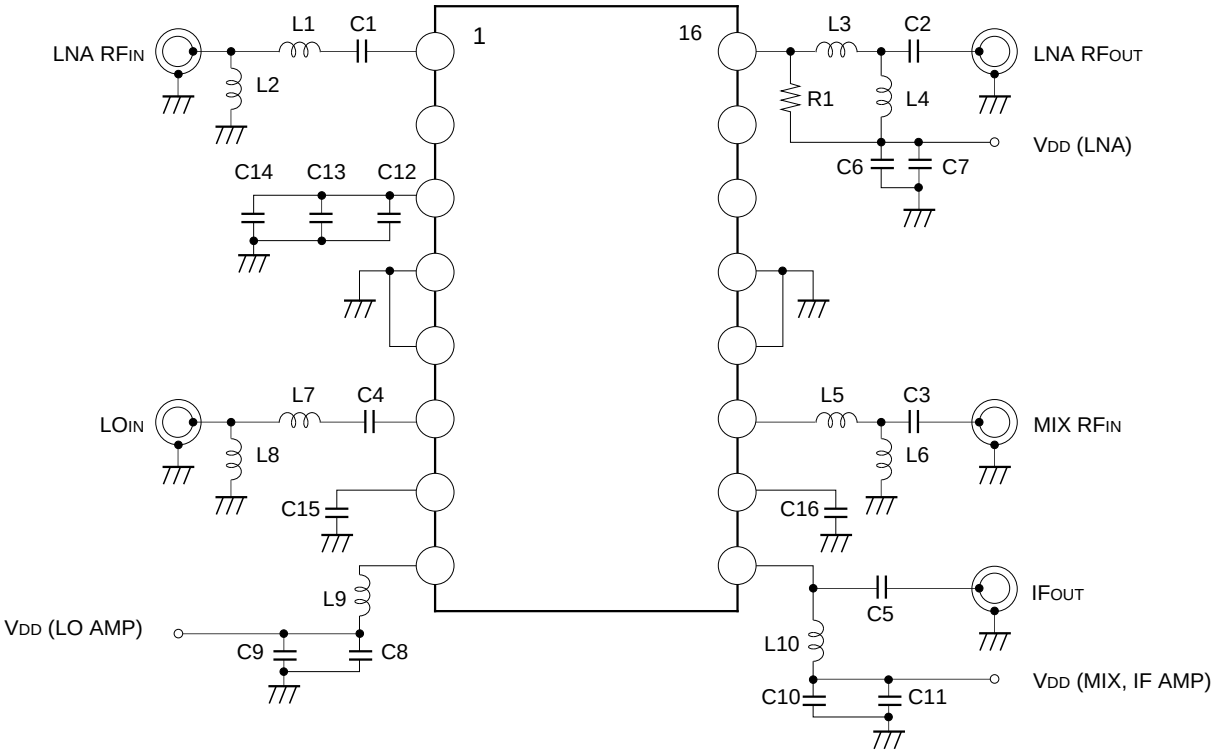


Pin Configuration



16pin SSOP (PLASTIC)

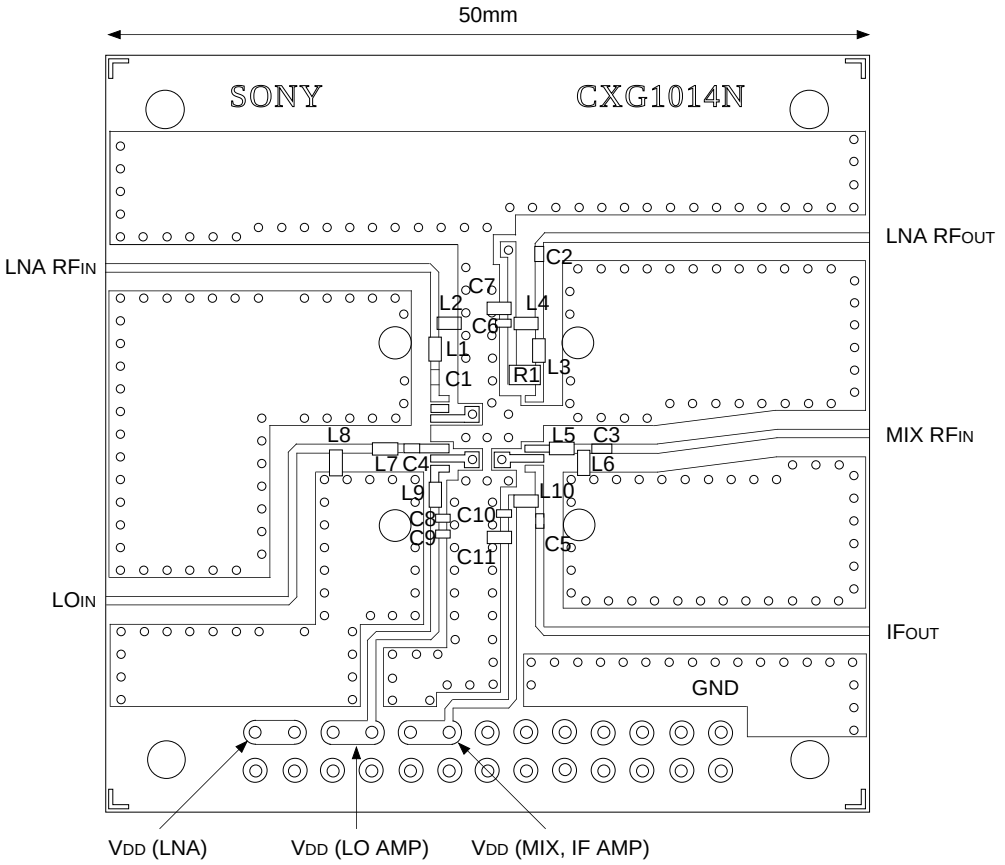
Recommended Circuit



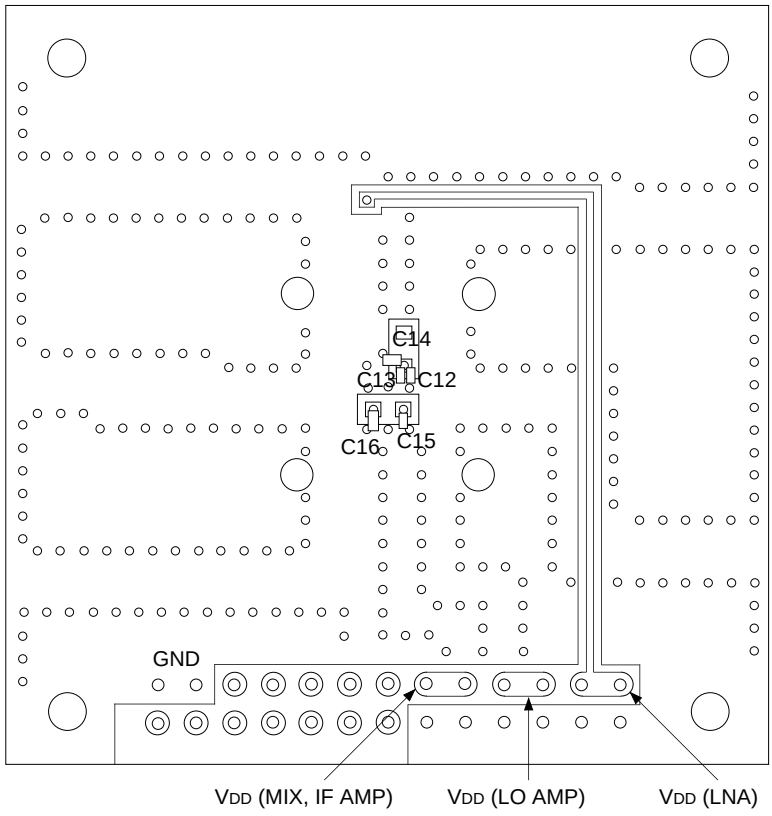
L1	6.8 nH	L10	150 nH	C9	10 nF
L2	4.7 nH	C1	100 pF	C10	1000 pF
L3	4.7 nH	C2	100 pF	C11	1 µF
L4	3.3 nH	C3	2 pF	C12	100 pF
L5	10 nH	C4	100 pF	C13	1000 pF
L6	4.7 nH	C5	10 pF	C14	1 µF
L7	5.6 nH	C6	1000 pF	C15	1000 pF
L8	3.3 nH	C7	1 µF	C16	1 µF
L9	10 nH	C8	1000 pF	R1	1 kΩ

Recommended Evaluation Board

Front



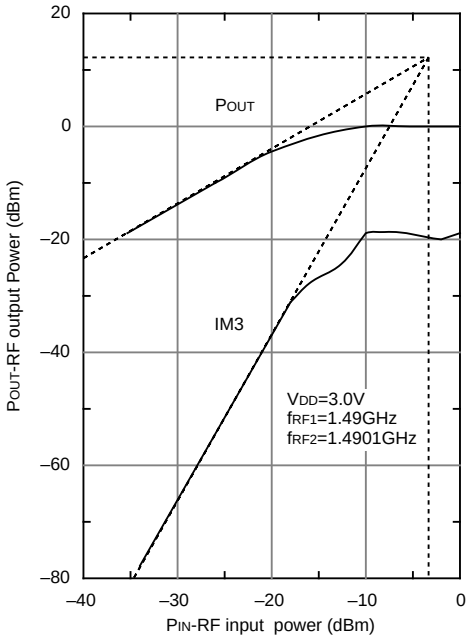
Back



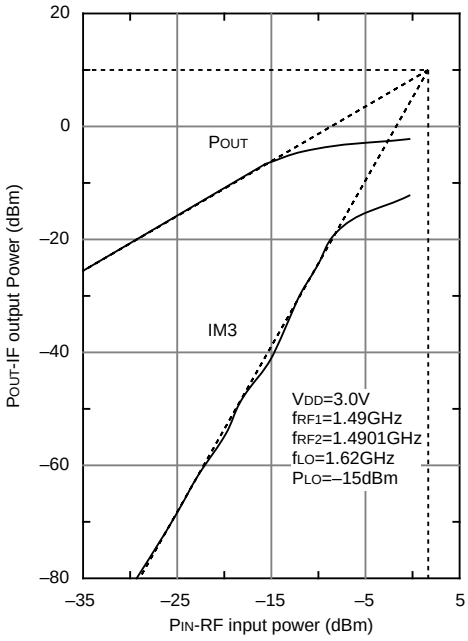
Glass fabric-base epoxy 4-layer board (2 × 0.3 mm thickness)
GND for the 2nd and 3rd layers.

Example of Representative Characteristics (Ta=25 °C)

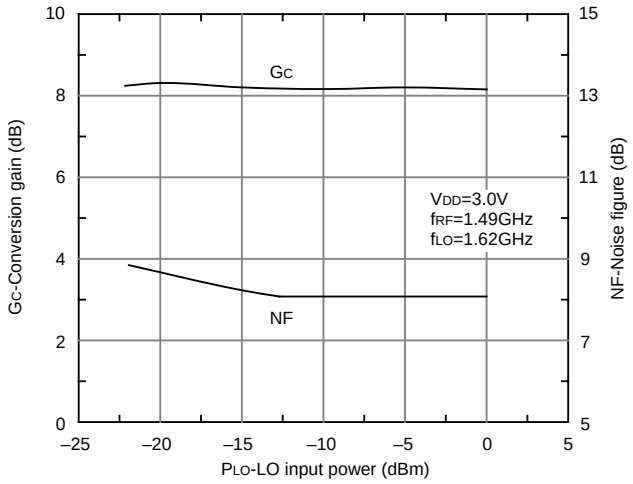
LNA block POUT, IM3 vs. PIN



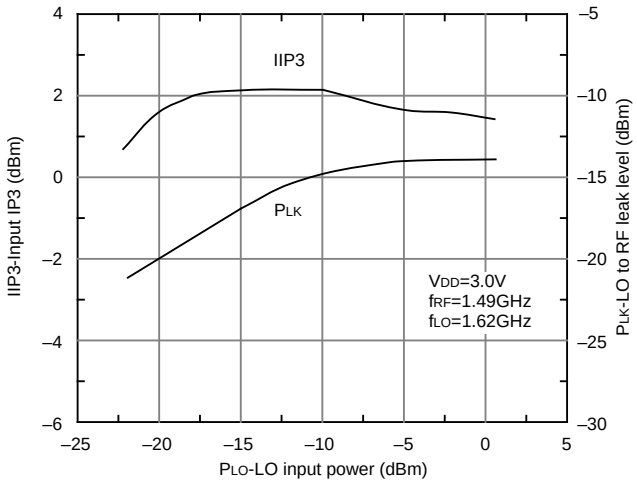
MIX block POUT, IM3 vs. PIN



MIX block GC, NF vs. PLO

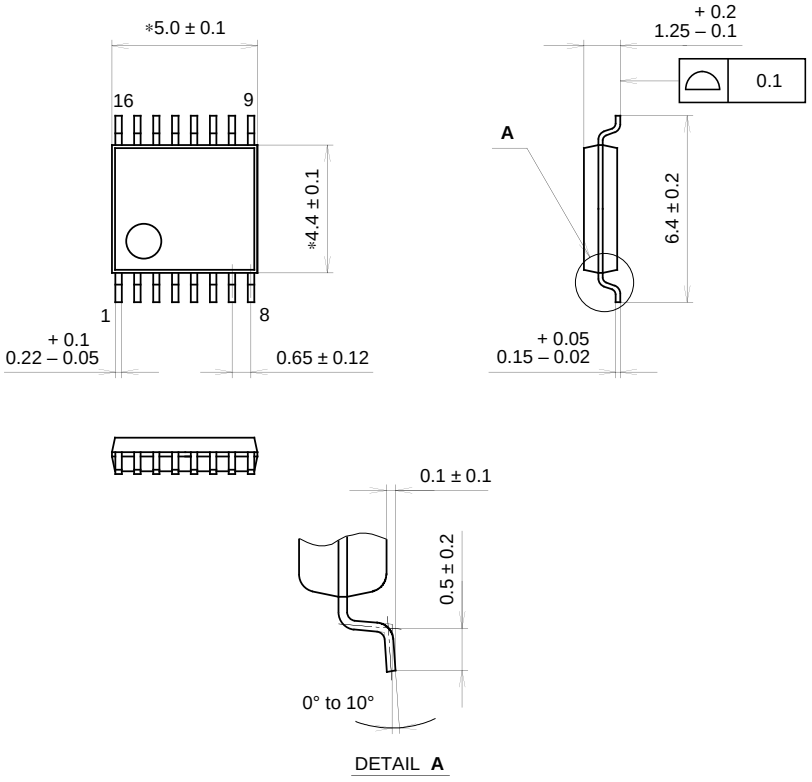


MIX block IIP3, PLK vs. PLO



Package Outline Unit : mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).