SONY

CXG1030N

Power Amplifier for PHS

Description

The CXG1030N is a power amplifier for PHS. This IC is designed using the Sony's GaAs J-FET process and operates at a single power supply.

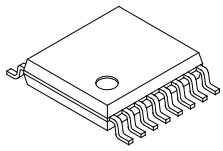
Features

- Output power 21 dBm
- Positive power supply 3.0 V
- Low current consumption 170 mA
- High power gain 39 dB Typ.
- Small mold package 16-pin SSOP

Structure

GaAs J-FET MMIC

16 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	Vgs0	1.5	V
• Drain current	I_{DD}	500	mA
• Power dissipation	P_D	3	W
• Channel temperature	Tch	175	°C
• Operating temperature	Top	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Electrical Characteristics

V_{DD}=3.0 V, V_{CTL}=2.0 V, f=1.90 GHz (Ta=25 °C)

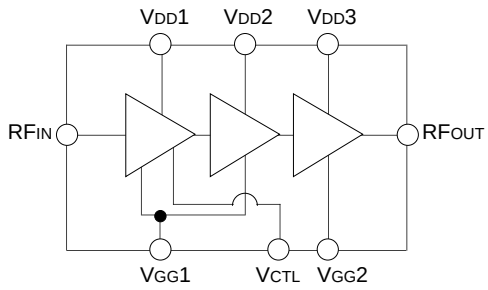
Item	Symbol	Min.	Typ.	Max.	Unit
*1 Current consumption	I_{DD}		170		mA
*1 Gate voltage adjustment value	V_{GG2}	0	0.4	0.8	V
Output power	P_{OUT}	21			dBm
*2 Power gain	G_P	36	39		dB
*2 Adjacent channel leak power ratio (600 kHz ±100 kHz)	ACPR600		–59	–54	dBc

*1 Values where $V_{GG}1$ and $V_{GG}2$ are adjusted so that I_{DD} becomes 170 mA when 21.0 dBm is output.

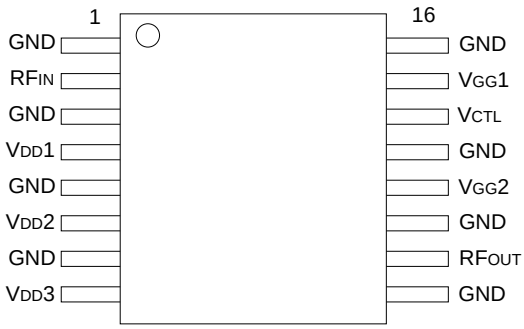
*2 When 21.0 dBm is output.

E96706-TE

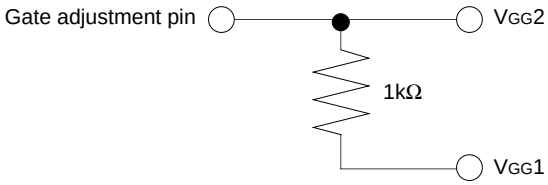
Block Diagram



Pin Configuration



Gate Bias Circuit



Recommended Current Adjustment Method

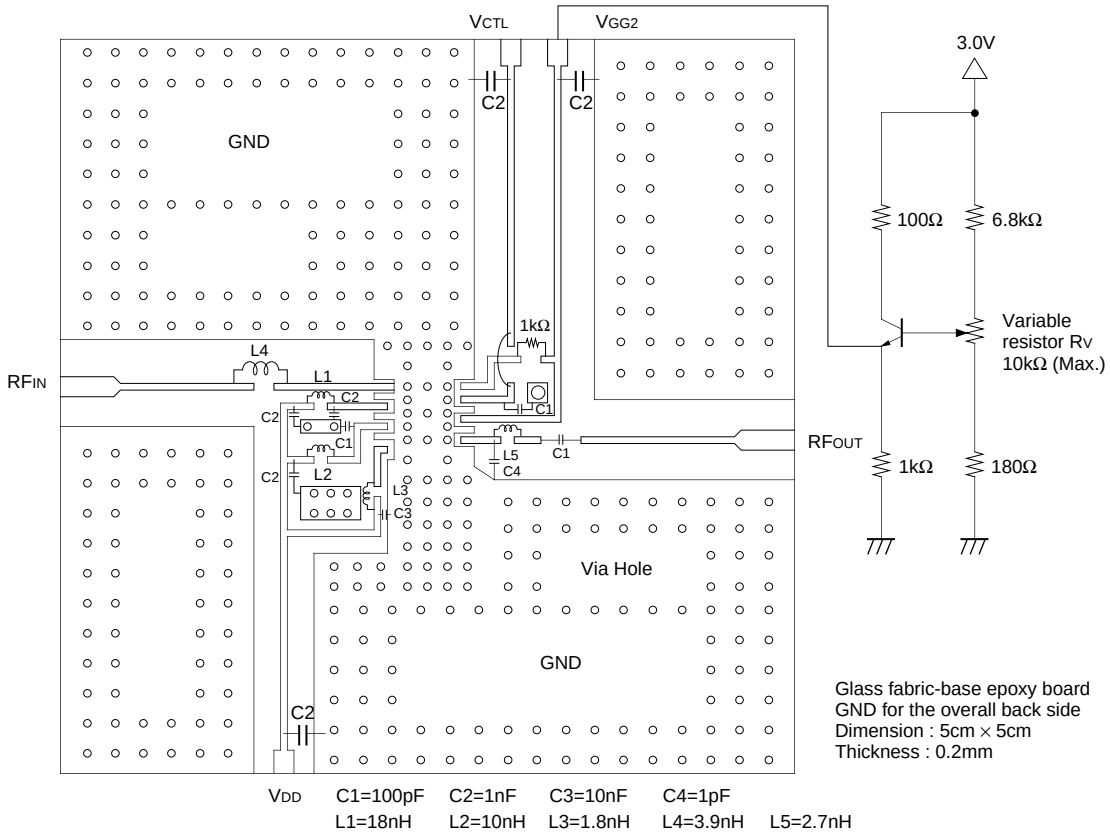
(1) $V_{GG}2/P_{IN}$ separate adjustment

($V_{GG}2$ adjustment 1)	(P_{IN} adjustment 1)	($V_{GG}2$ adjustment 2)	(P_{IN} adjustment 2)
When the RF input (P_{IN}) is off, the current consumption (I_{DD}) is adjusted to 170 mA.	The output power (P_{OUT}) is adjusted to 21.0 dBm.	The current consumption (I_{DD}) is finely adjusted to 170 mA.	The output power (P_{OUT}) is finely adjusted to 21.0 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	I_{DD}=170±20 mA P_{OUT}=21.0 dBm	I_{DD}=170 mA P_{OUT}=21.0±0.2 dBm	I_{DD}=170±5 mA P_{OUT}=21.0 dBm

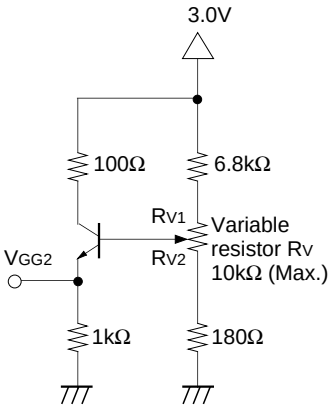
(2) Simple adjustment

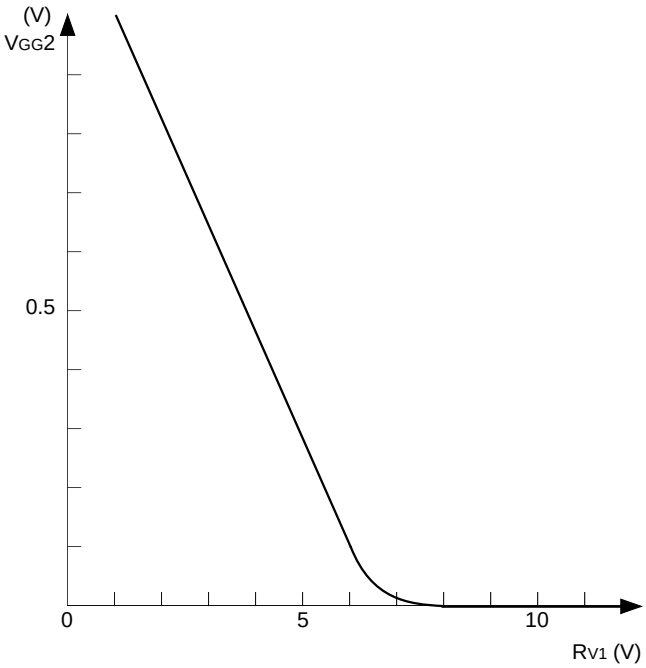
(I_{DD} read)	($V_{GG}2$ setting)	(P_{IN} adjustment)
When the RF input (P_{IN}) is off, the gate voltage ($V_{GG}2$) is set to 0.4 V and I_{DD} is read.	The formula*1 where $V_{GG}2=f(I_{DD}: V_{GG}2=0.4\ V)$ is used to set $V_{GG}2$.	The output power (P_{OUT}) is adjusted to 21.0 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	*1 e.g. $V_{GG}2=a-b\times I_{DD}$	I_{DD}=170±5 mA P_{OUT}=21.0 dBm

Recommended Evaluation Circuit



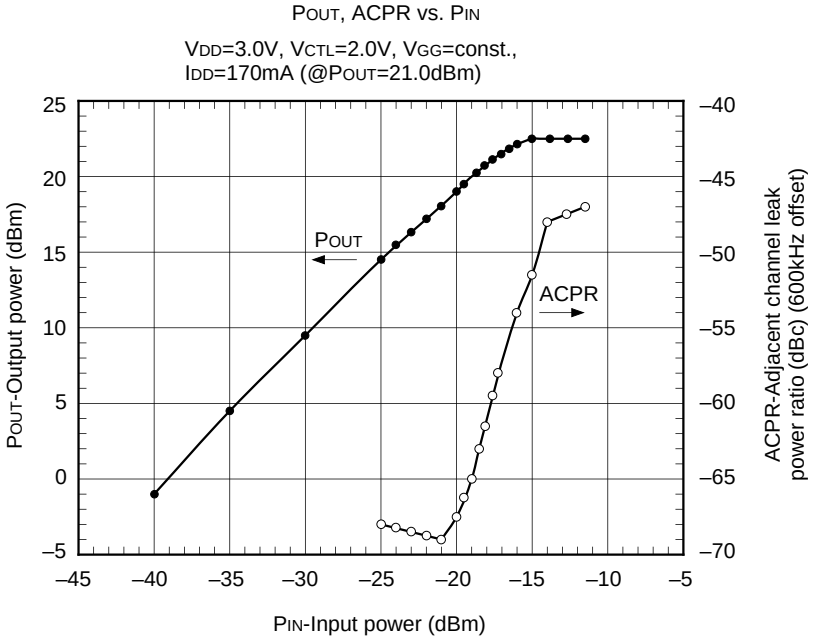
Recommended Gate Bias Circuit and Circuit Characteristics

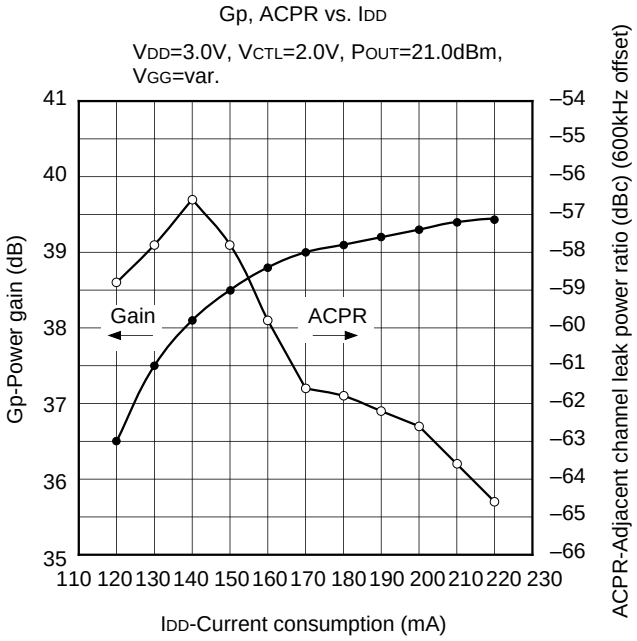


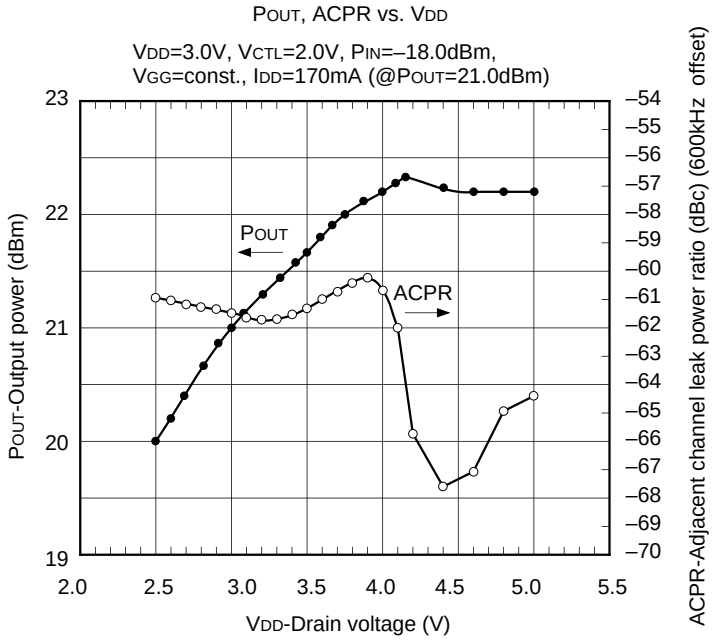


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (Ta=25 °C)

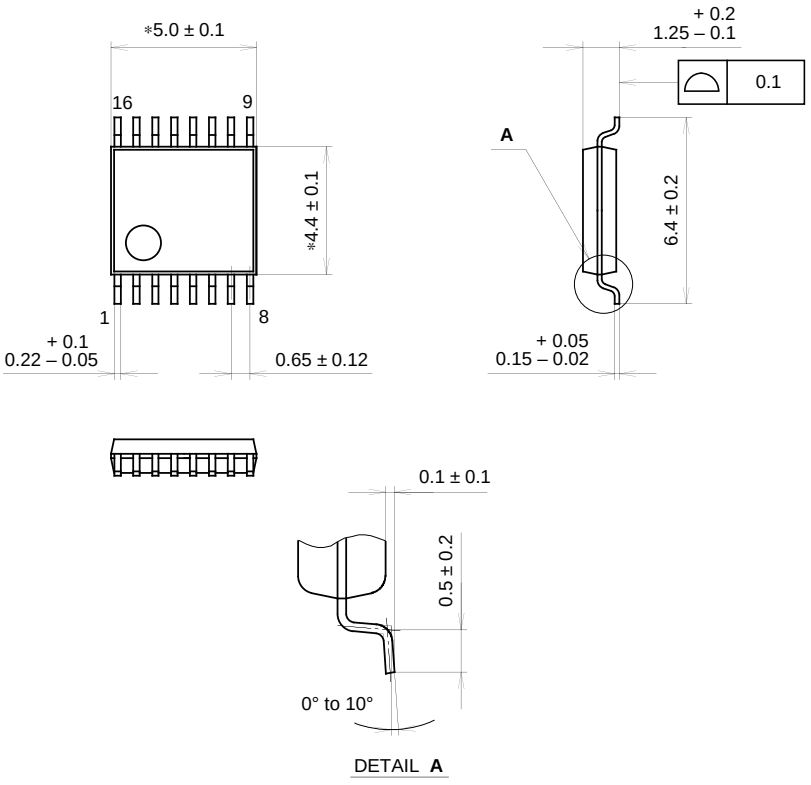






Package Outline Unit : mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

: PALLADIUM PLATING
This product uses PdPPF
(Palladium Pre-Plated Lead Frame).

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g