SONY

Switchable Step Capacitor

CXG1407XR

Description

The CXG1407XR can be selected four kinds of built-in capacitor (1 to 8 pF), or two path.
Sony JPHEMT GaAs process is utilized for low insertion loss, high linearity and high Q Factor capacitance with high accuracy.
(Applications: Antenna tuning, i.e Felica characteristics)

Features

- ◆Low insertion loss (internal switch)
- ◆Low voltage drive: 2.4 to 3.3 V
- ◆High Q Factor, high accuracy capacitance
- ◆Robustness against ESD
- ◆Small package: 12-pin XQFN (2.0 mm × 2.0 mm × 0.4 mm Max.)
- ◆Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC

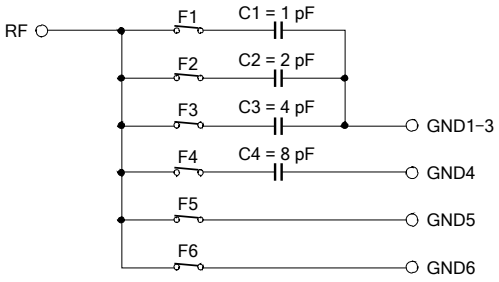
Absolute Maximum Ratings

Input voltage Max.	Vctl	+4	V (Ta = 25 °C)
Input voltage Min.	Vctl	–0.2	V (Ta = 25 °C)
Maximum input.		35	dBm (Ta = 25 °C)
Operating temperature		–30 to +90	°C
Storage temperature		–65 to +150	°C

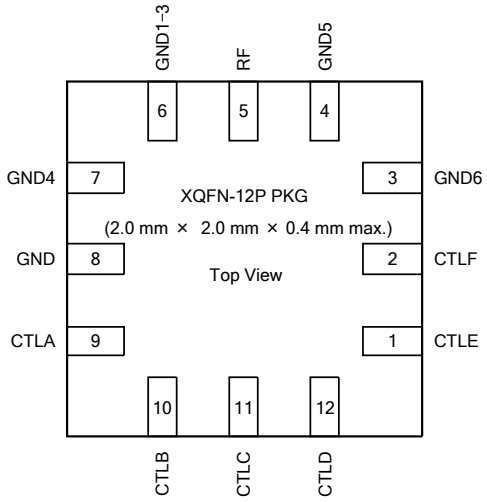
This IC is ESD sensitive device. Special handling precautions are required.

E11731D31

Block Diagram



Pin Configuration



Truth Table

CTLA	CTLB	CTLC	CTLD	CTLE	CTLF	F1	F2	F3	F4	F5	F6
L	—	—	—	—	—	OFF	—	—	—	—	—
H	—	—	—	—	—	ON	—	—	—	—	—
—	L	—	—	—	—	—	OFF	—	—	—	—
—	H	—	—	—	—	—	ON	—	—	—	—
—	—	L	—	—	—	—	—	OFF	—	—	—
—	—	H	—	—	—	—	—	ON	—	—	—
—	—	—	L	—	—	—	—	—	OFF	—	—
—	—	—	H	—	—	—	—	—	ON	—	—
—	—	—	—	L	—	—	—	—	—	OFF	—
—	—	—	—	H	—	—	—	—	—	ON	—
—	—	—	—	—	L	—	—	—	—	—	OFF
—	—	—	—	—	H	—	—	—	—	—	ON

Note) 1. [—] : Don't Care
2. It is prohibited that all control inputs are L.

DC Bias Condition

(Temperature = –30 to +90 °C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.4	2.8	3.3	V
Vctl (L)	0	—	0.3	

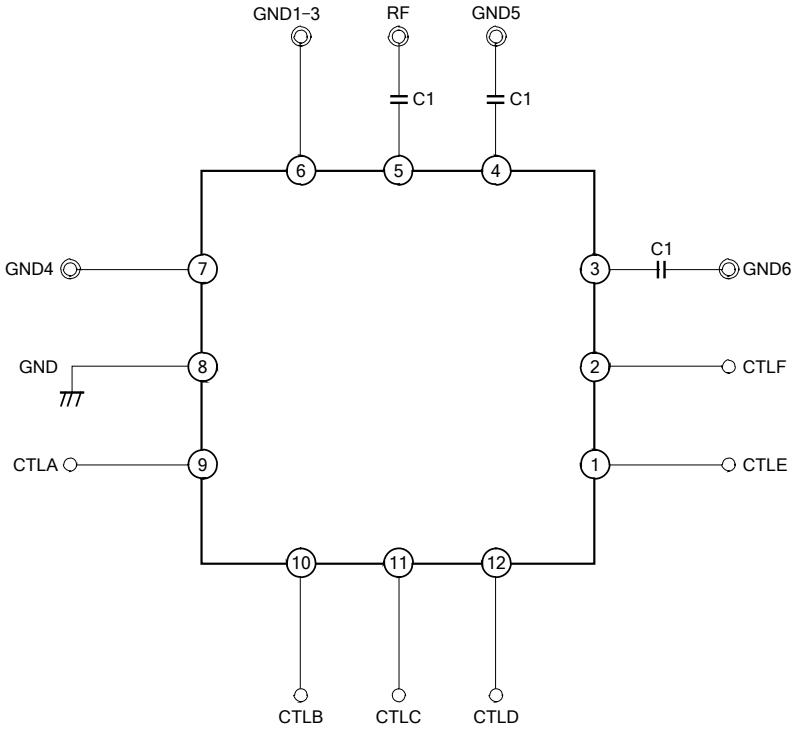
Electrical Characteristics

(Ta = 25 °C, V_{ctl} = 2.4 to 3.3 V/0 V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Transmission perfomance	S21	RF-GND1	*1	—	36.5	39.5	dB
			*2	—	4.9	5.7	
		RF-GND2	*1	—	32.6	35.6	
			*2	—	2.9	3.5	
		RF-GND3	*1	—	28.2	31.2	
			*2	—	1.6	2.05	
		RF-GND4	*1	—	23.4	26.4	
			*2	—	1.1	1.4	
		RF-GND5	*1	—	0.15	0.30	
			*2	—	0.56	0.71	
		RF-GND6	*1	—	0.16	0.31	
			*2	—	0.56	0.71	
Isolation	IOS	RF-GND1 to 3	*2	10	15	—	dB
		RF-GND4	*2	15	20	—	
		RF-GND5	*2	15	20	—	
		RF-GND6	*2	15	20	—	
Harmonics	2fo	RF-GND5	*3	55	75	—	dBc
	3fo		*3	55	67	—	
	2fo	RF-GND6	*3	55	75	—	
	3fo		*3	55	67	—	
$P_{0.2\ dB}$ compression	$P_{0.2\ dB}$	RF-GND5	*4	—	33	—	dBm
		RF-GND6	*4	—	33	—	
Capacitance	C1	GND1	*5	1.86	2.01	2.16	pF
	C2	GND2	*5	2.83	3.05	3.27	
	C3	GND3	*5	4.60	4.95	5.30	
	C4	GND4	*5	7.74	8.33	8.92	
Capacitance ratio	C2-1	—	C2/C1	1.44	1.52	1.60	—
	C3-2	—	C3/C2	1.53	1.62	1.71	
	C4-3	—	C4/C3	1.59	1.68	1.77	
Switching speed	SWT	RF-GND1 to 6	—	—	—	5.0	µs
Ictl	Ictl	VCTL = ALL_H	VCTL = 2.8 V	—	1.9	4.0	µA

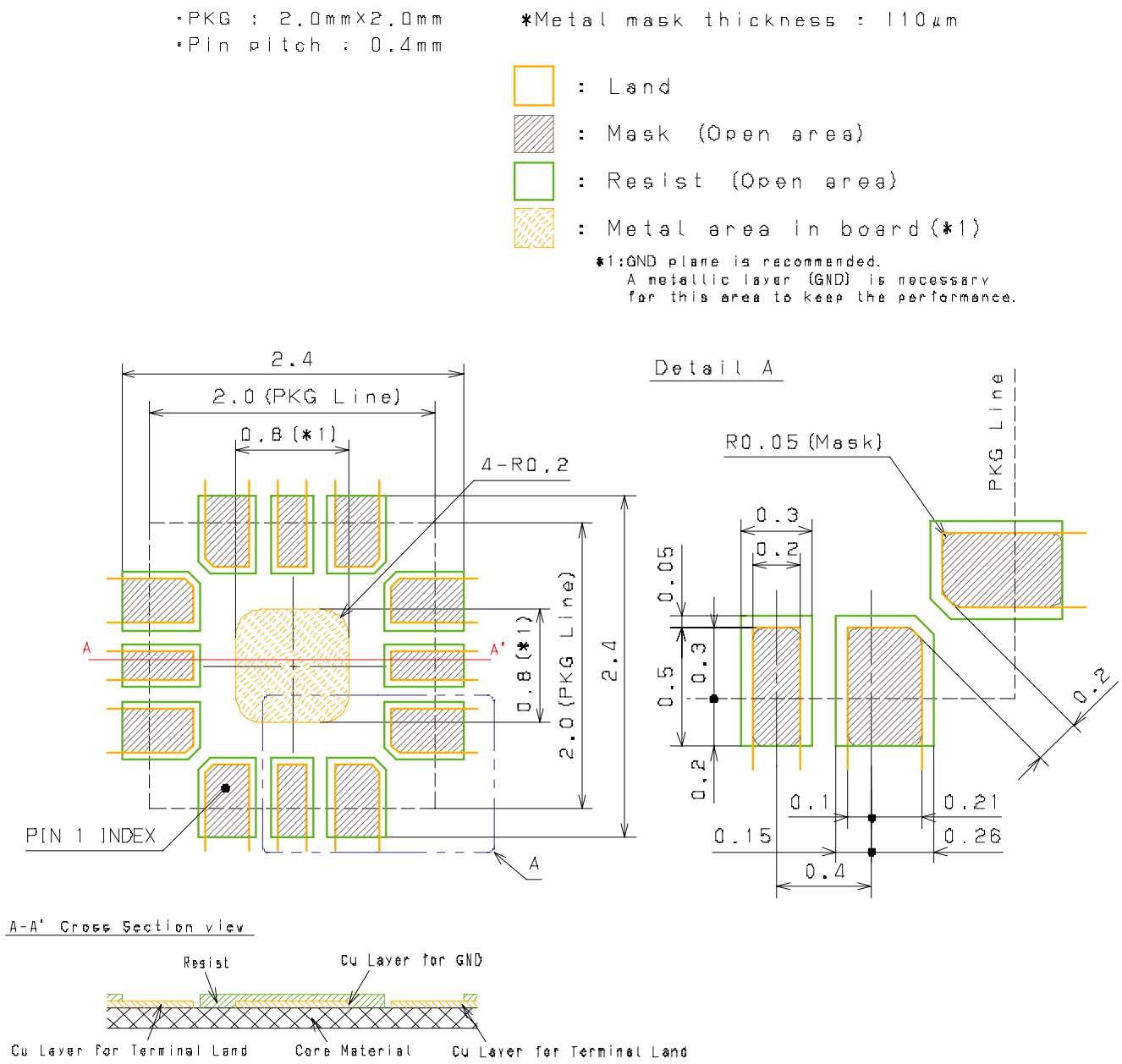
*1 Pin = 0 dBm, frequency = 13.56 MHz
*2 Pin = 0 dBm, frequency = 900 MHz
*3 Pin = 27 dBm, frequency = 900 MHz
*4 Frequency = 900 MHz
*5 Pin = 0 dBm, Calculated by S-parameter at 13.56 MHz

Recommended Circuit



∗ C1 = DC cut capacitor (10000 pF)

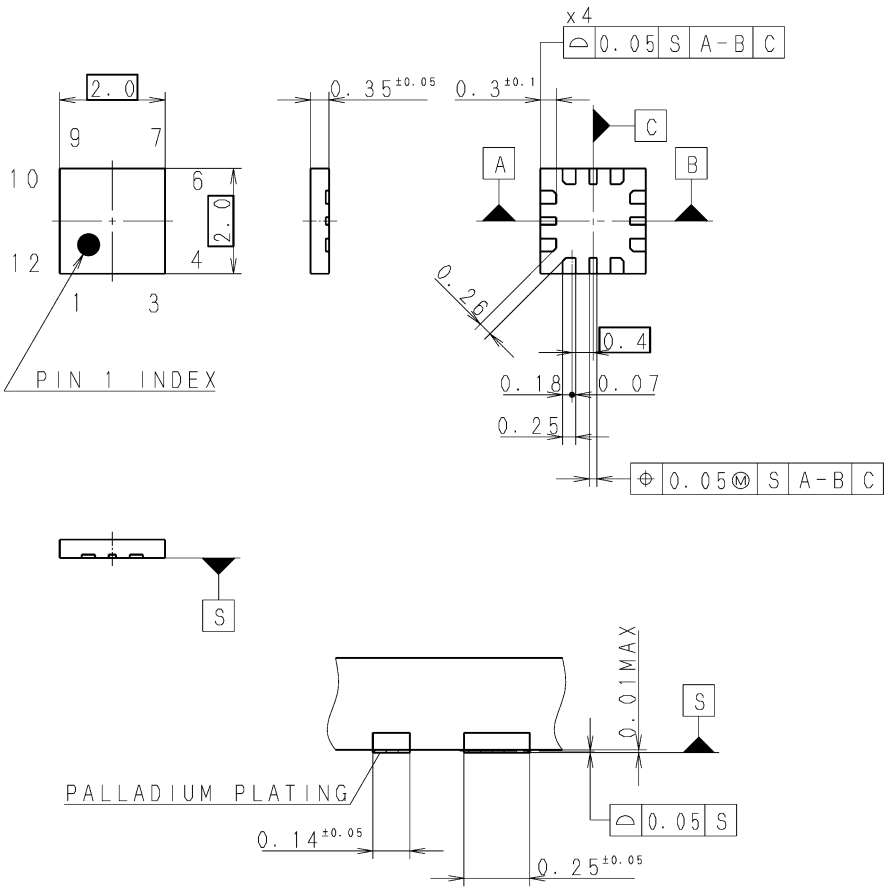
PCB Layout Template



Package Outline

Product Code: 75342691(SDT Bangna) / 75337336(SDT) / 75340787(Kagoshima)

12PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

SONY CODE	XQFN-12P-02
JEITA CODE	————
JEDEC CODE	————

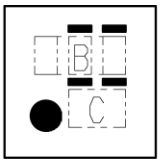
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.004g

PART No. AP-4000-12013S	
ISSUED '11.08.30	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CODE:XR-012-D	

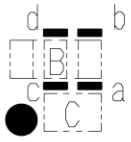
Marking

Product Code: 75342691(SDT Bangna) / 75337336(SDT) / 75340787(Kagoshima)



MARKING C: G9

注１） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注２） C部は製品名（Ｍａｘ２文字）を配置する。
（２文字を超える場合は製品名省略標示規定に従う。）
注３） マーク深さは，Ｍａｘ０．０５ｍｍの事。



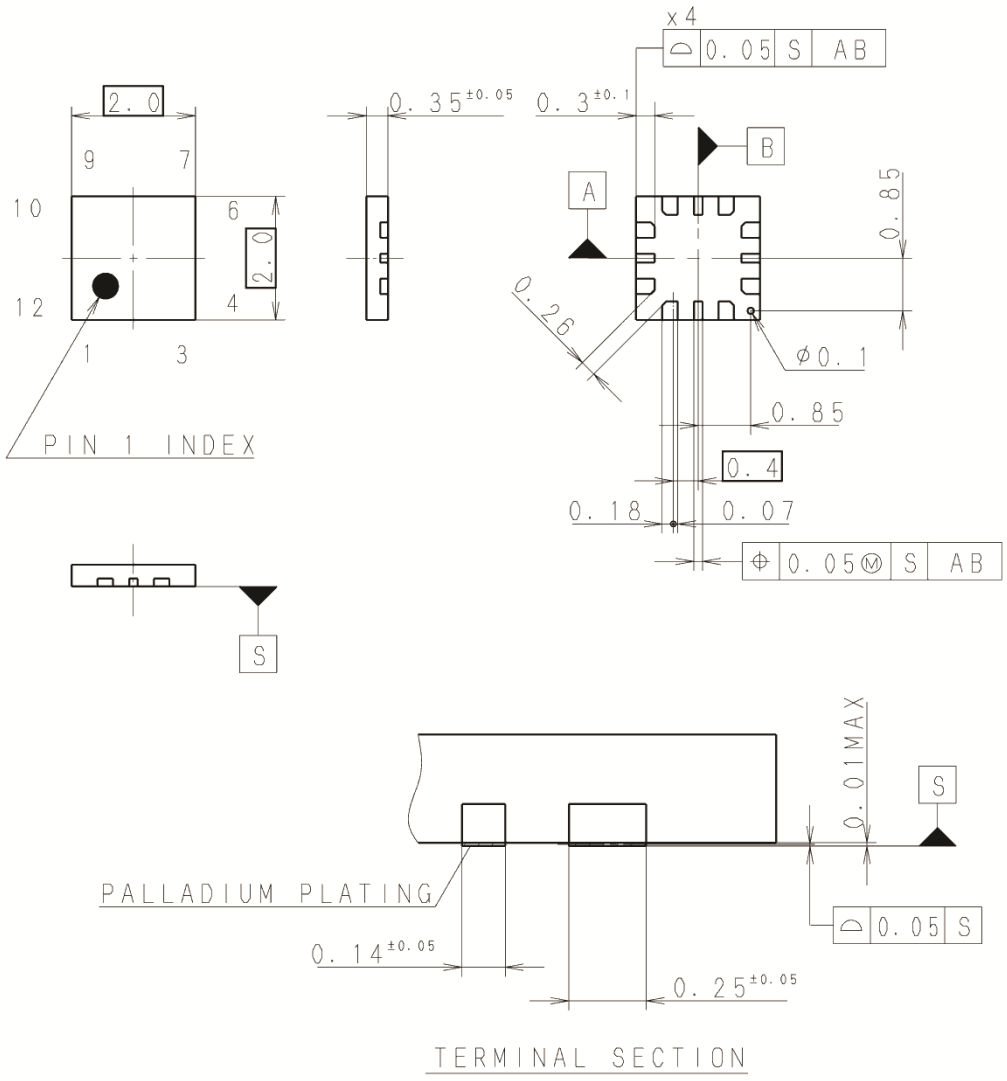
DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.

Package Outline

Product Code: 75340788,75342917 (Renesas)

12PIN XQFN (PLASTIC)



Note:Terminal burr height 0.05mm MAX.

SONY CODE	XQFN-12P-051
JEITA CODE	————
JEDEC CODE	————

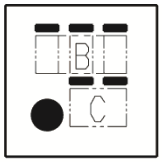
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.004g

PART No. AP-2000-12XND1	Rev. 0
ISSUED '11.12.01	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:XR-12-GD	

Marking

Product Code: 75340788,75342917 (Renesas)



MARKING C: G9

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製造年は下記2進法ビット方式により表示する。）
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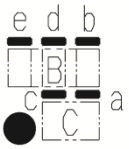
b部年コード（2進法ビット方式の2ビット目を表示）を配置する。
c部年コード（2進法ビット方式の3ビット目を表示）を配置する。
d部年コード（2進法ビット方式の4ビット目を表示）を配置する。
注2） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，Max0．05mmの事。
注4） e部は組立場所表記を配置する。



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2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.
4) ASSEMBLY PLACE IN SECTION e.

Note

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