8Mb Double Data Rate HSTL High Speed Synchronous SRAMs (256K x 36 or 512K x 18 Organization) **Preliminary**

## Description

The CXK77R3682AGB (organized as 262,144 words by 36 bits) and the CXK77R1882AGB (organized as 524,288 words by 18 bits) are high speed CMOS synchronous static RAMs with common I/O pins. These synchronous SRAMs integrate input registers, high speed RAM, output registers, and a two-deep write buffer onto a single monolithic IC. Burst and non-burst single data rate (SDR) and double data rate (DDR) Register - Register (R-R) read operations and Late Write (LW) write operations are supported, providing a flexible, high-performance user interface.

All address and control input signals except $\overline{G}$ (Output Enable) are registered on the rising edge of CK (Input Clock). Burst and non-burst, SDR and DDR read and write operations are initiated, on a cycle-by-cycle basis, via external control pins B(1:3).

During SDR read operations, output data is driven valid once, from the rising edge of CK, one full clock cycle after the address is registered. During DDR read operations, output data is driven valid twice, first from the rising edge of CK and then from the falling edge of CK, beginning one full clock cycle after the address is registered. One pair of output clocks (CQ/$\overline{CQ}$) is provided with each 18-bit word of output data. The timing relationship between each pair of output clocks and its corresponding word of output data is precisely controlled.

During SDR write operations, input data is registered once, on the rising edge of CK, one full clock cycle after the address is registered. During DDR write operations, input data is registered twice, first on the rising edge of CK and then on the falling edge of CK, beginning one full clock cycle after the address is registered.

The output drivers are series terminated, and the output impedance is programmable through an external impedance matching resistor RQ. By connecting RQ between ZQ and $V_{SS}$, the output impedance of all DQ and CQ pins can be precisely controlled.

285 MHz operation (570 Mbps) is obtained from a single 2.5V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

## Features

| 3 Speed Bins | Cycle Time / Access Time | Data Rate |
|---|---|---|
| -35 | 3.5ns / 2.2ns | 570 Mbps |
| -39 (-39A) | 3.9ns / 2.6ns (2.4ns) | 512 Mbps |
| -42 | 4.2ns / 2.6ns | 476 Mbps |

- Single 2.5V power supply ($V_{DD}$): 2.5V ± 5%
- Register - Register (R-R) read operations
- Late Write (LW), fully coherent write operations
- Single and double data rate burst read and write operations
- Linear or interleaved burst order, selectable via dedicated mode pin ($\overline{LBO}$)
- Burst length of two, three, or four, with automatic address wrap
- Two cycle deselect
- One pair of differential input clocks (CK/$\overline{CK}$)
- One pair of output clocks (CQ/$\overline{CQ}$) per 18 bits of output data (DQ)
- Asynchronous output enable ($\overline{G}$)
- Dedicated output supply voltage ($V_{DDQ}$): 1.5V to 1.8V typical
- HSTL-compatible I/O interface with dedicated input reference voltage ($V_{REF}$): $V_{DDQ}$/2 typical
- Programmable impedance output drivers
- Stop-Clock capability
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 153 pin (9x17), 1.27mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

## 256K x 36 Pin Assignment (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | $V_{DDQ}$ | SA | SA | ZQ | SA | SA | $V_{DDQ}$ | $V_{SS}$ |
| B | DQ | DQ | SA | $V_{SS}$ | B1 | $V_{SS}$ | SA | DQ | DQ |
| C | $V_{SS}$ | $V_{DDQ}$ | SA | SA | $\overline{G}$ | SA | SA | $V_{DDQ}$ | $V_{SS}$ |
| D | DQ | DQ | NC (2) | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | SA | DQ | DQ |
| E | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| F | DQ | CQ | DQ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | DQ | CQ | DQ |
| G | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | CK | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| H | DQ | DQ | DQ | $V_{DD}$ | $\overline{CK}$ | $V_{DD}$ | DQ | DQ | DQ |
| J | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| K | DQ | DQ | DQ | $V_{SS}$ | B2 | $V_{SS}$ | DQ | DQ | DQ |
| L | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $\overline{LBO}$ | B3 | NC (3) | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| M | DQ | $\overline{CQ}$ | DQ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | DQ | $\overline{CQ}$ | DQ |
| N | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| P | DQ | DQ | NC (1) | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | SA | DQ | DQ |
| R | $V_{SS}$ | $V_{DDQ}$ | $V_{DD}$ | SA | SA1 | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{SS}$ |
| T | DQ | DQ | SA | $V_{SS}$ | SA0 | $V_{SS}$ | SA | DQ | DQ |
| U | $V_{SS}$ | $V_{DDQ}$ | TMS | TDI | TCK | TDO | RSVD (4) | $V_{DDQ}$ | $V_{SS}$ |

Notes:

1. Pad Location 3P is a true no-connect. However, it is defined as an SA address input in x18 DDR SRAMs.
2. Pad Location 3D is a true no-connect. However, it is defined as an SA address input in 16Mb DDR SRAMs
3. Pad Location 6L is a true no-connect. However, it may be defined as a mode pin in future versions of DDR SRAMs.
4. Pad Location 7U must be left unconnected. It is used by Sony for internal test purposes.

## 512K x 18 Pin Assignment (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | $V_{DDQ}$ | SA | SA | ZQ | SA | SA | $V_{DDQ}$ | $V_{SS}$ |
| B | NC (1a) | DQ | SA | $V_{SS}$ | B1 | $V_{SS}$ | SA | NC (1a) | DQ |
| C | $V_{SS}$ | $V_{DDQ}$ | SA | SA | $\overline{G}$ | SA | SA | $V_{DDQ}$ | $V_{SS}$ |
| D | DQ | NC (1a) | NC (2) | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | SA | DQ | NC (1a) |
| E | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| F | NC (1a) | CQ | NC (1a) | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | DQ | NC (1b) | DQ |
| G | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | CK | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| H | DQ | NC (1a) | DQ | $V_{DD}$ | $\overline{CK}$ | $V_{DD}$ | NC (1a) | DQ | NC (1a) |
| J | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| K | NC (1a) | DQ | NC (1a) | $V_{SS}$ | B2 | $V_{SS}$ | DQ | NC (1a) | DQ |
| L | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $\overline{LBO}$ | B3 | NC (3) | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| M | DQ | NC (1b) | DQ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | NC (1a) | $\overline{CQ}$ | NC (1a) |
| N | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{SS}$ |
| P | NC (1a) | DQ | SA | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | SA | NC (1a) | DQ |
| R | $V_{SS}$ | $V_{DDQ}$ | $V_{DD}$ | SA | SA1 | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{SS}$ |
| T | DQ | NC (1a) | SA | $V_{SS}$ | SA0 | $V_{SS}$ | SA | DQ | NC (1a) |
| U | $V_{SS}$ | $V_{DDQ}$ | TMS | TDI | TCK | TDO | RSVD (4) | $V_{DDQ}$ | $V_{SS}$ |

Notes:

1a. Pad Locations 1B, 8B, 2D, 9D, 1F, 3F, 2H, 7H, 9H, 1K, 3K, 8K, 7M, 9M, 1P, 8P, 2T, and 9T are true no-connects. However, they are defined as DQ data input/outputs in x36 DDR SRAMs.

1b. Pad Locations 8F and 2M are true no-connects. However, they are defined as CQ output clocks in x36 DDR SRAMs.

2. Pad Location 3D is a true no-connect. However, it is defined as an SA address input in 16Mb DDR SRAMs

3. Pad Location 6L is a true no-connect. However, it may be defined as a mode pin in future versions of DDR SRAMs.

4. Pad Location 7U must be left unconnected. It is used by Sony for internal test purposes.

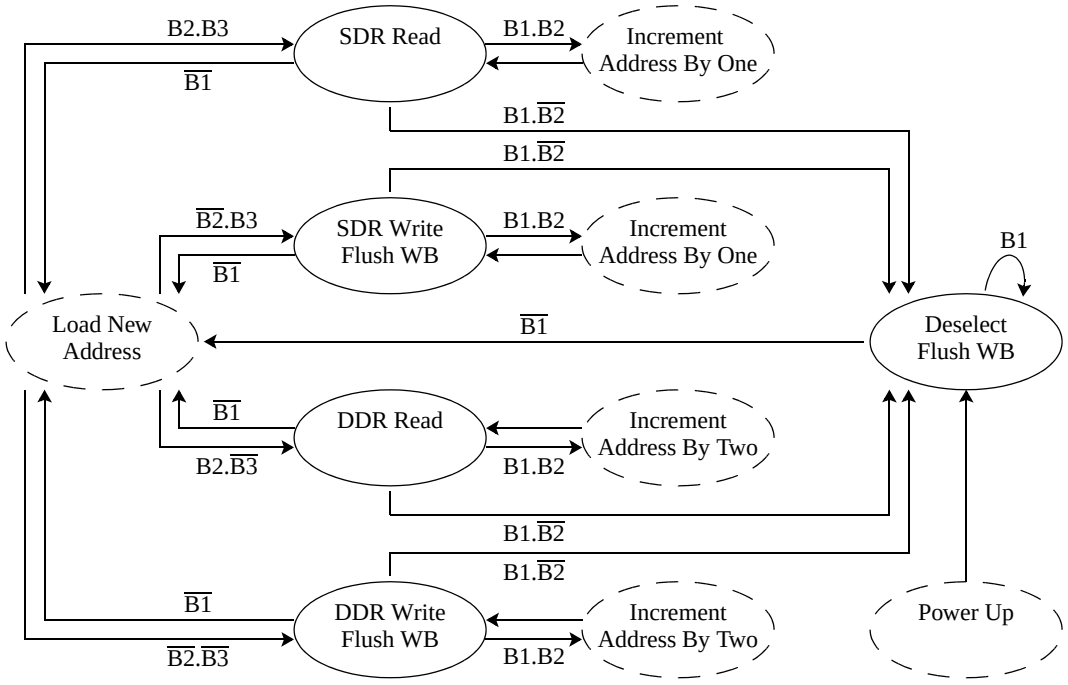
## Pin Description

| Symbol | Type | Description |
|---|---|---|
| SA | Input | Synchronous Address Inputs - Registered on the rising edge of CK. |
| SA1, SA0 | Input | Synchronous Address Inputs (1:0) - Registered on the rising edge of CK. Initialize burst counter. |
| DQ | I/O | Synchronous Data Inputs / Outputs - Registered on the rising edge of CK during SDR write operations. Registered on the rising and falling edges of CK during DDR write operations. Driven from the rising edge of CK during SDR read operations. Driven from the rising and falling edges of CK during DDR read operations |
| CK, $\overline{CK}$ | Input | Differential Input Clocks |
| CQ, $\overline{CQ}$ | I/O | Output Clocks |
| B1 | Input | Synchronous Control Input 1 - Registered on the rising edge of CK.<br>B1 = 0 loads a new address and begins a new operation<br>B1 = 1 increments the address and continues the previous operation when B2 = 1<br>specifies a deselect operation when B2 = 0 |
| B2 | Input | Synchronous Control Input 2 - Registered on the rising edge of CK.<br>B2 = 0 specifies a write operation when B1 = 0<br>specifies a deselect operation when B1 = 1<br>B2 = 1 specifies a read operation when B1 = 0<br>increments the address and continues the previous operation when B1 = 1 |
| B3 | Input | Synchronous Control Input 3 - Registered on the rising edge of CK.<br>B3 = 0 specifies a double data rate (DDR) operation when B1 = 0<br>is a “don’t care” when B1 = 1<br>B3 = 1 specifies a single data rate (SDR) operation when B1 = 0<br>is a “don’t care” when B1 = 1 |
| $\overline{G}$ | Input | Asynchronous Output Enable Input - De-asserted (high) forces the data output drivers to Hi-Z. |
| $\overline{LBO}$ | Input | Burst Order Select - This mode pin must be tied “high” or “low” to select the desired burst order.<br>$\overline{LBO}$ = 0 specifies Linear burst order<br>$\overline{LBO}$ = 1 specifies Interleaved burst order |
| ZQ | Input | Output Impedance Control Resistor Input |
| $V_{DD}$ | | 2.5V Core Power Supply - Core supply voltage. |
| $V_{DDQ}$ | | Output Power Supply - Output buffer supply voltage. |
| $V_{REF}$ | | Input Reference Voltage - Input buffer threshold voltage. |
| $V_{SS}$ | | Ground |
| TCK | Input | JTAG Clock |
| TMS | Input | JTAG Mode Select |
| TDI | Input | JTAG Data In |
| TDO | Output | JTAG Data Out |
| RSVD | | Reserved - This pin is used for Sony test purposes only. It must be left unconnected. |
| NC | | No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to $V_{DD}$, $V_{DDQ}$, or $V_{SS}$. |

## Clock Truth Table

| CK | B1 ($t_n$) | B2 ($t_n$) | B3 ($t_n$) | Previous Operation | Current Operation | DQ ($t_n$) | DQ ($t_{n+½}$) | DQ ($t_{n+1}$) | DQ ($t_{n+1½}$) |
|---|---|---|---|---|---|---|---|---|---|
| 0→1 | 0 | 1 | 1 | --- | Single Data Rate Read<br>Load New Address | X | | Q1($t_n$) | |
| 0→1 | 0 | 1 | 0 | --- | Double Data Rate Read<br>Load New Address | X | X | Q1($t_n$) | Q2($t_n$) |
| 0→1 | 0 | 0 | 1 | --- | Single Data Rate Write<br>Load New Address<br>Flush Write Buffer | X | | D1($t_n$) | |
| 0→1 | 0 | 0 | 0 | --- | Double Data Rate Write<br>Load New Address<br>Flush Write Buffer | X | X | D1($t_n$) | D2($t_n$) |
| 0→1 | 1 | 1 | X | SDR Read | Single Data Rate Read Continue<br>Increment Address by One | Q1($t_{n-1}$) | | Q2($t_n$) | |
| 0→1 | 1 | 1 | X | DDR Read | Double Data Rate Read Continue<br>Increment Address by Two | Q1($t_{n-1}$) | Q2($t_{n-1}$) | Q3($t_n$) | Q4($t_n$) |
| 0→1 | 1 | 1 | X | SDR Write | Single Data Rate Write Continue<br>Increment Address by One<br>Flush Write Buffer | D1($t_{n-1}$) | | D2($t_n$) | |
| 0→1 | 1 | 1 | X | DDR Write | Double Data Rate Write Continue<br>Increment Address by Two<br>Flush Write Buffer | D1($t_{n-1}$) | D2($t_{n-1}$) | D3($t_n$) | D4($t_n$) |
| 0→1 | 1 | 0 | X | not Deselect | Deselect | X | | Hi - Z | |
| 0→1 | 1 | X | X | Deselect | Deselect (Continue) | Hi - Z | | Hi - Z | |

## State Diagram



## •Burst Operations

When $\overline{LBO}$ = 1, burst operations follow the **Interleaved Burst** address sequence depicted in the table below:

| Interleaved Burst | HEX | | | | BINARY | | | | Sequence Key |
|---|---|---|---|---|---|---|---|---|---|
| | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | |
| 1st (Base) Address | 0 | 1 | 2 | 3 | 00 | 01 | 10 | 11 | SA1, SA0 |
| 2nd Address | 1 | 0 | 3 | 2 | 01 | 00 | 11 | 10 | SA1, $\overline{SA0}$ |
| 3rd Address | 2 | 3 | 0 | 1 | 10 | 11 | 00 | 01 | $\overline{SA1}$, SA0 |
| 4th Address | 3 | 2 | 1 | 0 | 11 | 10 | 01 | 00 | $\overline{SA1}$, $\overline{SA0}$ |

When $\overline{LBO}$ = 0, burst operations follow the **Linear Burst** address sequence depicted in the table below:

| Linear Burst | HEX | | | | BINARY | | | | Sequence Key |
|---|---|---|---|---|---|---|---|---|---|
| | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | SA (1:0) | |
| 1st (Base) Address | 0 | 1 | 2 | 3 | 00 | 01 | 10 | 11 | SA1, SA0 |
| 2nd Address | 1 | 2 | 3 | 0 | 01 | 10 | 11 | 00 | (SA1 xor SA0), $\overline{SA0}$ |
| 3rd Address | 2 | 3 | 0 | 1 | 10 | 11 | 00 | 01 | $\overline{SA1}$, SA0 |
| 4th Address | 3 | 0 | 1 | 2 | 11 | 00 | 01 | 10 | $\overline{(SA1 \text{ xor } SA0)}$, $\overline{SA0}$ |

## •Programmable Impedance Output Drivers

These devices have programmable impedance output drivers. The output impedance is controlled by an external resistor, RQ, connected between the SRAM's ZQ pin and $V_{SS}$, and is equal to one-fifth the value of this resistor, nominally. See the DC Electrical Characteristics section for further information.

The output impedance is updated whenever the output drivers are in a Hi-Z state. Consequently, impedance updates will occur during write and deselect operations, and when $\overline{G}$ is deasserted (high) (see **Note 1** below). At power up, 8192 clock cycles followed by an impedance update via one of the three methods described above are required to ensure that the output impedance has reached the desired value. After power up, periodic impedance updates via one of the three methods described above are also required to ensure that the output impedance remains within specified tolerances.

**Note 1:** In order to allow the SRAM sufficient time to update the output impedance when $\overline{G}$ is deasserted (high), $\overline{G}$ must meet setup and hold times with respect to CK clock. See the AC Electrical Characteristics section for further information.

## •Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence: $V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$, and Inputs. $V_{DDQ}$ should never exceed $V_{DD}$. If this power supply sequence cannot be met, a large bypass diode may be required between $V_{DD}$ and $V_{DDQ}$. Please contact Sony Memory Application Department for further information.

## •Absolute Maximum Ratings(1)

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +3.6 | V |
| Output Supply Voltage | $V_{DDQ}$ | -0.5 to +3.6 | V |
| Input Voltage (Address, Control, Data, Clock) | $V_{IN}$ | -0.5 to +2.6 | V |
| Input Voltage ($\overline{LBO}$) | $V_{MIN}$ | -0.5 to +2.6 | V |
| Input Voltage (TCK, TMS, TDI)) | $V_{TIN}$ | -0.5 to +2.6 | V |
| Operating Temperature | $T_A$ | 0 to 85 | °C |
| Junction Temperature | $T_J$ | 0 to 110 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 150 | °C |

(1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## •BGA Package Thermal Characteristics

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Junction to Case Temperature | $\Theta_{JC}$ | 1.0 | °C/W |

## •I/O Capacitance

**($T_A$ = 25°C, f = 1 MHz)**

| Item | | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | Address | $C_{ADDR}$ | $V_{IN}$ = 0V | --- | 3.0 | pF |
| | Control | $C_{CTRL}$ | $V_{IN}$ = 0V | --- | 3.5 | pF |
| | CK Clock | $C_{CK}$ | $V_{IN}$ = 0V | --- | 3.5 | pF |
| Output Capacitance | Data | $C_{DATA}$ | $V_{OUT}$ = 0V | --- | 4.5 | pF |
| | CQ Clock | $C_{CQ}$ | $V_{OUT}$ = 0V | --- | 4.5 | pF |

Note: These parameters are sampled and are not 100% tested.

## •DC Recommended Operating Conditions

**($V_{SS}$ = 0V, $T_A$ = 0 to 85°C)**

| Item | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.37 | 2.5 | 2.63 | V | |
| Output Supply Voltage | $V_{DDQ}$ | 1.4 | --- | 1.9 | V | |
| Input Reference Voltage | $V_{REF}$ | 0.6 | --- | 1.1 | V | 1 |
| Input High Voltage (Address, Control, Data) | $V_{IH}$ | $V_{REF}$ + 0.1 | --- | 2.4 | V | 2,4 |
| Input Low Voltage (Address, Control, Data) | $V_{IL}$ | -0.3 | --- | $V_{REF}$ - 0.1 | V | 3 |
| Input High Voltage ($\overline{LBO}$) | $V_{MIH}$ | $V_{REF}$ + 0.3 | --- | 2.4 | V | 4 |
| Input Low Voltage ($\overline{LBO}$) | $V_{MIL}$ | -0.3 | --- | $V_{REF}$ - 0.3 | V | |
| Clock Input Signal Voltage | $V_{KIN}$ | -0.3 | --- | 2.4 | V | 4 |
| Clock Input Differential Voltage | $V_{DIF}$ | 0.2 | --- | 2.7 | V | |
| Clock Input Common Mode Voltage | $V_{CM}$ | 0.6 | --- | 1.1 | V | |

(1) The peak-to-peak AC component superimposed on $V_{REF}$ may not exceed 5% of the DC component.

(2) $V_{IH}$ (max) AC = +3.3V for pulse width less than one-quarter of the cycle time ($t_{CYC}$/4).

(3) $V_{IL}$ (min) AC = -1.1V for pulse width less than one-quarter of the cycle time ($t_{CYC}$/4).

(4) $V_{IH}$ (max), $V_{MIH}$ (max), and $V_{KIN}$ (max) > 2.4V is supported, but input leakage current will be greater than as specified. Please contact Sony Memory Application Department for further information.

## •DC Electrical Characteristics

**($V_{DD}$ = 2.5V ± 5%, $V_{SS}$ = 0V, $T_A$ = 0 to 85°C)**

| Item | Symbol | Test Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input Leakage Current (Address, Control, Clock) | $I_{LI}$ | $V_{IN}$ = $V_{SS}$ to 2.1V | -1 | --- | 1 | uA | |
| Input Leakage Current ($\overline{LBO}$) | $I_{MLI}$ | $V_{MIN}$ = $V_{SS}$ to 2.1V | -1 | --- | 1 | uA | |
| Input Leakage Current (Data) | $I_{DLI}$ | $V_{DIN}$ = $V_{SS}$ to 2.1V<br>$\overline{G}$ = $V_{IH}$ | -10 | --- | 10 | uA | |
| Average Power Supply Operating Current - x36 | $I_{DD-35}$<br>$I_{DD-39}$<br>$I_{DD-42}$ | $I_{OUT}$ = 0 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | ---<br>---<br>--- | 810<br>760<br>720 | 950<br>890<br>840 | mA | |
| Average Power Supply Operating Current - x18 | $I_{DD-35}$<br>$I_{DD-39}$<br>$I_{DD-42}$ | $I_{OUT}$ = 0 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | ---<br>---<br>--- | 750<br>700<br>660 | 880<br>820<br>770 | mA | |
| Power Supply Deselect Operating Current (NOP Current) | $I_{DD2-35}$<br>$I_{DD2-39}$<br>$I_{DD2-42}$ | $I_{OUT}$ = 0 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | ---<br>---<br>--- | 380<br>360<br>340 | 440<br>420<br>400 | mA | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0 mA<br>RQ = 250Ω | $V_{DDQ}$-0.4 | --- | --- | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA<br>RQ = 250Ω | --- | --- | 0.4 | V | |
| Output Driver Impedance | $R_{OUT}$ | $V_{OH}$, $V_{OL}$ = $V_{DDQ}$/2<br>RQ < 150Ω | --- | --- | 33<br>(30*1.1) | Ω | 1,3 |
| | | $V_{OH}$ = $V_{DDQ}$/2<br>150Ω ≤ RQ ≤ 350Ω | (RQ/5)*<br>0.9 | RQ/5 | (RQ/5)*<br>1.1 | Ω | 3 |
| | | $V_{OH}$, $V_{OL}$= $V_{DDQ}$/2<br>RQ > 350Ω | 63<br>(70*0.9) | --- | --- | Ω | 2,3 |

1. For maximum output drive (i.e. minimum impedance), the ZQ pin can be tied directly to $V_{SS}$.
2. For minimum output drive (i.e. maximum impedance), the ZQ pin can be left unconnected or tied to $V_{DDQ}$.
3. This parameter is guaranteed by design through extensive corner lot characterization.

## •AC Electrical Characteristics

| Parameter | Symbol | -35 | | -39 | | -42 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Input Clock Cycle Time | $t_{KHKH}$ | 3.5 | --- | 3.9 | --- | 4.2 | --- | ns | |
| Input Clock High Pulse Width<br>Input Clock Low Pulse Width | $t_{KHKL}$<br>$t_{KLKH}$ | 1.3 | --- | 1.5 | --- | 1.5 | --- | ns | |
| Address Input Setup Time | $t_{AVKH}$ | 0.4 | --- | 0.5 | --- | 0.5 | --- | ns | |
| Address Input Hold Time | $t_{KHAX}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns | |
| Control Input Setup Time | $t_{BVKH}$ | 0.4 | --- | 0.5 | --- | 0.5 | --- | ns | |
| Control Input Hold Time | $t_{KHBX}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns | |
| Data Input Setup Time | $t_{DVKH}$<br>$t_{DVKL}$ | 0.4 | --- | 0.4 | --- | 0.4 | --- | ns | |
| Data Input Hold Time | $t_{KHDX}$<br>$t_{KLDX}$ | 0.4 | --- | 0.4 | --- | 0.4 | --- | ns | |
| Output Enable Setup Time | $t_{GVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns | 1,2 |
| Output Enable Hold Time | $t_{KHGX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns | 1,2 |
| Input Clock High to Output Data Valid (“A” Sub-Bin) | $t_{KHQV}$ | --- | 2.2 | --- | 2.6<br>2.4 | ---- | 2.6 | --- | |
| Input Clock Low to Output Data Valid (“A” Sub-Bin) | $t_{KLQV}$ | --- | 2.2 | --- | 2.6<br>2.4 | ---- | 2.6 | --- | |
| Input Clock High to Output Data Hold<br>Input Clock Low to Output Data Hold | $t_{KHQX}$<br>$t_{KLQX}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | 2 |
| Input Clock High to Output Data Low-Z | $t_{KHQX1}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns | 2,3 |
| Input Clock High to Output Data High-Z (“A” Sub-Bin) | $t_{KHQZ}$ | --- | 2.2 | --- | 2.6<br>2.4 | --- | 2.6 | ns | 2,3 |
| Input Clock Crossing to Output Clock High (“A” Sub-Bin) | $t_{KXCH}$ | 0.5 | 2.1 | 0.5 | 2.5<br>2.3 | 0.5 | 2.5 | ns | |
| Input Clock Crossing to Output Clock Low (“A” Sub-Bin) | $t_{KXCL}$ | 0.5 | 2.1 | 0.5 | 2.5<br>2.3 | 0.5 | 2.5 | ns | |
| Output Clock High to Output Data Valid<br>Output Clock Low to Output Data Valid | $t_{CHQV}$<br>$t_{CLQV}$ | --- | 0.1 | --- | 0.1 | --- | 0.1 | ns | 2 |
| Output Clock High to Output Data Hold<br>Output Clock Low to Output Data Hold | $t_{CHQX}$<br>$t_{CLQX}$ | -0.3 | --- | -0.3 | --- | -0.3 | --- | ns | 2 |
| Output Clock High Pulse Width | $t_{CHCL}$ | $t_{KHKL} \pm 0.1$ | | $t_{KHKL} \pm 0.1$ | | $t_{KHKL} \pm 0.1$ | | ns | 2 |
| Output Clock Low Pulse Width | $t_{CLCH}$ | $t_{KLKH} \pm 0.1$ | | $t_{KLKH} \pm 0.1$ | | $t_{KLKH} \pm 0.1$ | | ns | 2 |
| Output Enable Low to Output Data Valid | $t_{GLQV}$ | --- | 1.8 | --- | 2.0 | --- | 2.2 | ns | |
| Output Enable Low to Output Data Low-Z | $t_{GLQX}$ | 0.3 | --- | 0.3 | --- | 0.3 | --- | ns | 2,3 |
| Output Enable High to Output Data High-Z | $t_{GHQZ}$ | --- | 1.8 | --- | 2.0 | --- | 2.2 | ns | 2,3 |

All parameters are specified over the range $T_A$ = 0 to 85°C.

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal, unless otherwise noted.

1. These parameters apply only when deasserting $\overline{G}$ (high) in order to induce output impedance updates.
2. These parameters are verified through device characterization, and are not 100% tested.
3. These parameters are measured at ± 50mV from steady state voltage.

## •AC Electrical Characteristics (Note)

The four AC timing parameters listed below are tested according to specific combinations of Output Clocks (CQs) and Output Data (DQs):

1. $t_{CHQV}$ - Output Clock High to Output Data Valid (max)
2. $t_{CLQV}$ - Output Clock Low to Output Data Valid (max)
3. $t_{CHQX}$ - Output Clock High to Output Data Hold (min)
4. $t_{CLQX}$ - Output Clock Low to Output Data Hold (min)

The specific CQ / DQ combinations are defined as follows:

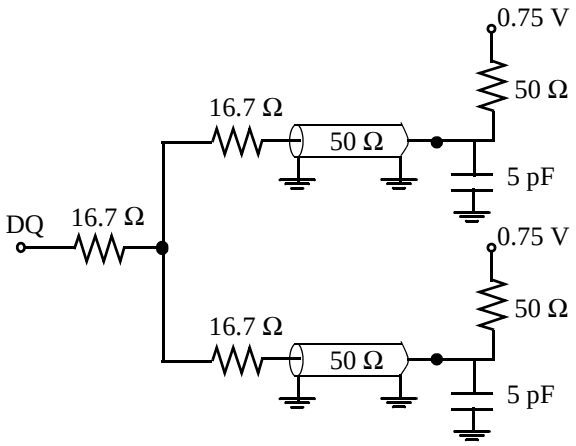
| 256K x 36 | | 512K x 18 | |
|---|---|---|---|
| CQs | DQs | CQs | DQs |
| 2F, 8M | 1D, 1H, 1M, 1T, 2B, 2K, 2P, 3H, 3M, 7F, 7K, 8D, 8H, 8T, 9B, 9F, 9K, 9P | 2F, 8M | 1D, 1H, 1M, 1T, 2B, 2K, 2P, 3H, 3M, 7F, 7K, 8D, 8H, 8T, 9B, 9F, 9K, 9P |
| 2M, 8F | 1B, 1F, 1K, 1P, 2D, 2H, 2T, 3F, 3K, 7H, 7M, 8B, 8K, 8P, 9D, 9H, 9M, 9T | | |

## •AC Test Conditions ($V_{DDQ}$ = 1.5V)

**($V_{DD}$ = 2.5V ± 5%, $V_{DDQ}$ = 1.5V ± 0.1V, $T_A$ = 0 to 85°C)**

| Item | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| Input Reference Voltage | $V_{REF}$ | 0.75 | V | |
| Input High Level | $V_{IH}$ | 1.25 | V | |
| Input Low Level | $V_{IL}$ | 0.25 | V | |
| Input Rise & Fall Time | | 0.5 | V/ns | |
| Input Reference Level | | 0.75 | V | |
| Clock Input High Voltage | $V_{KIH}$ | 1.25 | V | $V_{DIF}$ = 1.0V |
| Clock Input Low Voltage | $V_{KIL}$ | 0.25 | V | $V_{DIF}$ = 1.0V |
| Clock Input Common Mode Voltage | $V_{CM}$ | 0.75 | V | |
| Clock Input Rise & Fall Time | | 0.5 | V/ns | |
| Clock Input Reference Level | | CK/$\overline{CK}$ cross | V | |
| Output Reference Level | | 0.75 | V | |
| Output Load Conditions | | | | Fig.1<br>RQ = 250Ω |

**Fig. 1: AC Test Output Load ($V_{DDQ}$ = 1.5V)**

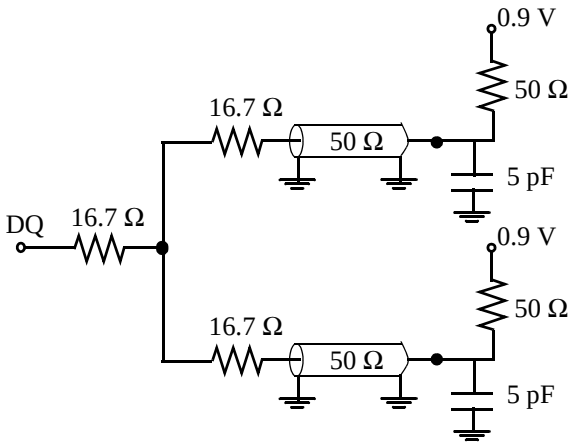


## •AC Test Conditions ($V_{DDQ}$ = 1.8V)

**($V_{DD}$ = 2.5V ± 5%, $V_{DDQ}$ = 1.8V ± 0.1V, $T_A$ = 0 to 85°C)**

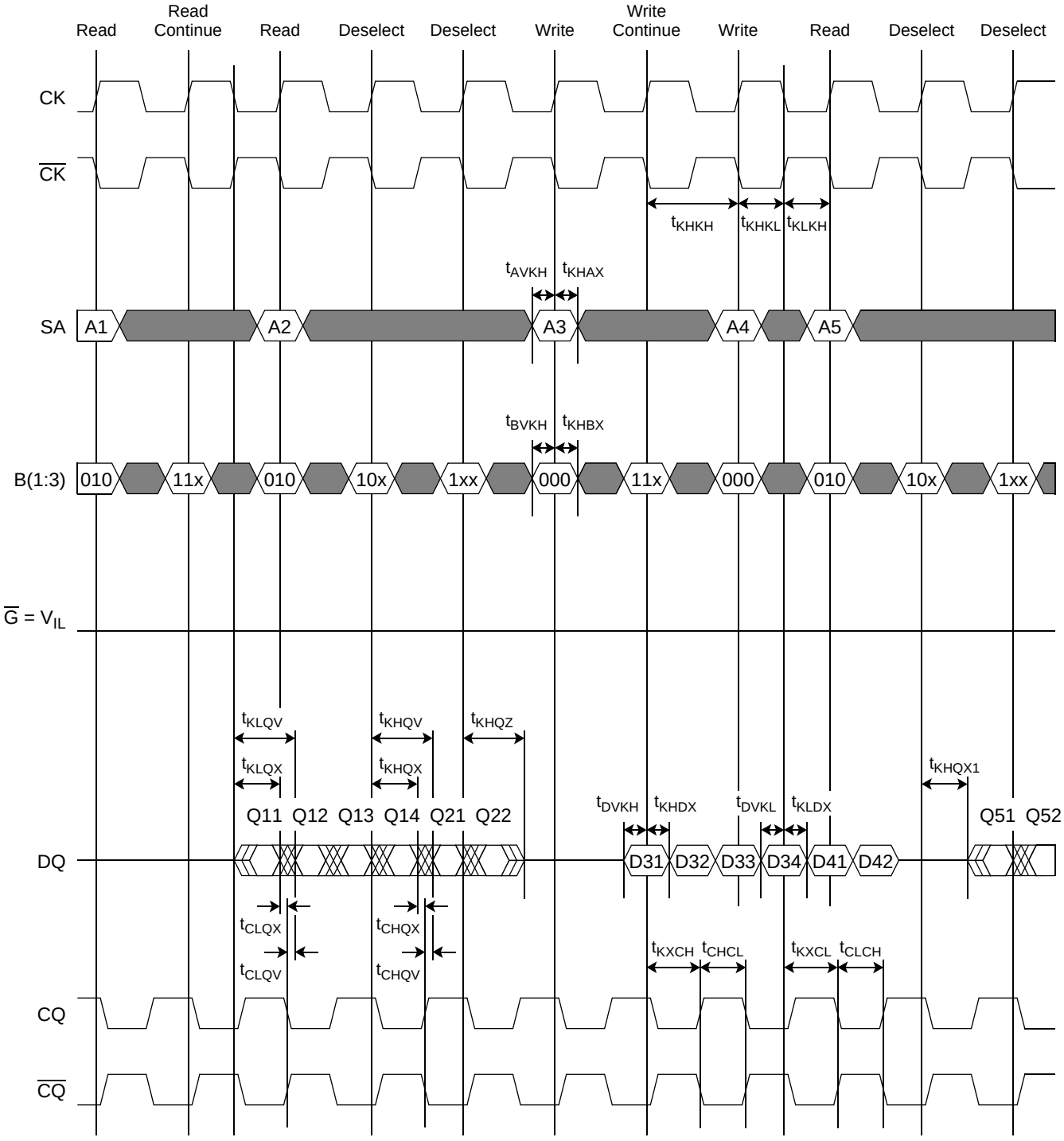
| Item | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| Input Reference Voltage | $V_{REF}$ | 0.9 | V | |
| Input High Level | $V_{IH}$ | 1.4 | V | |
| Input Low Level | $V_{IL}$ | 0.4 | V | |
| Input Rise & Fall Time | | 0.5 | V/ns | |
| Input Reference Level | | 0.9 | V | |
| Clock Input High Voltage | $V_{KIH}$ | 1.4 | V | $V_{DIF}$ = 1.0V |
| Clock Input Low Voltage | $V_{KIL}$ | 0.4 | V | $V_{DIF}$ = 1.0V |
| Clock Input Common Mode Voltage | $V_{CM}$ | 0.9 | V | |
| Clock Input Rise & Fall Time | | 0.5 | V/ns | |
| Clock Input Reference Level | | CK/$\overline{CK}$ cross | V | |
| Output Reference Level | | 0.9 | V | |
| Output Load Conditions | | | | Fig.2<br>RQ = 250Ω |

**Fig. 2: AC Test Output Load ($V_{DDQ}$ = 1.8V)**



## Timing Diagram of Double Data Rate (DDR) Read-Write-Read Operations Synchronously Controlled via Deselect Operations ($\overline{G}$ = Low)

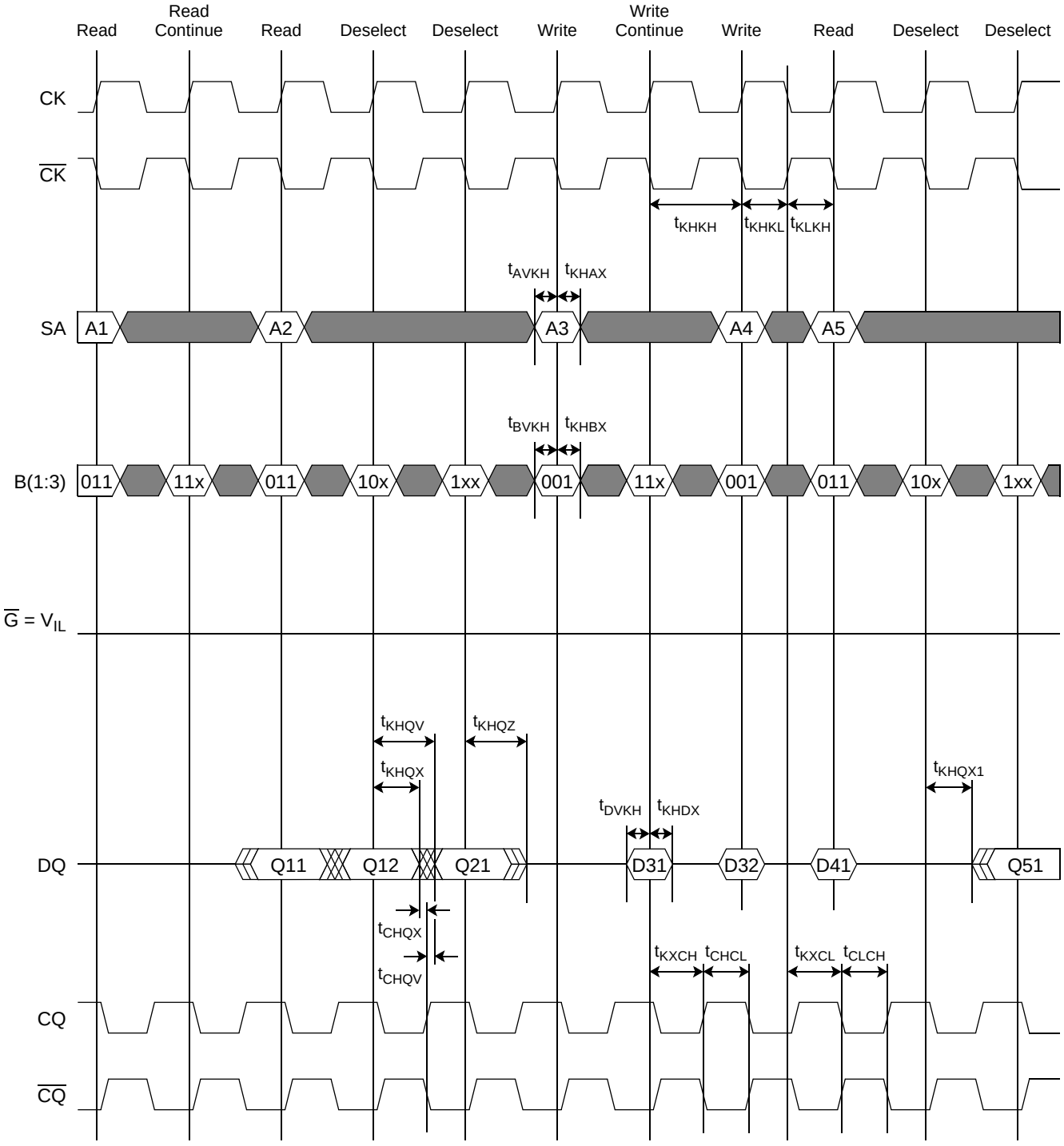
**Figure 3**




Note: In the diagram above, two Deselect operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Deselect operation may be sufficient.

## Timing Diagram of Single Data Rate (SDR) Read-Write-Read Operations Synchronously Controlled via Deselect Operations ($\overline{G}$ = Low)

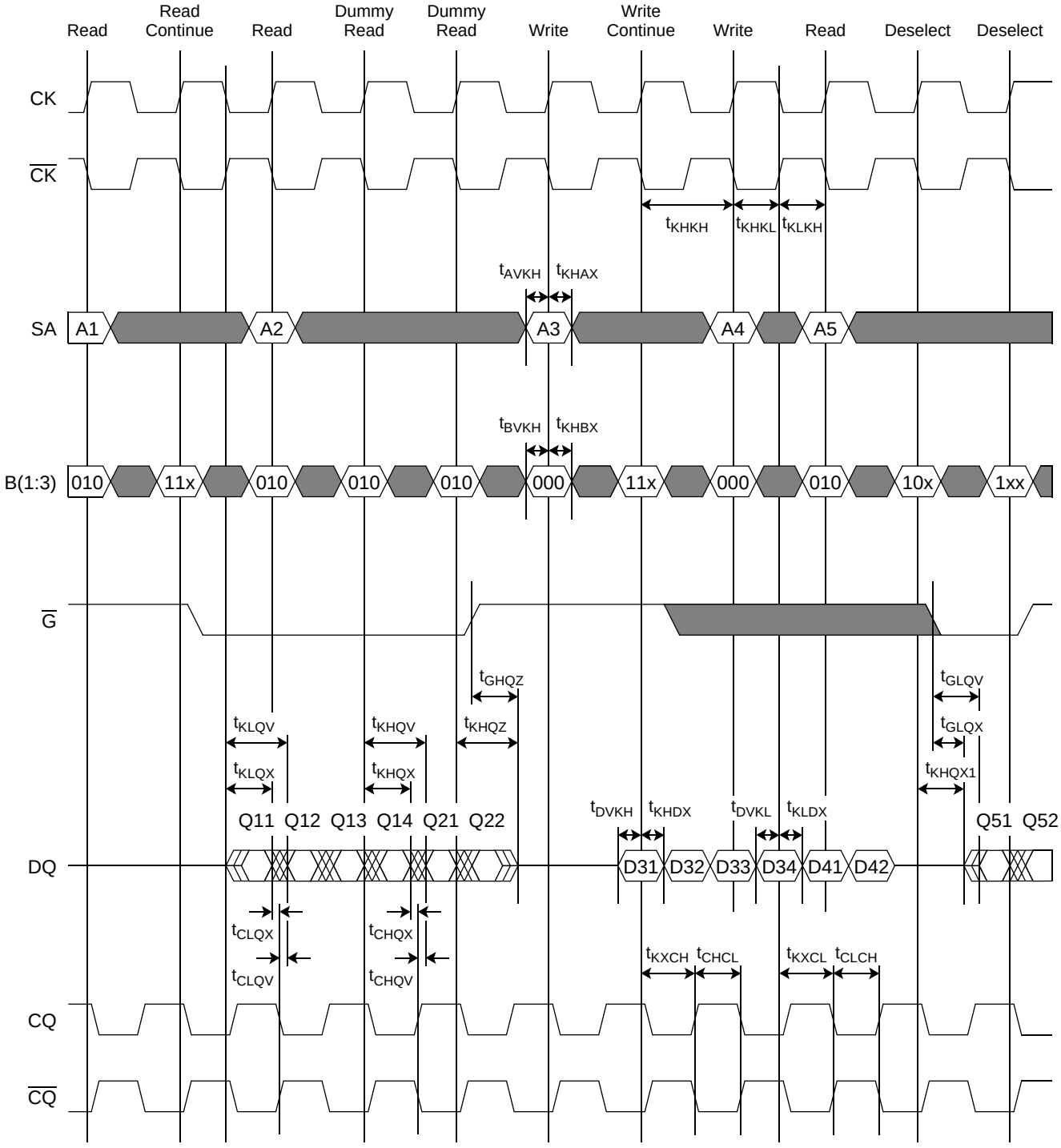
**Figure 4**




Note: In the diagram above, two Deselect operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Deselect operation may be sufficient.

## Timing Diagram of Double Data Rate (DDR) Read-Write-Read Operations Asynchronously Controlled via $\overline{G}$ and Dummy Read Operations

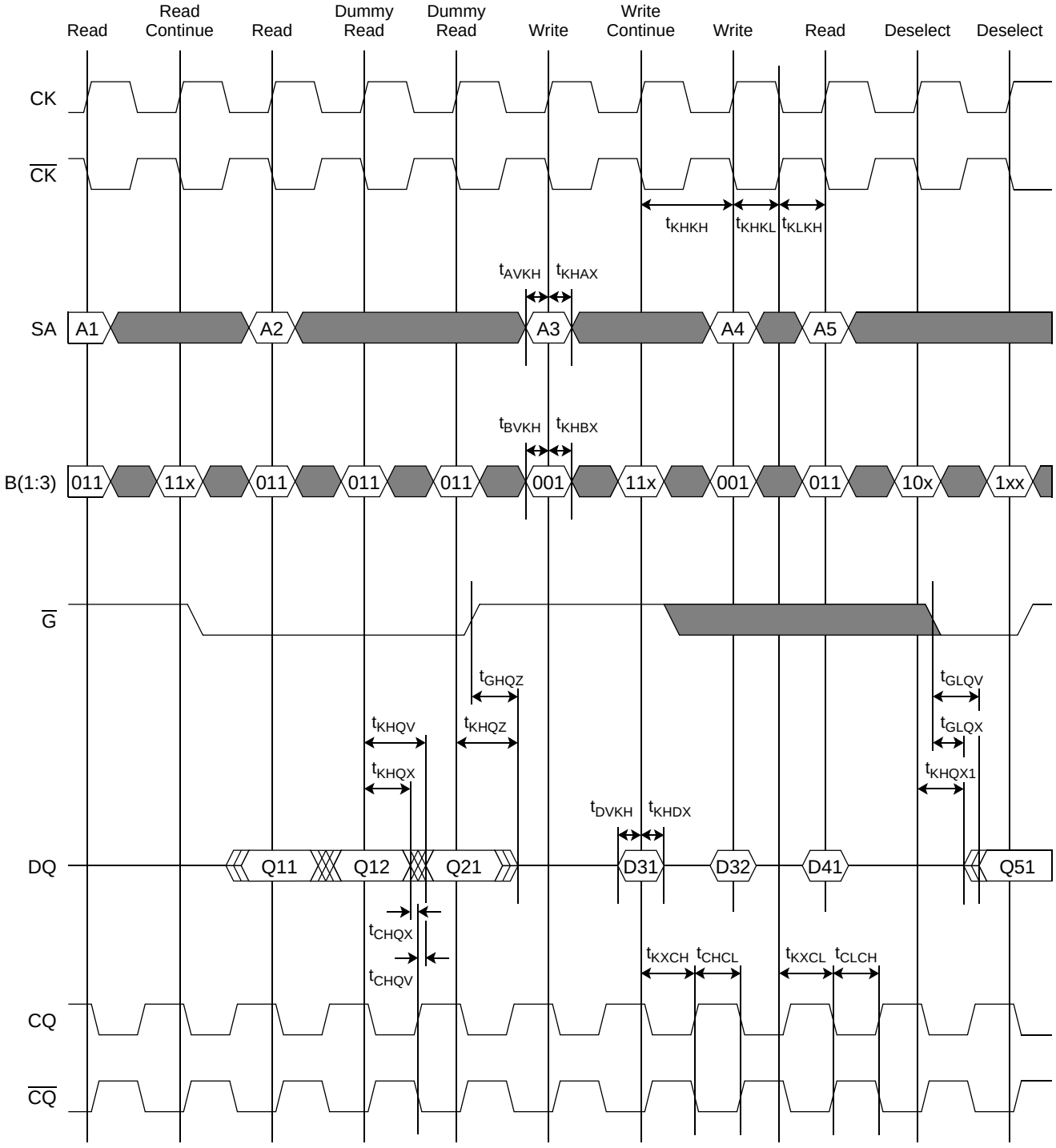
**Figure 5**




Note: In the diagram above, two Dummy Read operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Dummy Read operation may be sufficient.

## Timing Diagram of Single Data Rate (SDR) Read-Write-Read Operations Asynchronously Controlled via $\overline{G}$ and Dummy Read Operations

**Figure 6**




Note: In the diagram above, two Dummy Read operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Dummy Read operation may be sufficient.

## •Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist on one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

| | | |
|---|---|---|
| TCK: | Test Clock | Induces (clocks) TAP Controller state transitions. |
| TMS: | Test Mode Select | Inputs commands to the TAP Controller. Sampled on the rising edge of TCK. |
| TDI: | Test Data In | Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK. |
| TDO: | Test Data Out | Outputs data serially from the TAP Registers. Driven from the falling edge of TCK. |

### Disabling the TAP

When JTAG is not used, TCK should be tied “low” to prevent clocking the SRAM. TMS and TDI should either be tied “low” or tied “high” through a pull-up resistor, but they cannot be left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not interfere with normal SRAM operation EXCEPT during the SAMPLE-Z instruction, which forces the SRAM’s data output drivers (DQs) to a High-Z state. Consequently, when JTAG is not used the TAP can be operated or disabled any number of ways without adversely affecting the functionality of the device.

### JTAG DC Recommended Operating Conditions

**($T_A$ = 0 to 85°C)**

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| JTAG Input High Voltage (TCK) | $V_{TKIH}$ | --- | 1.7 | $V_{DD}$ | V |
| JTAG Input Low Voltage (TCK) | $V_{TKIL}$ | --- | -0.3 | 0.7 | V |
| JTAG Input High Voltage (TMS, TDI) | $V_{TIH}$ | --- | $V_{REF}$ + 0.4 | $V_{DD}$ | V |
| JTAG Input Low Voltage (TMS, TDI) | $V_{TIL}$ | --- | -0.3 | $V_{REF}$ - 0.4 | V |
| JTAG Output High Voltage (TDO) | $V_{TOH}$ | $I_{TOH}$ = -2.0 mA | 2.0 | --- | V |
| JTAG Output Low Voltage (TDO) | $V_{TOL}$ | $I_{TOL}$ = 2.0 mA | --- | 0.2 | V |
| JTAG Input Leakage Current | $I_{TLI}$ | $V_{TIN}$ = $V_{SS}$ to $V_{DD}$ | -10 | 10 | uA |

### JTAG AC Test Conditions

**($V_{DD}$ = 2.5V ± 5%, $T_A$ = 0 to 85°C)**

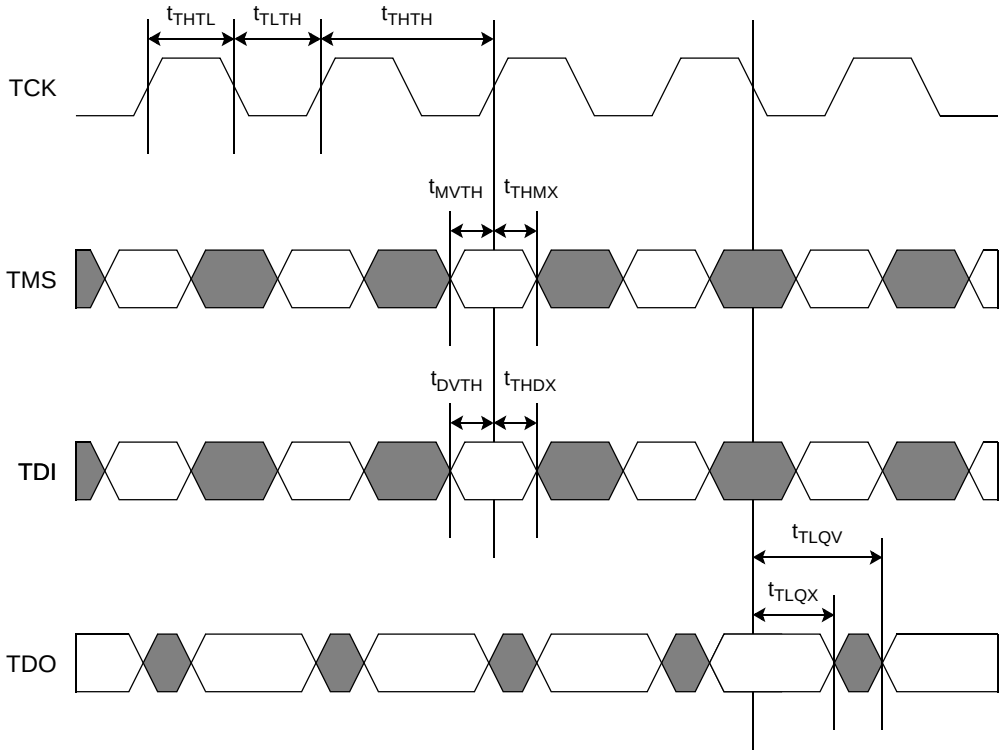
| Parameter | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| JTAG Input High Level | $V_{TIH}$ | 2.5 | V | |
| JTAG Input Low Level | $V_{TIL}$ | 0.0 | V | |
| JTAG Input Rise & Fall Time | | 0.5 | V/ns | |
| JTAG Input Reference Level | | 1.25 | V | |
| JTAG Output Reference Level | | 1.25 | V | |
| JTAG Output Load Condition | | | | See Fig.1 (p. 12) |

## JTAG AC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| TCK Cycle Time | $t_{THTH}$ | 100 | | ns |
| TCK High Pulse Width | $t_{THTL}$ | 40 | | ns |
| TCK Low Pulse Width | $t_{TLTH}$ | 40 | | ns |
| TMS Setup Time | $t_{MVTH}$ | 10 | | ns |
| TMS Hold TIme | $t_{THMX}$ | 10 | | ns |
| TDI Setup Time | $t_{DVTH}$ | 10 | | ns |
| TDI Hold TIme | $t_{THDX}$ | 10 | | ns |
| TCK Low to TDO Valid | $t_{TLQV}$ | | 20 | ns |
| TCK Low to TDO Hold | $t_{TLQX}$ | 0 | | ns |

## JTAG Timing Diagram

**Figure 7**



## TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: “Instruction Registers”, of which there is one- the Instruction Register, and “Data Registers”, of which there are three - the ID Register, the Bypass Register, and the Boundary Scan Register. Individual TAP registers are “selected” (inserted between TDI and TDO) when the appropriate sequence of commands is given to the TAP Controller.

**Instruction Register (3 bits)**

The Instruction Register stores the instructions that are executed by the TAP Controller when the TAP Controller is in the “Run-Test / Idle” state, or in any of the various “Data Register” states. It is loaded with the IDCODE instruction at power-up, or when the TAP Controller is in the “Test-Logic Reset” state or the “Capture-IR” state. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed by the TAP Controller until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

| Code (2:0) | Instruction | Description |
|---|---|---|
| 000 | BYPASS | Inserts the Bypass Register between TDI and TDO. |
| 001 | IDCODE | Inserts the ID Register between TDI and TDO. |
| 010 | SAMPLE-Z | Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. Forces the SRAM’s outputs (DQs and CQs) to High-Z. |
| 011 | BYPASS | Inserts the Bypass Register between TDI and TDO. |
| 100 | SAMPLE | Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. |
| 101 | PRIVATE | Do not use. Reserved for manufacturer use only. |
| 110 | BYPASS | Inserts the Bypass Register between TDI and TDO. |
| 111 | BYPASS | Inserts the Bypass Register between TDI and TDO. |

Bit 0 is the LSB of the Instruction Register, and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

**ID Register (32 bits)**

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The ID Register is 32 bits wide, and is encoded as follows:

| Device | Revision Number (31:28) | Part Number (27:12) | Sony ID (11:1) | Start Bit (0) |
|---|---|---|---|---|
| 256K x 36 | xxxx | 0000 0000 0100 0011 | 0000 1110 001 | 1 |
| 512K x 18 | xxxx | 0000 0000 0100 0100 | 0000 1110 001 | 1 |

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, the LSB serially shifts data out through TDO. However, unlike the Instruction Register and the other Data Registers, TDI does not serially shift data into the MSB. The ID Register is a “read-only” register.

**Bypass Register (1 bit)**

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic "0" when the BYPASS instruction has been loaded in the the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

**Boundary Scan Register (68 bits for x36, 49 bits for x18)**

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for density and/or functional upgrades. The Boundary Scan Register is loaded with the contents of the SRAM's I/O ring when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

The Boundary Scan Register contains the following bits:

| 256K x 36 | | 512K x 18 | |
|---|---|---|---|
| DQ | 36 | DQ | 18 |
| SA, SA1, SA0 | 18 | SA, SA1, SA0 | 19 |
| CK, $\overline{CK}$ | 2 | CK, $\overline{CK}$ | 2 |
| CQ, $\overline{CQ}$ | 4 | CQ, $\overline{CQ}$ | 2 |
| B1, B2, B3 | 3 | B1, B2, B3 | 3 |
| $\overline{G}$ | 1 | $\overline{G}$ | 1 |
| $\overline{LBO}$ | 1 | $\overline{LBO}$ | 1 |
| ZQ | 1 | ZQ | 1 |
| Place Holder | 2 | Place Holder | 2 |

For deterministic results, all signals composing the SRAM's I/O ring must meet setup and hold times with respect to TCK (same as TDI and TMS) when sampled.

CK/$\overline{CK}$ are connected to a differential input receiver that generates a single-ended input clock signal to the device. Therefore, in order to capture specific values for these signals in the Boundary Scan Register, these signals must be at opposite logic levels when sampled.

Place Holders are required for some NC pins to allow for future density and/or functional upgrades. They are connected to $V_{DD}$ internally, regardless of pin connection externally.

The Boundary Scan Order Assignment tables on the following page depict the order in which the bits from the table above are arranged in the Boundary Scan Register. In each notation, Bit 1 is the LSB bit of the register. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

## Boundary Scan Order Assignments (By Exit Sequence)

**256K x 36**

| Bit | Signal | Pad | Bit | Signal | Pad |
|---|---|---|---|---|---|
| 1 | SA1 | 5R | 35 | SA | 6A |
| 2 | SA0 | 5T | 36 | SA | 4A |
| 3 | SA | 6R | 37 | SA | 4C |
| 4 | SA | 7T | 38 | SA | 3A |
| 5 | SA | 7P | 39 | SA | 3B |
| 6 | DQ | 8T | 40 | SA | 3C |
| 7 | DQ | 9T | 41 | NC (1) | 3D |
| 8 | DQ | 8P | 42 | DQ | 2B |
| 9 | DQ | 7M | 43 | DQ | 1B |
| 10 | DQ | 9P | 44 | DQ | 2D |
| 11 | $\overline{CQ}$ | 8M | 45 | DQ | 3F |
| 12 | DQ | 9M | 46 | DQ | 1D |
| 13 | DQ | 7K | 47 | CQ | 2F |
| 14 | DQ | 8K | 48 | DQ | 1F |
| 15 | DQ | 9K | 49 | DQ | 3H |
| 16 | NC (1) | 6L | 50 | DQ | 2H |
| 17 | $\overline{CK}$ | 5H | 51 | DQ | 1H |
| 18 | CK | 5G | 52 | ZQ | 5A |
| 19 | $\overline{G}$ | 5C | 53 | B1 | 5B |
| 20 | DQ | 9H | 54 | B2 | 5K |
| 21 | DQ | 8H | 55 | B3 | 5L |
| 22 | DQ | 7H | 56 | $\overline{LBO}$ | 4L |
| 22 | DQ | 9F | 57 | DQ | 1K |
| 24 | CQ | 8F | 58 | DQ | 2K |
| 25 | DQ | 9D | 59 | DQ | 3K |
| 26 | DQ | 7F | 60 | DQ | 1M |
| 27 | DQ | 8D | 61 | $\overline{CQ}$ | 2M |
| 28 | DQ | 9B | 62 | DQ | 1P |
| 29 | DQ | 8B | 63 | DQ | 3M |
| 30 | SA | 7D | 64 | DQ | 2P |
| 31 | SA | 7C | 65 | DQ | 1T |
| 32 | SA | 7B | 66 | DQ | 2T |
| 33 | SA | 7A | 67 | SA | 3T |
| 34 | SA | 6C | 68 | SA | 4R |

**512K x 18**

| Bit | Signal | Pad | Bit | Signal | Pad |
|---|---|---|---|---|---|
| 1 | SA1 | 5R | 35 | DQ | 3H |
| 2 | SA0 | 5T | 36 | DQ | 1H |
| 3 | SA | 6R | 37 | ZQ | 5A |
| 4 | SA | 7T | 38 | B1 | 5B |
| 5 | SA | 7P | 39 | B2 | 5K |
| 6 | DQ | 8T | 40 | B3 | 5L |
| 7 | DQ | 9P | 41 | $\overline{LBO}$ | 4L |
| 8 | $\overline{CQ}$ | 8M | 42 | DQ | 2K |
| 9 | DQ | 7K | 43 | DQ | 1M |
| 10 | DQ | 9K | 44 | DQ | 3M |
| 11 | NC (1) | 6L | 45 | DQ | 2P |
| 12 | $\overline{CK}$ | 5H | 46 | DQ | 1T |
| 13 | CK | 5G | 47 | SA | 3P |
| 14 | $\overline{G}$ | 5C | 48 | SA | 3T |
| 15 | DQ | 8H | 49 | SA | 4R |
| 16 | DQ | 9F | 50 | | |
| 17 | DQ | 7F | 51 | | |
| 18 | DQ | 8D | 52 | | |
| 19 | DQ | 9B | 53 | | |
| 20 | SA | 7D | 54 | | |
| 21 | SA | 7C | 55 | | |
| 22 | SA | 7B | 56 | | |
| 22 | SA | 7A | 57 | | |
| 24 | SA | 6C | 58 | | |
| 25 | SA | 6A | 59 | | |
| 26 | SA | 4A | 60 | | |
| 27 | SA | 4C | 61 | | |
| 28 | SA | 3A | 62 | | |
| 29 | SA | 3B | 63 | | |
| 30 | SA | 3C | 64 | | |
| 31 | NC (1) | 3D | 65 | | |
| 32 | DQ | 2B | 66 | | |
| 33 | DQ | 1D | 67 | | |
| 34 | CQ | 2F | 68 | | |

Note 1: NC pins at pad locations 6L and 3D are connected to $V_{DD}$ internally, regardless of pin connection externally.

## TAP Instructions

**IDCODE**

The IDCODE instruction causes a predetermined device- and manufacturer-specific identification code to be loaded into the ID Register when the TAP Controller is in the "Capture-DR" state, and causes the ID Register to be inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state. IDCODE is the default instruction loaded into the Instruction Register at power-up, and when the TAP Controller is in the "Test-Logic Reset" state.

**BYPASS**

The BYPASS instruction causes a logic "0" to be loaded into the Bypass Register when the TAP Controller is in the "Capture-DR" state, and causes the Bypass Register to be inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

**SAMPLE**

The SAMPLE instruction causes the logic levels of the signals composing the SRAM's I/O ring (see the Boundary Scan Register description for the complete list of signals) to be loaded into the Boundary Scan Register when the TAP Controller is in the "Capture-DR" state, and causes the Boundary Scan Register to be inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

The SAMPLE instruction does NOT affect the state of the SRAM's clock output drivers (CQs). They behave exactly as they do during normal SRAM operation. Specifically, the CQs remain in a Low-Z (output) state during this instruction, and are logically equivalent to the SRAM's clock inputs (CKs).

The SAMPLE instruction does NOT affect the state of the SRAM's data output drivers (DQs). They behave exactly as they do during normal SRAM operation. Specifically, the DQs remain in either a High-Z (input) state or Low-Z (output) state during this instruction, depending on when the instruction is executed, as follows:

| SAMPLE Executed After | and | State of $\overline{G}$ | then | State of DQs |
|---|---|---|---|---|
| Power-Up | | X | | High-Z (Input) |
| Read Operation | | L | | Low-Z (Output - Drive most recent read data) |
| | | H | | High-Z (Input) |
| Write Operation | | X | | High-Z (Input) |
| Deselect Operation | | X | | High-Z (Input) |

**SAMPLE-Z**

Like the SAMPLE instruction, the SAMPLE-Z instruction causes the logic levels of the signals composing the SRAM's I/O ring (see the Boundary Scan Register description for the complete list of signals) to be loaded into the Boundary Scan Register when the TAP Controller is in the "Capture-DR" state, and causes the Boundary Scan Register to be inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

However, unlike the SAMPLE instruction, the SAMPLE-Z instruction DOES affect the state of the SRAM's clock (CQ) and data (DQ) output drivers. Specifically, the CQs and DQs are forced to a High-Z (input) state during this instruction, allowing an external source to drive these signals without bus contention.

## TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction (see Figure 8). State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the "Test-Logic Reset" state in one of two ways:

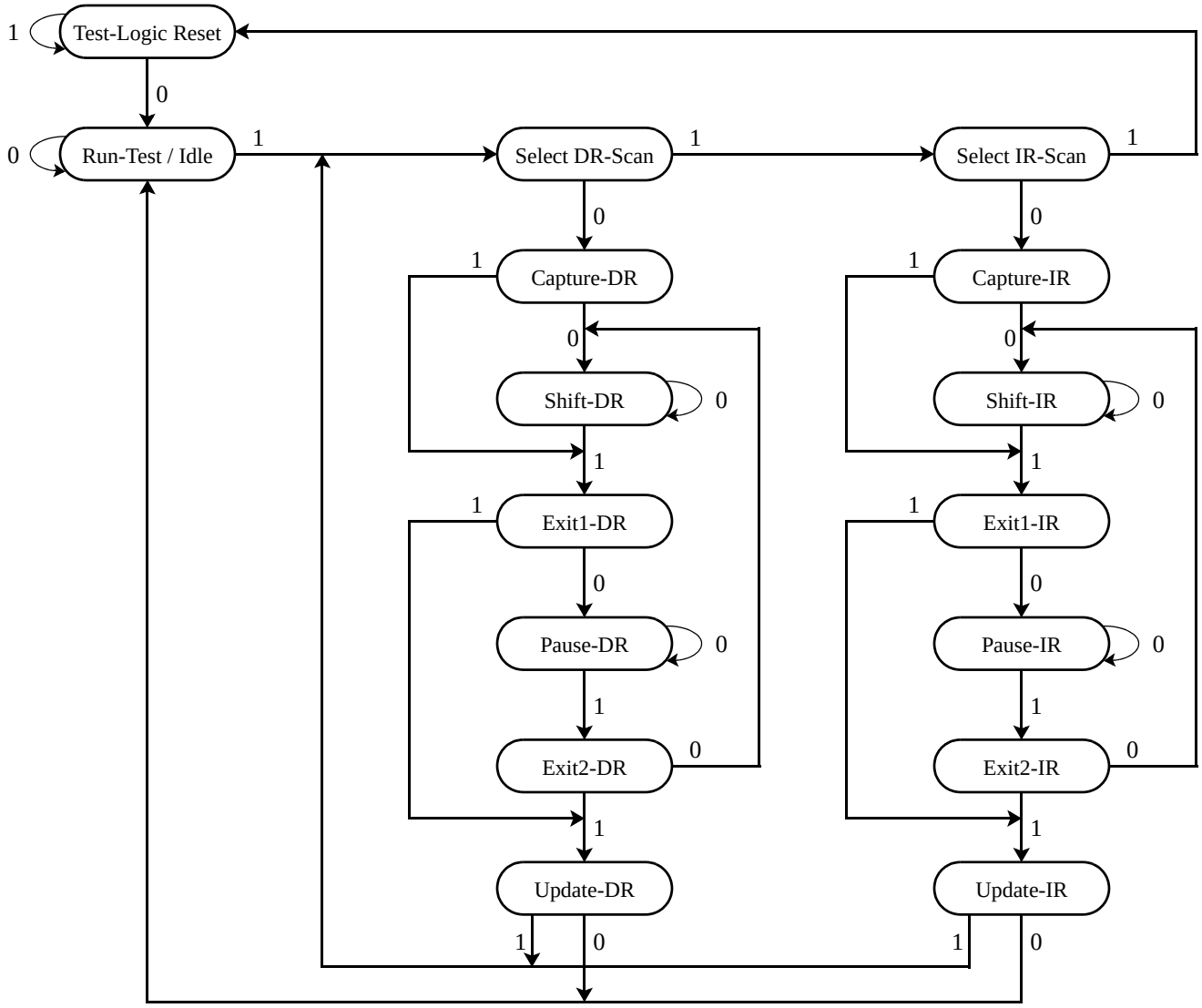
1. At power up.
2. When a logic "1" is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the "Shift-IR" state or the "Shift-DR" state.

The TDO output driver is active only when the TAP Controller is in either the "Shift-IR" state or the "Shift-DR" state.

## TAP Controller State Diagram

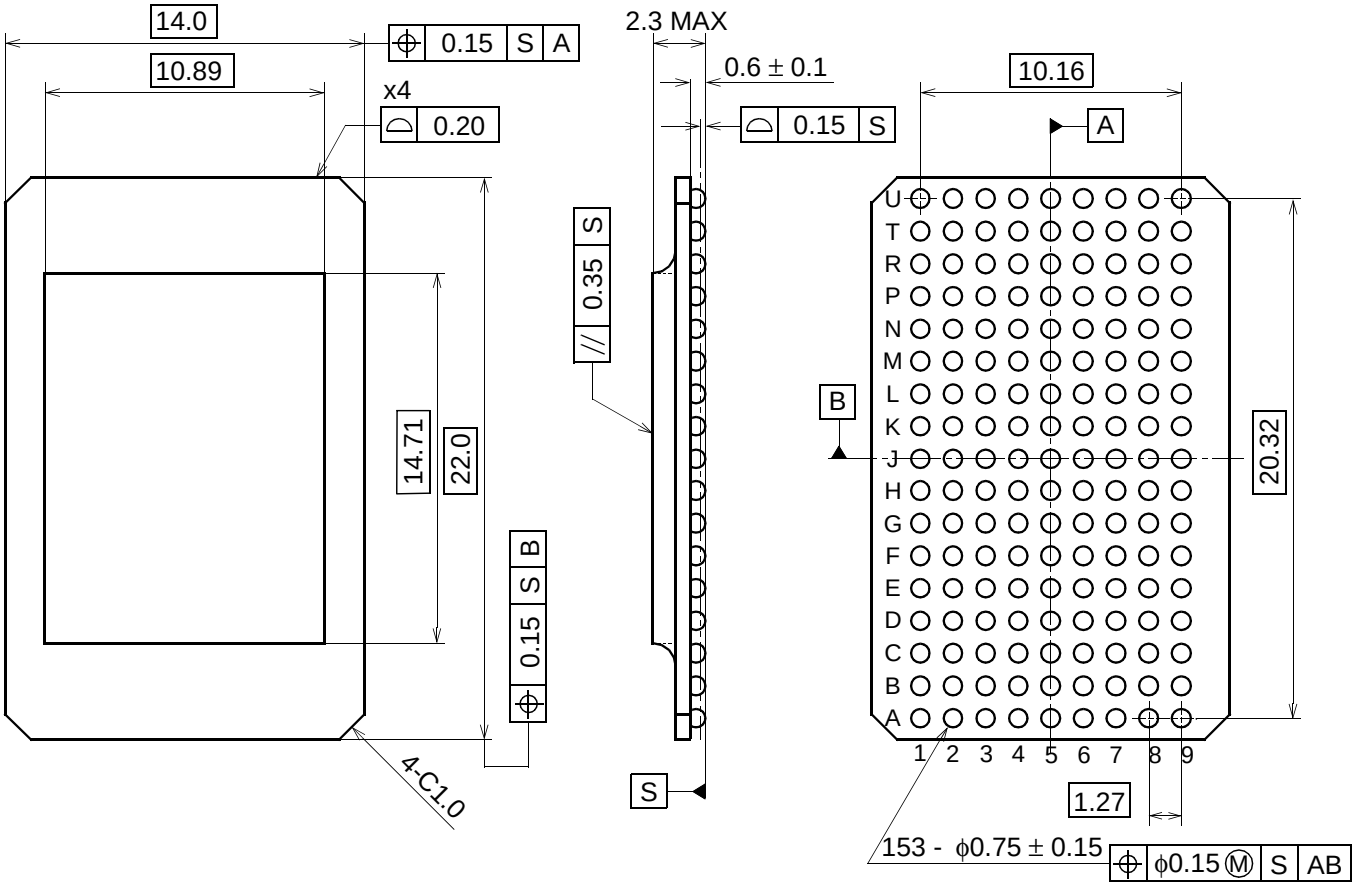
**Figure 8**



## •Ordering Information

| Part Number | $V_{DD}$ | I/O Type | Size | Speed (Cycle / Data Access Time) |
|---|---|---|---|---|
| CXK77R3682AGB-35 | 2.5V | HSTL | 256K x 36 | 3.5ns / 2.2ns |
| CXK77R3682AGB-39A<br>CXK77R3682AGB-39 | 2.5V | HSTL | 256K x 36 | 3.9ns / 2.4ns<br>3.9ns / 2.6ns |
| CXK77R3682AGB-42 | 2.5V | HSTL | 256K x 36 | 4.2ns / 2.6ns |
| CXK77R1882AGB-35 | 2.5V | HSTL | 512K x 18 | 3.5ns / 2.2ns |
| CXK77R1882AGB-39A<br>CXK77R1882AGB-39 | 2.5V | HSTL | 512K x 18 | 3.9ns / 2.4ns<br>3.9ns / 2.6ns |
| CXK77R1882AGB-42 | 2.5V | HSTL | 512K x 18 | 4.2ns / 2.6ns |

# (9x17) 153 Pin BGA Package Dimensions




PRELIMINARY

| | |
|---|---|
| SONY CODE | BGA-153P-021 |
| EIAJ CODE | BGA153-P-1422 |
| JEDEC CODE | ———— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| BORAD TREATMENT | COPPER-CLAD LAMINATE |
| LEAD MATERIAL | SOLDER |
| PACKAGE MASS | 1.4g |

## •Revision History

| Rev. # | Rev. Date | Description of Modifications |
|---|---|---|
| rev 0.0 | 09/03/99 | Initial Version. |
| rev 1.0 | 10/29/99 | 1. Modified DC Recommended Operating Conditions (p. 8).<br>$V_{MIH}$ (min) $V_{REF}$ + 0.1V to $V_{REF}$ + 0.3V<br>$V_{MIL}$ (max) $V_{REF}$ - 0.1V to $V_{REF}$ - 0.3V<br>$V_{IH}$ (max) AC (note 2) +3.5V to +3.3V<br>$V_{IL}$ (min) AC (note 3) -1.5V to -1.1V<br>$V_{IH}$ (max) AC and $V_{IL}$ (min) AC Duration (max) (notes 2,3) 1ns to ($t_{CYC}$ / 4)<br>Removed Output Impedance Control Resistor (RQ) specifications.<br>2. Modified DC Electrical Characteristics (p. 9).<br>Updated max and typ Average Power Supply Operating Currents ($I_{DD}$).<br>Updated max and typ Power Supply Deselect Operating Current ($I_{DD2}$).<br>Updated max and typ Average Power Supply Operating Current at 3 MHz ($I_{DD3}$).<br>Updated Output Driver Impedance - specified pull-up and pull-down min, typ, and max $R_{OUT}$ output impedance per various RQ impedance control resistor values.<br>3. Modified AC Timing Characteristics (p. 11).<br>Added sub-bin “A” to “-39” bin.<br>-35 $t_{AVKH}$, $t_{BVKH}$ 0.5ns to 0.4ns<br>4. Updated Package Drawing (p. 27). |
| rev 1.1 | 12/10/99 | 1. Modified DC Electrical Characteristics (p. 9).<br>Updated “-31” max and typ Average Power Supply Operating Currents ($I_{DD-31}$).<br>Updated “-31” max and typ Power Supply Deselect Operating Current ($I_{DD2-31}$).<br>Updated Output Driver Impedance - combined separate pull-up and pull-down specifications, and changed accuracy from (RQ/5) ± 15% to (RQ/5) ± 10%.<br>2. Modified AC Timing Characteristics (p. 11).<br>Changed “-3” bin to “-31” bin.<br>-31 $t_{KHKL}$, $t_{KLKH}$ 1.2ns to 1.3ns<br>$t_{KHAX}$, $t_{KHBX}$ 0.4ns to 0.5ns<br>$t_{DVKH}$, $t_{DVKL}$, $t_{KHDX}$, $t_{KLDX}$ 0.35ns to 0.4ns<br>$t_{KXCH}$, $t_{KXCL}$ 1.8ns to 1.9ns<br>$t_{KHQZ}$ 1.9ns to 2.0ns<br>-33 $t_{KHAX}$, $t_{KHBX}$ 0.4ns to 0.5ns<br>$t_{DVKH}$, $t_{DVKL}$, $t_{KHDX}$, $t_{KLDX}$ 0.35ns to 0.4ns |
| rev 1.2 | 08/25/00 | 1. Added BGA Package Thermal Characteristics (p. 7).<br>Junction to Case Temperature ($\Theta_{JC}$) 1.0 °C/W<br>2. Modified DC Recommended Operating Conditions (p. 8).<br>Removed Clock Input Cross Point Voltage ($V_X$) specification.<br>3. Modified DC Electrical Characteristics (p. 9).<br>Removed $I_{DD-31}$, $I_{DD-33}$, $I_{DD2-31}$, and $I_{DD2-33}$, (typ and max) specifications.<br>Added x36 $I_{DD-42}$ (typ and max) 720mA / 840mA<br>Added x18 $I_{DD-42}$ (typ and max) 660mA / 770mA<br>Added $I_{DD2-42}$ (typ and max) 340mA / 400mA<br>Removed $I_{DD3}$ (typ and max) specifications.<br>$V_{OH}$ (min) $I_{OH}$ test condition -8.0mA at RQ = 125Ω to -4.0mA at RQ = 250Ω<br>$V_{OL}$ (max) $I_{OL}$ test condition 8.0mA at RQ = 125Ω to 4.0mA at RQ = 250Ω<br>Added Note 3 regarding $R_{OUT}$ that states “This parameter is guaranteed by design through extensive corner lot characterization”. |

| Rev. # | Rev. Date | Description of Modifications |
|---|---|---|
| rev 1.2 | 08/25/00 | 4. Modified AC Electrical Characteristics (p. 10).<br>Removed "-31" and "-33" bins. Added "-42" bin.<br>Indicated that $t_{GVKH}$ and $t_{KHGX}$ are sampled and not 100% tested.<br>Added $t_{KHQV}$ (max) and $t_{KLQV}$ (max) specifications.<br>Added $t_{KHQX}$ (min) and $t_{KLQX}$ (min) specifications.<br>Removed $t_{CHQZ}$ (min) specifications.<br>5. Added note to Disabling the TAP section that states that TAP operation does not interfere with normal SRAM operation except during the SAMPLE-Z instruction (p. 18).<br>6. Modified JTAG DC Recommended Operating Conditions (p. 18).<br>$V_{TOH}$ (min) 1.9V to 2.0V<br>$I_{TLI}$ (min/max) at $V_{TIN} = V_{SS}$ to $V_{DD}$ ±1uA to ±10uA |