8Mb Late Write HSTL High Speed Synchronous SRAMs (256K x 36 or 512K x 18 Organization) **Preliminary**

Description

The CXK77S36R80AGB (organized as 262,144 words by 36 bits) and the CXK77S18R80AGB (organized as 524,288 words by 18 bits) are high speed CMOS synchronous static RAMs with common I/O pins. These synchronous SRAMs integrate input registers, high speed RAM, output registers, and a one-deep write buffer onto a single monolithic IC. Register - Register (R-R) read operations and Late Write (LW) are supported, providing a high-performance user interface.

All address and control input signals except $\overline{G}$ (Output Enable) and ZZ (Sleep Mode) are registered on the rising edge of K (Input Clock).

During read operations, output data is driven valid from the rising edge of K, one full clock cycle after the address is registered.

During write operations, input data is registered on the rising edge of K, one full clock cycle after the address is registered.

The output drivers are series terminated, and the output impedance is programmable through an external impedance matching resistor RQ. By connecting RQ between ZQ and V_{SS}, the output impedance of all DQ pins can be precisely controlled.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 300 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

Features

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3 Speed Bins	Cycle Time / Access Time
-33 (-33A)	3.3ns / 1.7ns (1.6ns)
-36	3.6ns / 1.8ns
-4 (-4A)	4.0ns / 2.0ns (1.8ns)

- Single 3.3V power supply (V_{DD}): 3.3V ± 5%
- Register - Register (R-R) read operations
- Late Write (LW), fully coherent write operations
- Byte Write capability
- Two cycle deselect
- Differential input clocks (K/$\overline{K}$)
- Asynchronous output enable ($\overline{G}$)
- Dedicated output supply voltage (V_{DDQ}): 1.4V (min) to 2.0V (max)
- HSTL-compatible I/O interface with dedicated input reference voltage (V_{REF}): V_{DDQ}/2 typical
- Programmable impedance output drivers
- Sleep (power down) mode via dedicated mode pin (ZZ)
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 119 pin (7x17), 1.27mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

256K x 36 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC (2)	SA	NC	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBW}$c	NC	$\overline{SBW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBW}$d	$\overline{K}$	$\overline{SBW}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	M1 (4)	V_{DD}	M2 (5)	SA	NC
T	NC	NC (1)	SA	SA	SA	NC (1)	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	RSVD (3)	V_{DDQ}

Notes:

1. Pad Locations 2T and 6T are true no-connects. However, they are defined as SA address inputs in x18 LW SRAMs.
2. Pad Location 2B is a true no-connect. However, it is defined as an SA address input in 16Mb LW SRAMs.
3. Pad Location 6U must be left unconnected. It is used by Sony for internal test purposes.
4. Pad Location 3R is defined as an M1 mode pin in LW SRAMs. However, it must be tied “low” in this device.
5. Pad Location 5R is defined as an M2 mode pin in LW SRAMs. However, it must be tied “high” in this device.

512K x 18 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC (2)	SA	NC	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC (1b)	V_{SS}	ZQ	V_{SS}	DQa	NC (1b)
E	NC (1b)	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC (1b)	DQa
F	V_{DDQ}	NC (1b)	V_{SS}	$\overline{G}$	V_{SS}	DQ6a	V_{DDQ}
G	NC (1b)	DQb	$\overline{SBW}$b	NC	V_{SS}	NC (1b)	DQa
H	DQb	NC (1b)	V_{SS}	NC	V_{SS}	DQa	NC (1b)
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC (1b)	DQb	V_{SS}	K	V_{SS}	NC (1b)	DQa
L	DQb	NC (1b)	V_{SS}	$\overline{K}$	$\overline{SBW}$a	DQa	NC (1b)
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC (1b)	V_{DDQ}
N	DQb	NC (1b)	V_{SS}	SA	V_{SS}	DQa	NC (1b)
P	NC (1b)	DQb	V_{SS}	SA	V_{SS}	NC (1b)	DQa
R	NC	SA	M1 (4)	V_{DD}	M2 (5)	SA	NC
T	NC	SA	SA	NC (1a)	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	RSVD (3)	V_{DDQ}

Notes:

1a. Pad Location 4T is a true no-connect. However, it is defined as an SA address input in x36 LW SRAMs.

1b. Pad Locations 2D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 7L, 6M, 2N, 7N, 1P, and 6P are true no-connects. However, they are defined as DQ data inputs / outputs in x36 LW SRAMs.

2. Pad Location 2B is a true no-connect. However, it is defined as an SA address input in 16Mb LW SRAMs.

3. Pad Location 6U must be left unconnected. It is used by Sony for internal test purposes.

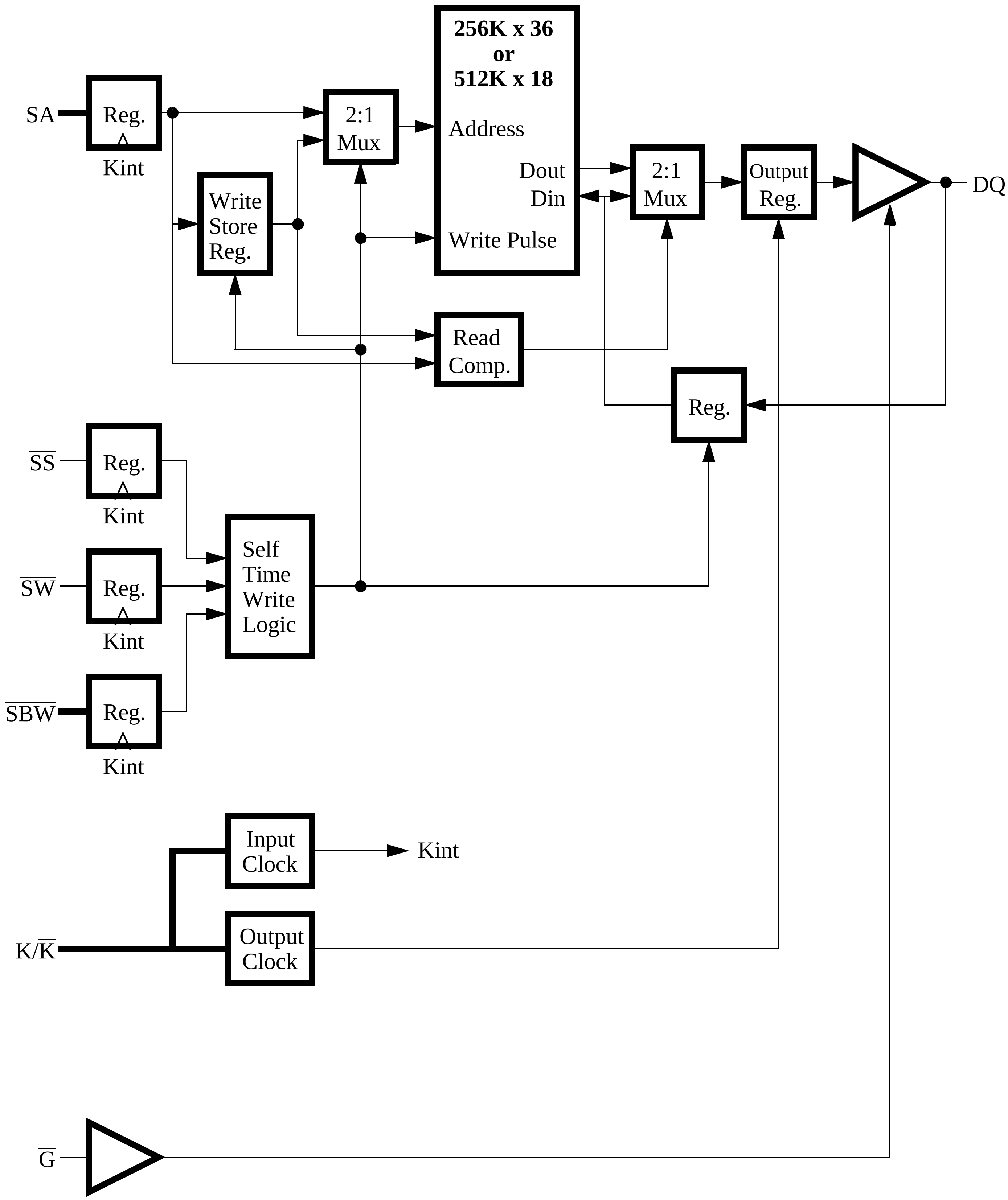
4. Pad Location 3R is defined as an M1 mode pin in LW SRAMs. However, it must be tied “low” in this device.

5. Pad Location 5R is defined as an M2 mode pin in LW SRAMs. However, it must be tied “high” in this device.

Pin Description

Symbol	Type	Description
SA	Input	Synchronous Address Inputs - Registered on the rising edge of K.
DQa, DQb DQc, DQd	I/O	Synchronous Data Inputs / Outputs - Registered on the rising edge of K during write operations. Driven from the rising edge of K during read operations. DQa - indicates Data Byte a DQb - indicates Data Byte b DQc - indicates Data Byte c DQd - indicates Data Byte d
K, $\overline{K}$	Input	Differential Input Clocks
$\overline{SS}$	Input	Synchronous Select Input - Registered on the rising edge of K. $\overline{SS}$ = 0 specifies a write operation when $\overline{SW}$ = 0 specifies a read operation when $\overline{SW}$ = 1 $\overline{SS}$ = 1 specifies a deselect operation
$\overline{SW}$	Input	Synchronous Global Write Enable Input - Registered on the rising edge of K. $\overline{SW}$ = 0 specifies a write operation when $\overline{SS}$ = 0 $\overline{SW}$ = 1 specifies a read operation when $\overline{SS}$ = 0
$\overline{SBW}$a, $\overline{SBW}$b, $\overline{SBW}$c, $\overline{SBW}$d	Input	Synchronous Byte Write Enable Inputs - Registered on the rising edge of K. $\overline{SBW}$a = 0 specifies write Data Byte a when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$b = 0 specifies write Data Byte b when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$c = 0 specifies write Data Byte c when $\overline{SS}$ = 0 and $\overline{SW}$ = 0 $\overline{SBW}$d = 0 specifies write Data Byte d when $\overline{SS}$ = 0 and $\overline{SW}$ = 0
$\overline{G}$	Input	Asynchronous Output Enable Input - De-asserted (high) forces the data output drivers to Hi-Z.
ZZ	Input	Asynchronous Sleep Mode Input - Asserted (high) forces the SRAM into low-power mode.
M1, M2	Input	Read Operation Protocol Select - These mode pins must be tied “low” and “high” respectively to select Register - Register read operations.
ZQ	Input	Output Impedance Control Resistor Input
V_{DD}		3.3V Core Power Supply - Core supply voltage.
V_{DDQ}		Output Power Supply - Output buffer supply voltage.
V_{REF}		Input Reference Voltage - Input buffer threshold voltage.
V_{SS}		Ground
TCK	Input	JTAG Clock
TMS	Input	JTAG Mode Select
TDI	Input	JTAG Data In
TDO	Output	JTAG Data Out
RSVD		Reserved - This pin is used for Sony test purposes only. It must be left unconnected.
NC		No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V_{DD}, V_{DDQ}, or V_{SS}.

BLOCK DIAGRAM



•Clock Truth Table

K	ZZ	$\overline{SS}$ (t_n)	$\overline{SW}$ (t_n)	$\overline{SBW}x$ (t_n)	$\overline{G}$	Operation	DQ (t_n)	DQ (t_{n+1})
X	H	X	X	X	X	Sleep (Power Down) Mode	Hi - Z	Hi - Z
L→H	L	H	X	X	X	Deselect	X	Hi - Z
L→H	L	L	H	X	H	Read	Hi - Z	Hi - Z
L→H	L	L	H	X	L	Read	X	Q(t_n)
L→H	L	L	L	L	X	Write All Bytes	X	D(t_n)
L→H	L	L	L	X	X	Write Bytes With $\overline{SBW}x$ = L	X	D(t_n)
L→H	L	L	L	H	X	Abort Write	X	Hi - Z

•Sleep (Power Down) Mode

Sleep (power down) mode is provided through the asynchronous input signal ZZ. When ZZ is asserted (high), the output drivers will go to a Hi-Z state, and the SRAM will begin to draw standby current. Contents of the memory array will be preserved. An enable time (t_{ZZE}) must be met before the SRAM is guaranteed to be in sleep mode, and a recovery time (t_{ZZR}) must be met before the SRAM can resume normal operation.

•Programmable Impedance Output Drivers

These devices have programmable impedance output drivers. The output impedance is controlled by an external resistor, RQ, connected between the SRAM's ZQ pin and V_{SS}, and is equal to one-fifth the value of this resistor, nominally. See the DC Electrical Characteristics section for further information.

The output impedance is updated whenever the output drivers are in a Hi-Z state. Consequently, impedance updates will occur during write and deselect operations, and when $\overline{G}$ is deasserted (high) (see **Note 1** below). At power up, 8192 clock cycles followed by an impedance update via one of the three methods described above are required to ensure that the output impedance has reached the desired value. After power up, periodic impedance updates via one of the three methods described above are also required to ensure that the output impedance remains within specified tolerances.

Note 1: In order to allow the SRAM sufficient time to update the output impedance when $\overline{G}$ is deasserted (high), $\overline{G}$ must meet setup and hold times with respect to K clock. See the AC Electrical Characteristics sections for further information.

•Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs. V_{DDQ} should never exceed V_{DD}. If this power supply sequence cannot be met, a large bypass diode may be required between V_{DD} and V_{DDQ}. Please contact Sony Memory Application Department for further information.

•Absolute Maximum Ratings[1]

Item	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.5 to +3.9	V
Output Supply Voltage	V_{DDQ}	-0.5 to +3.6	V
Input Voltage (Address, Control, Data, Clock)	V_{IN}	-0.5 to V_{DDQ} + 0.5 (2.6V max.)	V
Input Voltage (TCK, TMS, TDI)	V_{TIN}	see p. 14 “JTAG DC Recommended Operating Conditions”	V
Operating Temperature	T_A	0 to 85	°C
Junction Temperature	T_J	0 to 110	°C
Storage Temperature	T_{STG}	-55 to 150	°C

(1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

•BGA Package Thermal Characteristics

Item	Symbol	Rating	Unit
Junction to Case Temperature	Θ_{JC}	1.0	°C/W

•I/O Capacitance

(T_A = 25°C, f = 1 MHz)

Item		Symbol	Test conditions	Min	Max	Unit
Input Capacitance	Address	C_{ADDR}	V_{IN} = 0V	---	3.0	pF
	Control	C_{CTRL}	V_{IN} = 0V	---	3.5	pF
	Clock	C_{CLK}	V_{IN} = 0V	---	3.5	pF
Output Capacitance		C_{OUT}	V_{OUT} = 0V	---	4.5	pF

Note: These parameters are sampled and are not 100% tested.

•DC Recommended Operating Conditions

(V_{SS} = 0V, T_A = 0 to 85°C)

Item	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage	V_{DD}	3.13	3.3	3.47	V	1
Output Supply Voltage	V_{DDQ}	1.4	---	2.0	V	
Input Reference Voltage	V_{REF}	0.6	---	1.0	V	2
Input High Voltage (Address, Control, Data)	V_{IH}	V_{REF} + 0.1	---	V_{DDQ} + 0.3	V	3
Input Low Voltage (Address, Control, Data)	V_{IL}	-0.3	---	V_{REF} - 0.1	V	4
Clock Input Signal Voltage	V_{KIN}	-0.3	---	V_{DDQ} + 0.3	V	5
Clock Input Differential Voltage	V_{DIF}	0.2	---	V_{DDQ} + 0.6	V	
Clock Input Common Mode Voltage	V_{CM}	0.6	---	1.0	V	
Clock Input Cross Point Voltage	V_X	0.6	---	1.0	V	

(1) V_{DD} (min) down to 2.37V is supported, but certain restrictions apply. Please contact the Sony Memory Application Department for further information.

(2) The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component.

(3) V_{IH} (max) AC = V_{DDQ} + 0.75V for pulse width less than one-quarter of the cycle time (t_{CYC}/4).

(4) V_{IL} (min) AC = -0.75V for pulse width less than one-quarter of the cycle time (t_{CYC}/4).

(5) These devices support two different input clocking schemes:

a. Differential - In this scheme, both clock inputs (K and $\overline{K}$) are driven differentially. V_{KIN}, V_{DIF}, and V_{CM} must all be considered when using this scheme.

b. Single Ended - In this scheme, one of the two clock inputs (either K or $\overline{K}$) is driven to the same voltage levels as the other inputs, i.e. from V_{SS} to V_{DDQ} nominally, while the other clock input (either $\overline{K}$ or K) is tied to an external reference voltage (V_X). V_{KIN}, V_{DIF}, and V_X must all be considered when using this scheme.

•DC Electrical Characteristics

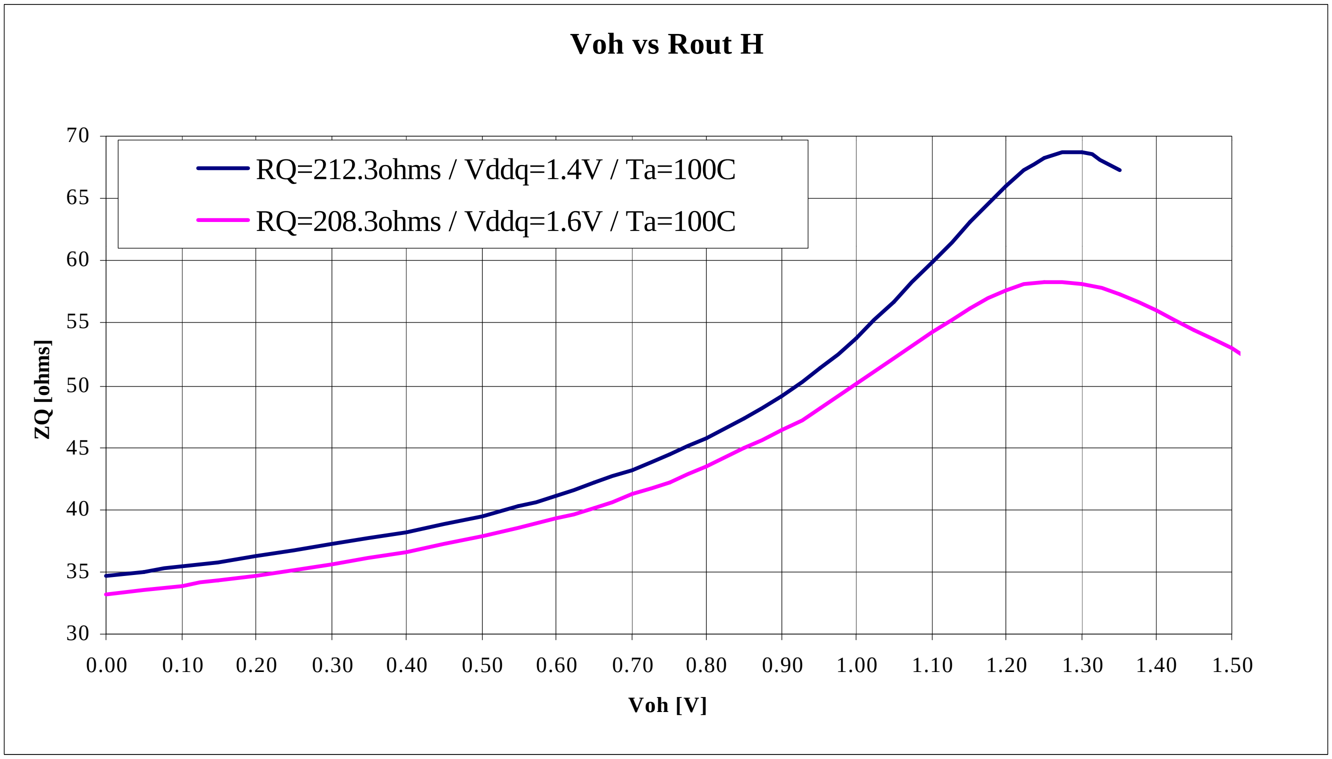
(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, T_A = 0 to 85^{o}C)

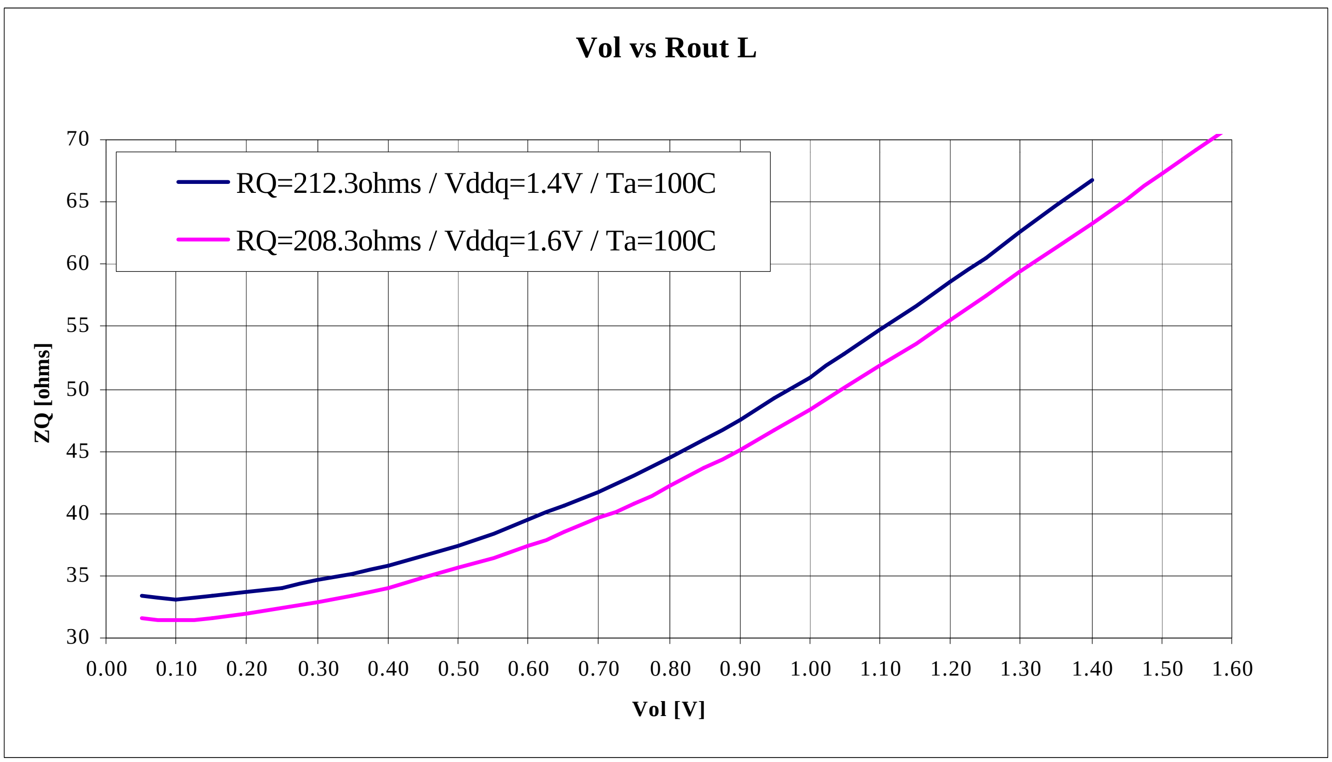
Item	Symbol	Test Conditions	Min	Typ	Max	Units	Notes
Input Leakage Current (Address, Control, Clock)	I_{LI}	$V_{IN} = V_{SS}$ to V_{DDQ}	-1	---	1	uA	
Input Leakage Current (Data)	I_{DLI}	$V_{DIN} = V_{SS}$ to V_{DDQ} $\overline{G} = V_{IH}$	-10	---	10	uA	
Average Power Supply Operating Current	I_{DD-33} I_{DD-36} I_{DD-4}	I_{OUT} = 0 mA $\overline{SS} = V_{IL}$, ZZ = V_{IL}	--- --- ---	660 620 570	750 700 650	mA	
Average Power Supply Operating Current (3 MHz Operation)	I_{DD3}	I_{OUT} = 0 mA $\overline{SS} = V_{IL}$, ZZ = V_{IL} t_{CYC} = 3 MHz	---	125	200	mA	
Power Supply Standby Current	I_{SB}	I_{OUT} = 0 mA ZZ = V_{IH}	---	40	65	mA	
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA RQ = 250Ω	V_{DDQ}-0.4	---	---	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA RQ = 250Ω	---	---	0.4	V	
Output Driver Impedance	R_{OUT}	V_{OH}, V_{OL} = V_{DDQ}/2 RQ < 150Ω	---	---	33 (30*1.1)	Ω	1,4
		V_{OH}, V_{OL} = V_{DDQ}/2 150Ω ≤ RQ ≤ 350Ω	(RQ/5)* 0.9	RQ/5	(RQ/5)* 1.1	Ω	3,4
		V_{OH}, V_{OL} = V_{DDQ}/2 RQ > 350Ω	63 (70*0.9)	---	---	Ω	2,4

1. For maximum output drive (i.e. minimum impedance), the ZQ pin can be tied directly to V_{SS}.
2. For minimum output drive (i.e. maximum impedance), the ZQ pin can be left unconnected or tied to V_{DDQ}.
3. See the following page for information on typical output driver impedance for V_{OH}/V_{OL} = 0V to 1.5V when RQ = ~210Ω.
4. This parameter is guaranteed by design through extensive corner lot characterization.

•DC Electrical Characteristics (Note)

The following diagrams describe typical output driver impedance for V_{OH}/V_{OL} = 0V to 1.5V when RQ = ~210Ω. The parameters are not guaranteed, but rather are representative of a typical device.





•AC Electrical Characteristics

Parameter	Symbol	-33		-36		-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
K Cycle Time	t_{KHKH}	3.3	---	3.6	---	4.0	---	ns	
K Clock High Pulse Width	t_{KHKL}	1.3	---	1.4	---	1.5	---	ns	
K Clock Low Pulse Width	t_{KLKH}	1.3	---	1.4	---	1.5	---	ns	
Address Setup Time	t_{AVKH}	0.3	---	0.3	---	0.3	---	ns	1
Address Hold Time	t_{KHAX}	0.7	---	0.7	---	0.7	---	ns	
Write Enables Setup Time	t_{WVKH}	0.3	---	0.3	---	0.3	---	ns	1
Write Enables Hold Time	t_{KHWX}	0.7	---	0.7	---	0.7	---	ns	
Synchronous Select Setup Time	t_{SVKH}	0.3	---	0.3	---	0.3	---	ns	1
Synchronous Select Hold Time	t_{KHSX}	0.7	---	0.7	---	0.7	---	ns	
Output Enable Setup Time	t_{GVKH}	0.5	---	0.5	---	0.5	---	ns	2,3
Output Enable Hold Time	t_{KHGX}	1.0	---	1.0	---	1.0	---	ns	2,3
Data Input Setup Time	t_{DVKH}	0.3	---	0.3	---	0.3	---	ns	1
Data Input Hold Time	t_{KHDX}	0.7	---	0.7	---	0.7	---	ns	
K Clock High to Output Valid (“A” Sub-Bin)	t_{KHQV}	---	1.7 1.6	---	1.8	---	2.0 1.8	ns	
K Clock High to Output Hold	t_{KHQX}	0.7	---	0.7	---	0.7	---	ns	3
K Clock High to Output Low-Z	t_{KHQX1}	0.5	---	0.5	---	0.5	---	ns	3,4
K Clock High to Output High-Z	t_{KHQZ}	0.7	1.8	0.7	2.0	0.7	2.0	ns	3,4
Output Enable Low to Output Valid	t_{GLQV}	---	1.8	---	2.0	---	2.0	ns	
Output Enable Low to Output Low-Z	t_{GLQX}	0.3	---	0.3	---	0.3	---	ns	3,4
Output Enable High to Output High-Z	t_{GHQZ}	---	1.8	---	2.0	---	2.0	ns	3,4
Sleep Mode Enable Time	t_{ZZE}	---	15	---	15	---	15	ns	3
Sleep Mode Recovery Time	t_{ZZR}	30	---	30	---	30	---	ns	3

All parameters are specified over the range T_A = 0 to 85°C.

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal, unless otherwise noted.

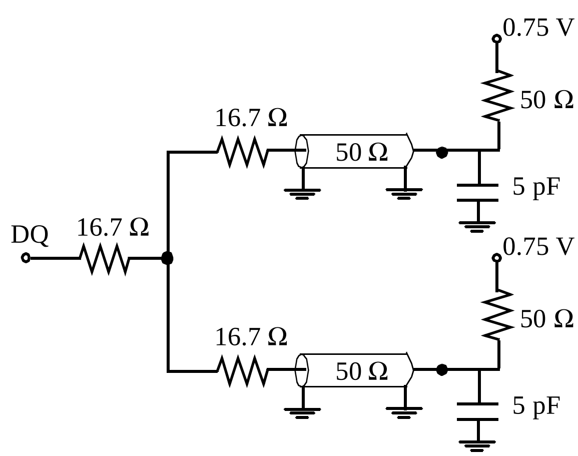
1. These parameters are measured from V_{REF} ± 200mV to the clock mid-point.
2. These parameters apply only when deasserting $\overline{G}$ (high) in order to induce output impedance updates.
3. These parameters are sampled and are not 100% tested.
4. These parameters are measured at ± 50mV from steady state voltage.

•AC Test Conditions

(V_{DD} = 3.3V ± 5%, V_{DDQ} = 1.5V ± 0.1V, T_A = 0 to 85°C)

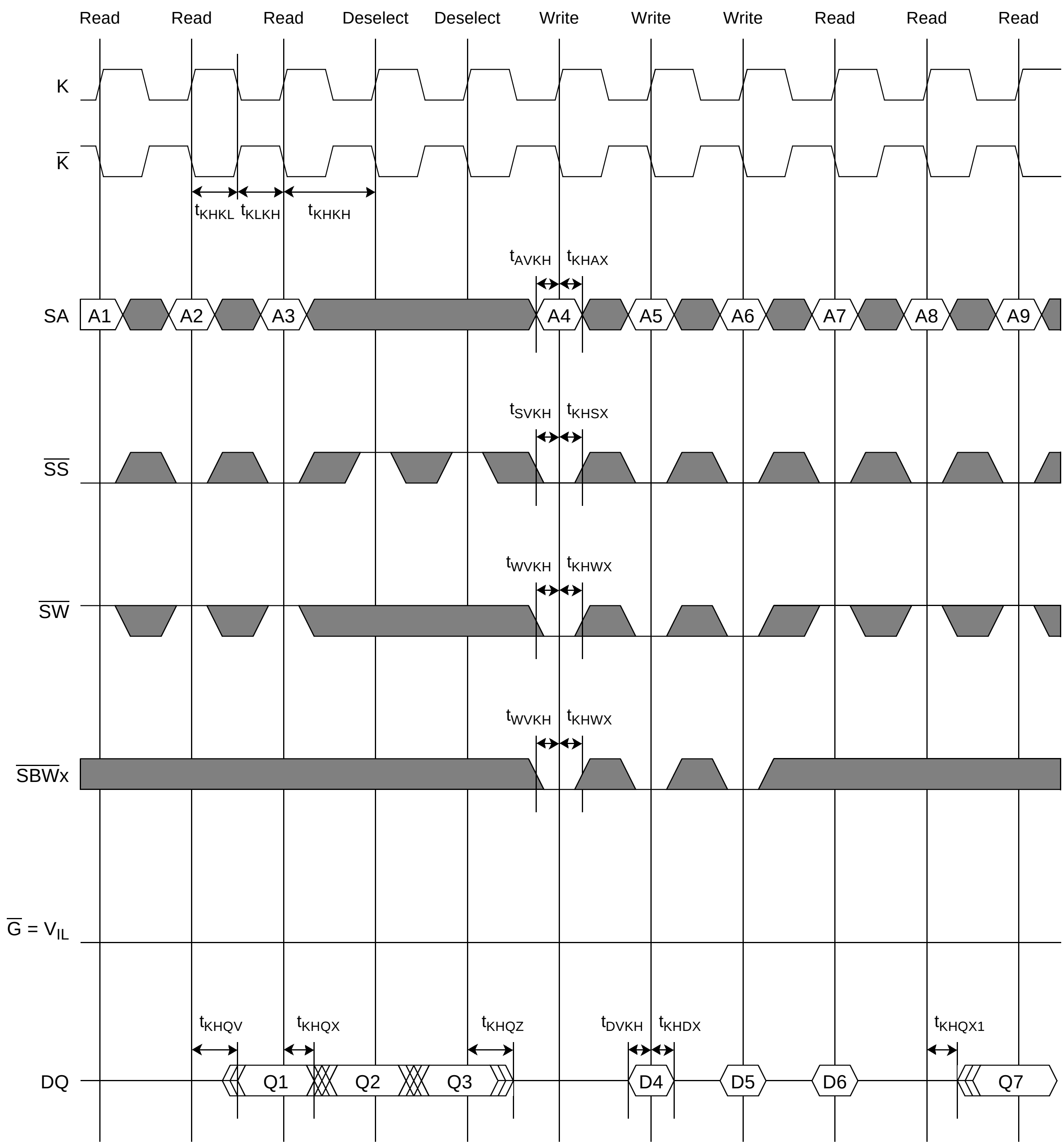
Item	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.75	V	
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Rise & Fall Time		0.5	V/ns	
Input Reference Level		0.75	V	
Clock Input High Voltage	V_{KIH}	1.25	V	$V_{DIF} \geq 0.5V$
Clock Input Low Voltage	V_{KIL}	0.25	V	$V_{DIF} \geq 0.5V$
Clock Input Common Mode Voltage	V_{CM}	0.75	V	
Clock Input Rise & Fall Time		0.5	V/ns	
Clock Input Reference Level		$K/\overline{K}$ cross	V	
Output Reference Level		0.75	V	
Output Load Conditions				Fig.1 RQ = 250Ω

Fig. 1: AC Test Output Load



Timing Diagram of Read-Write-Read Operations Synchronously Controlled via $\overline{SS}$ and Deselect Operations ($\overline{G}$ = Low)

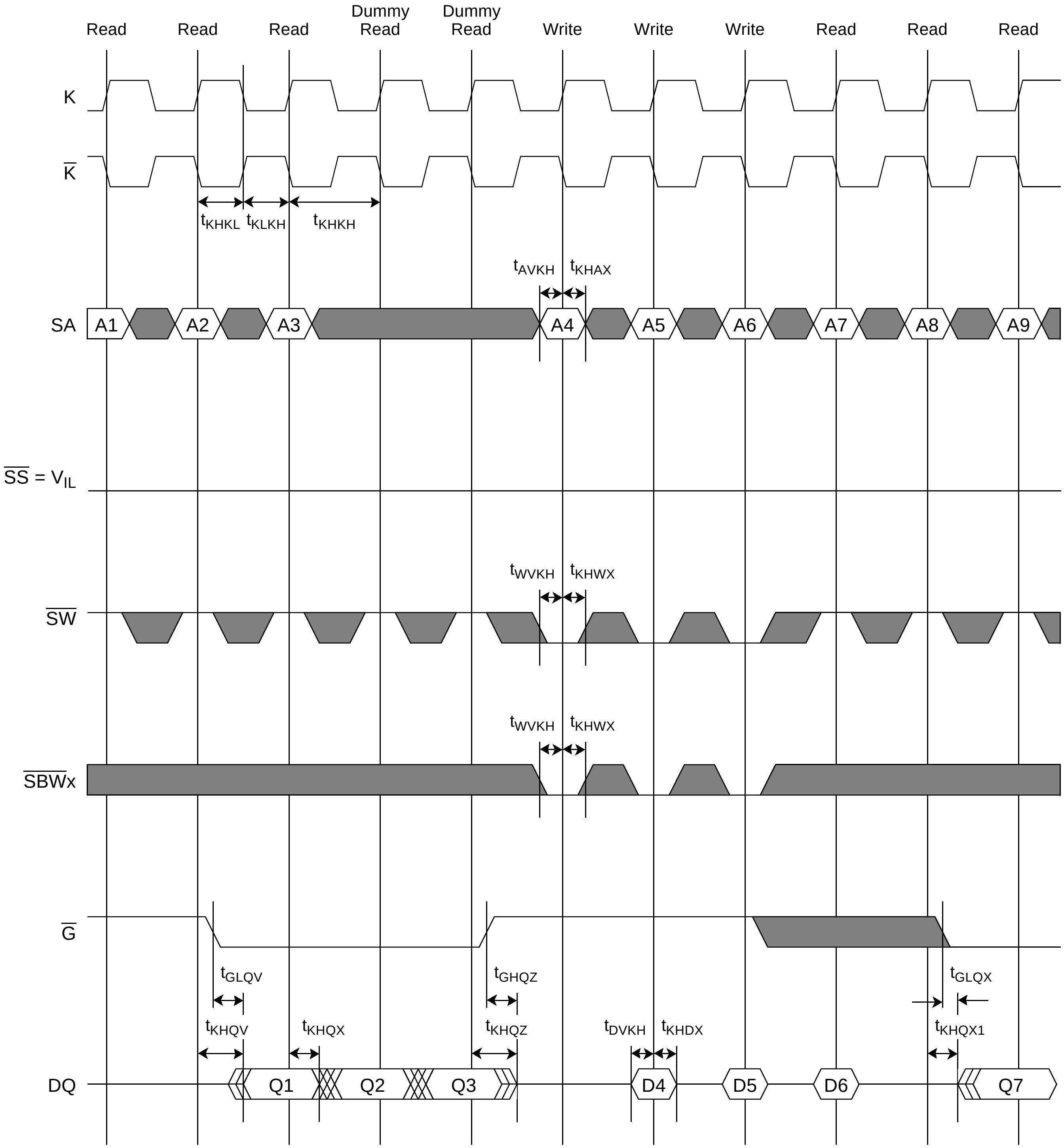
Figure 2



Note: In the diagram above, two Deselect operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Deselect operation may be sufficient.

Timing Diagram of Read-Write-Read Operations Asynchronously Controlled via $\overline{G}$ and Dummy Read Operations ($\overline{SS}$ = Low)

Figure 3



Note: In the diagram above, two Dummy Read operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Dummy Read operation may be sufficient.

•Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

TCK:	Test Clock	Induces (clocks) TAP Controller state transitions.
TMS:	Test Mode Select	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI:	Test Data In	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO:	Test Data Out	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Disabling the TAP

When JTAG is not used, TCK should be tied “low” to prevent clocking the SRAM. TMS and TDI should either be tied “low” or tied “high” through a pull-up resistor, but they cannot be left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not interfere with normal SRAM operation EXCEPT during the SAMPLE-Z instruction, which forces the SRAM’s data output drivers (DQs) to a High-Z state. Consequently, when JTAG is not used the TAP can be operated or disabled any number of ways without adversely affecting the functionality of the device.

JTAG DC Recommended Operating Conditions

(V_{DD} = 3.3V ± 5%, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Max	Units
JTAG Input High Voltage (TCK)	V_{TKIH}	---	1.7	3.15	V
JTAG Input Low Voltage (TCK)	V_{TKIL}	---	-0.3	0.7	V
JTAG Input High Voltage (TMS, TDI)	V_{TIH}	---	V_{REF} + 0.15	3.15	V
JTAG Input Low Voltage (TMS, TDI)	V_{TIL}	---	-0.3	V_{REF} - 0.15	V
JTAG Output High Voltage (TDO)	V_{TOH}	I_{TOH} = -2.0 mA	2.0	---	V
JTAG Output Low Voltage (TDO)	V_{TOL}	I_{TOL} = 2.0 mA	---	0.2	V
JTAG Input Leakage Current	I_{TLI}	V_{TIN} = 0V to 2.5V	-10	10	uA

Note 1: V_{TKIH} and V_{TIH} (max) greater than 3.15V is supported, but certain restrictions apply. An application note describing the restrictions is available on request from the Sony Memory Application Department.

Note 2: V_{TOH} is ~2.15V nominally. An application note describing how to increase V_{TOH} in order to interface with a 3.3V LVTTL receiver (via an external pull-up resistor to 3.3V) is available on request from the Sony Memory Application Department. A second application note describing how to decrease V_{TOH} in order to interface with a 1.5V HSTL receiver (via an external resistor-divider circuit) is also available on request from the Sony Memory Application Department.

JTAG AC Test Conditions

(V_{DD} = 3.3V ± 5%, T_A = 0 to 85°C)

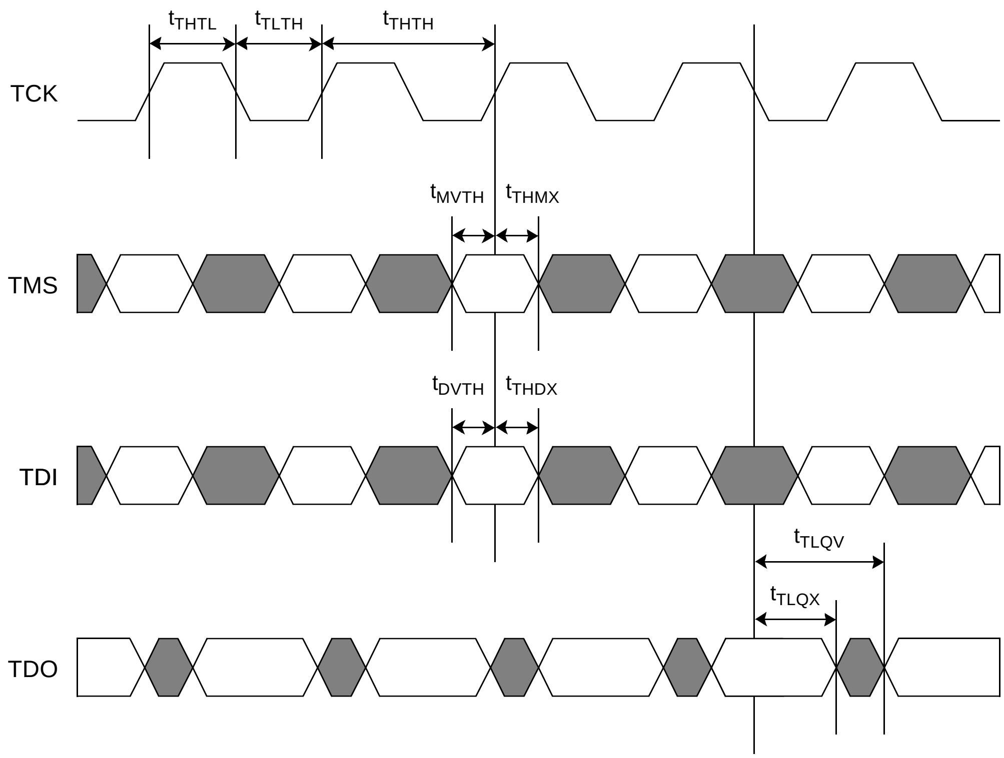
Parameter	Symbol	Conditions	Units	Notes
JTAG Input High Level	V_{TIH}	2.5	V	
JTAG Input Low Level	V_{TIL}	0.0	V	
JTAG Input Rise & Fall Time		0.5	V/ns	
JTAG Input Reference Level		1.25	V	
JTAG Output Reference Level		1.25	V	
JTAG Output Load Condition				See Fig.1 (p. 11)

JTAG AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{THTH}	100		ns
TCK High Pulse Width	t_{THTL}	40		ns
TCK Low Pulse Width	t_{TLTH}	40		ns
TMS Setup Time	t_{MVTH}	10		ns
TMS Hold TIme	t_{THMX}	10		ns
TDI Setup Time	t_{DVTH}	10		ns
TDI Hold TIme	t_{THDX}	10		ns
TCK Low to TDO Valid	t_{TLQV}		9	ns
TCK Low to TDO Hold	t_{TLQX}	0		ns

JTAG Timing Diagram

Figure 4



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: “Instruction Registers”, of which there is one- the Instruction Register, and “Data Registers”, of which there are three - the ID Register, the Bypass Register, and the Boundary Scan Register. Individual TAP registers are “selected” (inserted between TDI and TDO) when the appropriate sequence of commands is given to the TAP Controller.

Instruction Register (3 bits)

The Instruction Register stores the instructions that are executed by the TAP Controller when the TAP Controller is in the “Run-Test / Idle” state, or in any of the various “Data Register” states. It is loaded with the IDCODE instruction at power-up, or when the TAP Controller is in the “Test-Logic Reset” state or the “Capture-IR” state. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed by the TAP Controller until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	BYPASS	Inserts the Bypass Register between TDI and TDO.
001	IDCODE	Inserts the ID Register between TDI and TDO.
010	SAMPLE-Z	Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. Forces the SRAM’s outputs (DQs) to High-Z.
011	BYPASS	Inserts the Bypass Register between TDI and TDO.
100	SAMPLE	Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO.
101	PRIVATE	Do not use. Reserved for manufacturer use only.
110	BYPASS	Inserts the Bypass Register between TDI and TDO.
111	BYPASS	Inserts the Bypass Register between TDI and TDO.

Bit 0 is the LSB of the Instruction Register, and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

ID Register (32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The ID Register is 32 bits wide, and is encoded as follows:

Device	Revision Number (31:28)	Part Number (27:12)	Sony ID (11:1)	Start Bit (0)
256K x 36	xxxx	0000 0000 0100 0001	0000 1110 001	1
512K x 18	xxxx	0000 0000 0100 0010	0000 1110 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bypass Register (1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic “0” when the BYPASS instruction has been loaded in the the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

Boundary Scan Register (70 bits for x36, 51 bits for x18)

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for density and/or functional upgrades. The Boundary Scan Register is loaded with the contents of the SRAM’s I/O ring when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The Boundary Scan Register contains the following bits:

256K x 36		512K x 18	
DQ	36	DQ	18
SA	18	SA	19
K, $\overline{K}$	2	K, $\overline{K}$	2
$\overline{SS}$, $\overline{SW}$, $\overline{SBW}$x	6	$\overline{SS}$, $\overline{SW}$, $\overline{SBW}$x	4
$\overline{G}$, ZZ	2	$\overline{G}$, ZZ	2
M1, M2	2	M1, M2	2
ZQ	1	ZQ	1
Place Holder	3	Place Holder	3

For deterministic results, all signals composing the SRAM’s I/O ring must meet setup and hold times with respect to TCK (same as TDI and TMS) when sampled.

K/$\overline{K}$ are connected to a differential input receiver that generates a single-ended input clock signal to the device. Therefore, in order to capture specific values for these signals in the Boundary Scan Register, these signals must be at opposite logic levels when sampled.

Place Holders are required for some NC pins to allow for future density and/or functional upgrades. They are connected to V_{SS} internally, regardless of pin connection externally.

The Boundary Scan Order Assignment tables that follow depict the order in which the bits from the table above are arranged in the Boundary Scan Register. In each notation, Bit 1 is the LSB bit of the register. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Order Assignments
(By Exit Sequence)

256K x 36

Bit	Signal	Pad	Bit	Signal	Pad
1	M2	5R	36	SA	3B
2	SA	4P	37	NC (1)	2B
3	SA	4T	38	SA	3A
4	SA	6R	39	SA	3C
5	SA	5T	40	SA	2C
6	ZZ	7T	41	SA	2A
7	DQa	6P	42	DQc	2D
8	DQa	7P	43	DQc	1D
9	DQa	6N	44	DQc	2E
10	DQa	7N	45	DQc	1E
11	DQa	6M	46	DQc	2F
12	DQa	6L	47	DQc	2G
13	DQa	7L	48	DQc	1G
14	DQa	6K	49	DQc	2H
15	DQa	7K	50	DQc	1H
16	$\overline{SBW}$a	5L	51	$\overline{SBW}$c	3G
17	$\overline{K}$	4L	52	ZQ	4D
18	K	4K	53	$\overline{SS}$	4E
19	$\overline{G}$	4F	54	NC (1)	4G
20	$\overline{SBW}$b	5G	55	NC (1)	4H
21	DQb	7H	56	$\overline{SW}$	4M
22	DQb	6H	57	$\overline{SBW}$d	3L
22	DQb	7G	58	DQd	1K
24	DQb	6G	59	DQd	2K
25	DQb	6F	60	DQd	1L
26	DQb	7E	61	DQd	2L
27	DQb	6E	62	DQd	2M
28	DQb	7D	63	DQd	1N
29	DQb	6D	64	DQd	2N
30	SA	6A	65	DQd	1P
31	SA	6C	66	DQd	2P
32	SA	5C	67	SA	3T
33	SA	5A	68	SA	2R
34	SA	6B	69	SA	4N
35	SA	5B	70	M1	3R

512K x 18

Bit	Signal	Pad	Bit	Signal	Pad
1	M2	5R	36	$\overline{SBW}$b	3G
2	SA	6T	37	ZQ	4D
3	SA	4P	38	$\overline{SS}$	4E
4	SA	6R	39	NC (1)	4G
5	SA	5T	40	NC (1)	4H
6	ZZ	7T	41	$\overline{SW}$	4M
7	DQa	7P	42	DQb	2K
8	DQa	6N	43	DQb	1L
9	DQa	6L	44	DQb	2M
10	DQa	7K	45	DQb	1N
11	$\overline{SBW}$a	5L	46	DQb	2P
12	$\overline{K}$	4L	47	SA	3T
13	K	4K	48	SA	2R
14	$\overline{G}$	4F	49	SA	4N
15	DQa	6H	50	SA	2T
16	DQa	7G	51	M1	3R
17	DQa	6F	52		
18	DQa	7E	53		
19	DQa	6D	54		
20	SA	6A	55		
21	SA	6C	56		
22	SA	5C	57		
22	SA	5A	58		
24	SA	6B	59		
25	SA	5B	60		
26	SA	3B	61		
27	NC (1)	2B	62		
28	SA	3A	63		
29	SA	3C	64		
30	SA	2C	65		
31	SA	2A	66		
32	DQb	1D	67		
33	DQb	2E	68		
34	DQb	2G	69		
35	DQb	1H	70		

Note 1: NC pins at pad location 2B, 4G, and 4H are connected to V_{SS} internally, regardless of pin connection externally.

TAP Instructions

IDCODE

The IDCODE instruction causes a predetermined device- and manufacturer-specific identification code to be loaded into the ID Register when the TAP Controller is in the “Capture-DR” state, and causes the ID Register to be inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state. IDCODE is the default instruction loaded into the Instruction Register at power-up, and when the TAP Controller is in the “Test-Logic Reset” state.

BYPASS

The BYPASS instruction causes a logic “0” to be loaded into the Bypass Register when the TAP Controller is in the “Capture-DR” state, and causes the Bypass Register to be inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

SAMPLE

The SAMPLE instruction causes the logic levels of the signals composing the SRAM’s I/O ring (see the Boundary Scan Register description for the complete list of signals) to be loaded into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and causes the Boundary Scan Register to be inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

The SAMPLE instruction does NOT affect the state of the SRAM’s data output drivers (DQs). They behave exactly as they do during normal SRAM operation. Specifically, the DQs remain in either a High-Z (input) state or Low-Z (output) state during this instruction, depending on when the instruction is executed, as follows:

SAMPLE Executed After	and	State of $\overline{G}$	then	State of DQs
Power-Up		X		High-Z (Inputs)
Sleep Mode		X		High-Z (Inputs)
Read		L		Low-Z (Outputs - Drive most recent read data)
		H		High-Z (Inputs)
Write		X		High-Z (Inputs)
Deselect		X		High-Z (Inputs)

SAMPLE-Z

Like the SAMPLE instruction, the SAMPLE-Z instruction causes the logic levels of the signals composing the SRAM’s I/O ring (see the Boundary Scan Register description for the complete list of signals) to be loaded into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and causes the Boundary Scan Register to be inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

However, unlike the SAMPLE instruction, the SAMPLE-Z instruction DOES affect the state of the SRAM’s data output drivers (DQs). Specifically, the DQs are forced to a High-Z (input) state, allowing an external source to drive these signals as inputs during this instruction.

TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction (see Figure 5). State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the “Test-Logic Reset” state in one of two ways:

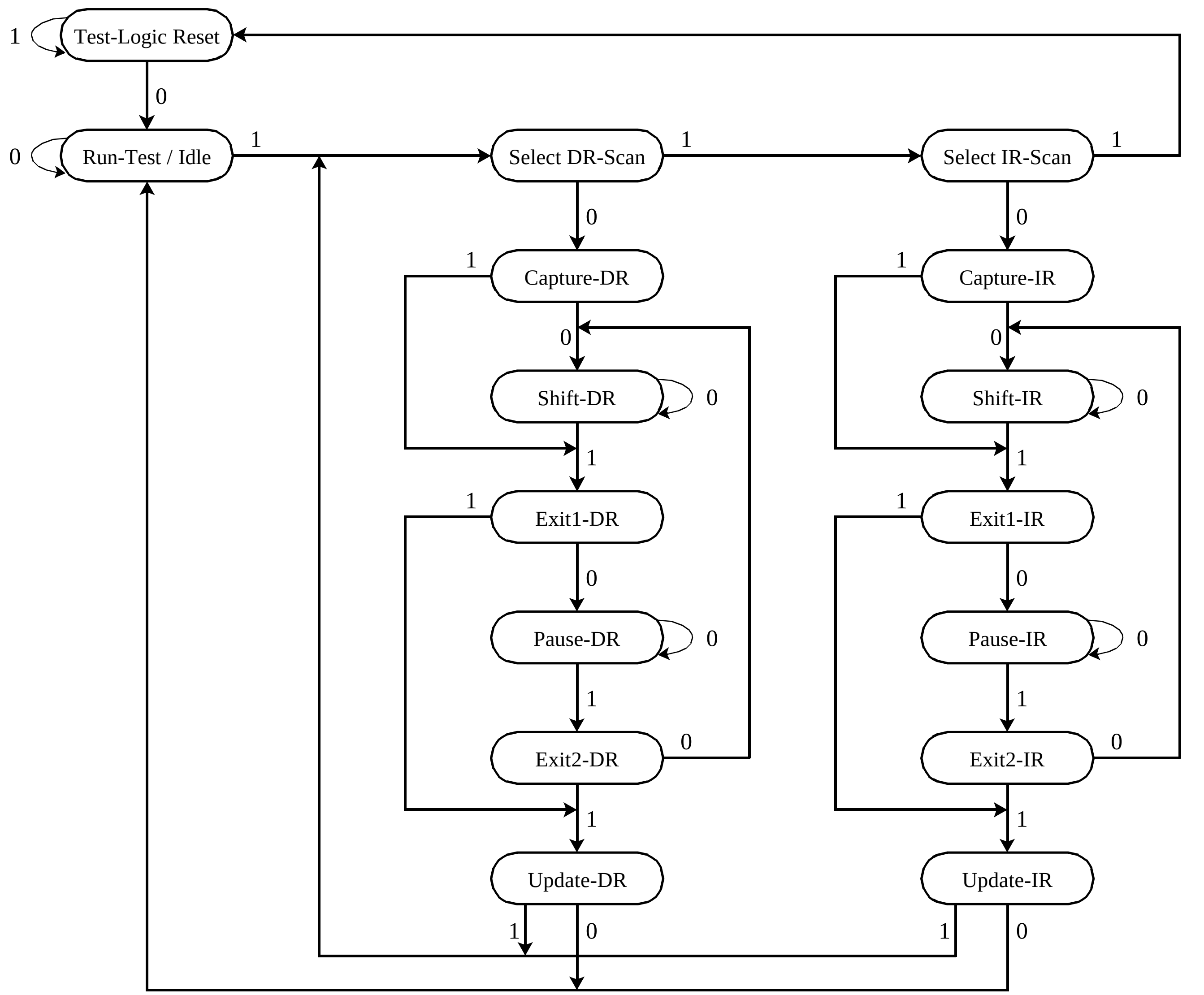
1. At power up.
2. When a logic “1” is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

The TDO output driver is active only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

TAP Controller State Diagram

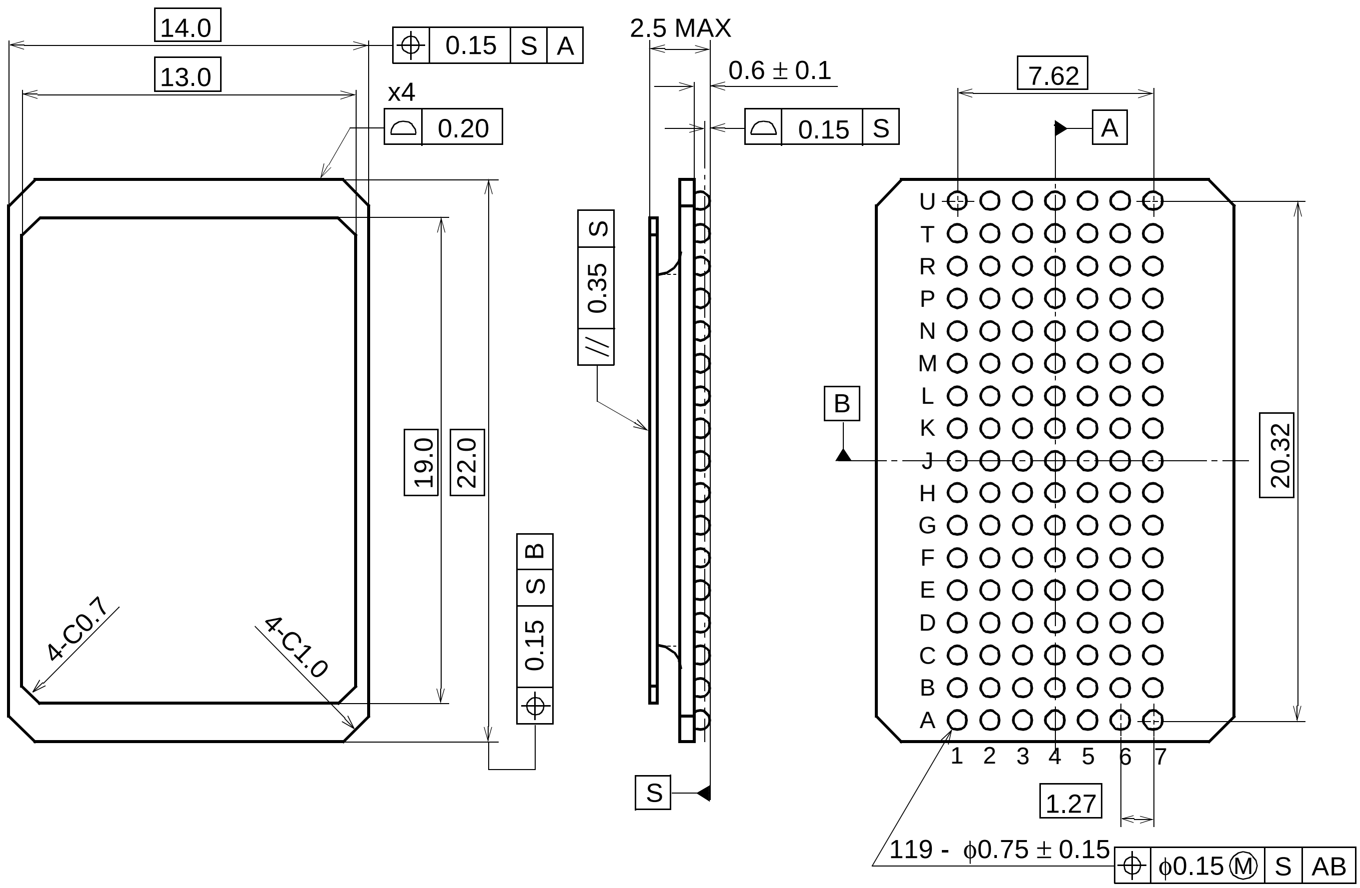
Figure 5



•Ordering Information

Part Number	Device Revision	External V_{DD}	Internal V_{DD}	Size	Speed (Cycle / Data Access Time)
CXK77S36R80AGB-4 CXK77S36R80AGB-4A	2.3.3	3.3V	~2.1V	256K x 36	4.0ns / 2.0ns 4.0ns / 1.8ns
CXK77S36R80AGB-4M CXK77S36R80AGB-4AM	2.3.6	3.3V	~2.4V	256K x 36	4.0ns / 2.0ns 4.0ns / 1.8ns
CXK77S36R80AGB-36	2.3.6	3.3V	~2.4V	256K x 36	3.6ns / 1.8ns
CXK77S36R80AGB-33 CXK77S36R80AGB-33A	2.3.6	3.3V	~2.4V	256K x 36	3.3ns / 1.7ns 3.3ns / 1.6ns
CXK77S18R80AGB-4 CXK77S18R80AGB-4A	2.3.6	3.3V	~2.4V	512K x 18	4.0ns / 2.0ns 4.0ns / 1.8ns
CXK77S18R80AGB-36	2.3.6	3.3V	~2.4V	512K x 18	3.6ns / 1.8ns
CXK77S18R80AGB-33 CXK77S18R80AGB-33A	2.3.6	3.3V	~2.4V	512K x 18	3.3ns / 1.7ns 3.3ns / 1.6ns

(7x17) 119 Pin BGA Package Dimensions



PRELIMINARY

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
BORAD TREATMENT	COPPER-CLAD LAMINATE
LEAD MATERIAL	SOLDER
PACKAGE MASS	1.3g

SONY CODE	BGA-119P-021
EIAJ CODE	BGA119-P-1422
JEDEC CODE	————

•Revision History

Rev. #	Rev. date	Description of Modification
rev 0.0	09/03/99	Initial Version
rev 1.0	10/29/99	1. Modified DC Recommended Operating Conditions (p. 8). V_{DDQ} (max) 1.8V to 1.6V V_{REF}, V_{CM}, V_X (min) 0.55V to 0.6V V_{REF}, V_{CM}, V_X (max) 1.1V to 0.9V V_{IH} (max) AC (note 2) V_{DDQ} + 1.5V to V_{DDQ} + 0.75V V_{IL} (min) AC (note 3) -1.5V to -0.75V V_{IH} (max) AC and V_{IL} (min) AC Duration (max) 1ns to (t_{CYC} / 4) Removed Output Impedance Control Resistor (RQ) specifications. 2. Modified DC Electrical Characteristics (p. 9). Updated max and typ Average Power Supply Operating Currents (I_{DD}). Updated max and typ Average Power Supply Operating Current at 3 MHz (I_{DD3}). Updated max and typ Power Supply Standby Current (I_{SB}). Updated Output Driver Impedance - specified pull-up and pull-down min, typ, and max R_{OUT} output impedance per various RQ impedance control resistor values. 3. Modified AC Timing Characteristics (p. 11). All Bins t_{KHAX}, t_{KHWX}, t_{KHSX}, t_{KHDX} 0.5ns to 0.7ns t_{ZZE} 100ns to 15ns t_{ZZR} 100ns to 30ns
rev 1.1	11/12/99	1. Modified AC Timing Characteristics (p. 11). Added note 4 regarding Address, Write Enables, Synchronous Select, and Data Input Setup Times in the "-33" and "-4" bins that states "these parameters are measured from V_{REF} ± 200mV to the clock mid-point ("-33" and "-4" bins only)". All Bins t_{KHQX}, t_{KHQZ} (min) 0.5ns to 0.7ns -33 t_{AVKH}, t_{WVKH}, t_{SVKH}, t_{DVKH} 0.5ns to 0.3ns -4 t_{AVKH}, t_{WVKH}, t_{SVKH}, t_{DVKH} 0.5ns to 0.3ns
rev 1.2	02/18/00	1. Modified DC Electrical Characteristics (p. 9). Combined separate pull-up and pull-down R_{OUT} specifications into one specification. R_{OUT} (max) at RQ < 150Ω 35Ω to 33Ω R_{OUT} (max) at 150Ω ≤ RQ ≤ 350Ω (RQ/5)*1.15 to (RQ/5)*1.1 R_{OUT} (min) at 150Ω ≤ RQ ≤ 350Ω (RQ/5)*0.85 to (RQ/5)*0.9 R_{OUT} (min) at RQ > 350Ω 59Ω to 63Ω 2. Modified AC Electrical Characteristics (p. 11). Indicated that t_{GVKH} and t_{KHGX} are sampled and not 100% tested. 3. Modified JTAG DC Recommended Operating Conditions (p. 16). V_{TKIH}, V_{TIH} (max) 2.6V to 3.15V V_{TIH} (min) V_{REF} + 0.4V to V_{REF} + 0.15V V_{TIL} (max) V_{REF} - 0.4V to V_{REF} - 0.15V V_{TOH} (min) 1.9V to 2.0V I_{TLI} (min/max) ±10uA at V_{TIN} = 0V to 2.5V Added Note 1 regarding the availability of an application note describing restricted support for V_{TKIH} and V_{TIH} (max) greater than 3.15V. Added Note 2 regarding the availability of application notes describing (1) how to increase V_{TOH} in order to interface with a 3.3V LVTTL receiver, and (2) how to decrease V_{TOH} in order to interface with a 1.5V HSTL receiver. 4. Modified JTAG AC Electrical Characteristics (p. 17). t_{TLQV} (max) 20ns to 9ns

Rev. #	Rev. date	Description of Modification
rev 1.3	05/12/00	1. Modified DC Recommended Operating Conditions (p. 8). V_{DDQ} (max) 1.6V to 2.0V V_{REF}, V_{CM}, V_X (max) 0.9V to 1.0V 2. Modified DC Electrical Characteristics (p. 9). Added "-38" max and typ Average Power Supply Operating Currents (I_{DD}). Added Note 3 regarding R_{OUT} that states "This parameter is guaranteed by design through extensive corner lot characterization". 3. Modified AC Electrical Characteristics (p. 11). Added "-38" bin.
rev 1.4	08/25/00	1. Added BGA Package Thermal Characteristics (p. 7). Junction to Case Temperature (Θ_{JC}) 1.0 °C/W 2. Modified DC Recommended Operating Conditions (p. 8). Added Note 1 regarding V_{DD} (min) that states "V_{DD} (min) down to 2.37V is supported, but certain restrictions apply. Please contact the Sony Memory Application Department for further information". 3. Modified DC Electrical Characteristics (p. 9). Combined separate x36 and x18 I_{DD} specifications into one set of specifications. Removed I_{DD-38} and I_{DD-5} (typ and max) specifications. I_{DD-33} (typ and max) 540ma / 630mA to 660mA / 750mA I_{DD-36} (typ and max) 620mA / 700mA I_{DD-4} (typ and max) 480ma / 560mA to 540mA / 620mA V_{OH} (min) I_{OH} test condition -8.0mA at RQ = 125Ω to -4.0mA at RQ = 250Ω V_{OL} (max) I_{OL} test condition 8.0mA at RQ = 125Ω to 4.0mA at RQ = 250Ω 4. Modified AC Electrical Characteristics (p. 10). Added sub-bin "A" to "-33" bin (t_{KHQV} = 1.6ns). Changed "-38" bin to "-36" bin. Removed "-5" and "-5A" bins. -33 t_{KHQV} 1.8ns to 1.7ns -36 t_{KHKL}, t_{KLKH} 1.5ns to 1.4ns 5. Updated Timing Diagrams (pp. 12-13). 6. Added note to Disabling the TAP section that states that TAP operation does not interfere with normal SRAM operation except during the SAMPLE-Z instruction (p. 14). 7. Modified JTAG AC Test Conditions (p. 15). Corrected V_{DD} test condition 2.5V ± 5% to 3.3V ± 5%
rev 1.5	12/12/00	1. Modified DC Electrical Characteristics (p. 9). I_{DD-4} (typ and max) 540ma / 620mA to 570mA / 650mA 2. Added Note to DC Electrical Characteristics section that illustrates typical output driver impedance for V_{OH}/V_{OL} = 0V to 1.5V when RQ = ~210Ω (p. 10).
rev 1.6	02/05/01	1. Added "M" part number marking to the Ordering Information section in order to distinguish between revision 2.3.3 250MHz x36 devices (marked as "-4" and "-4A") and revision 2.3.6 250MHz x36 devices (marked as "-4M" and "-4AM") (p. 23).