

## CXM3555ER

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### Description

The CXM3555ER is a SP10T antenna switch module for GSM/UMTS/CDMA/LTE multi-mode handset. The CXM3555ER has a built-in dual low pass filter and a +1.8V CMOS compatible decoder. The Sony GaAs Junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.  
(Applications: GSM/UMTS/CDMA/LTE multi-mode handset)

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### Features

- ◆ Low insertion loss :           0.50dB (Typ.) TRx (Cellular band)  
  0.65dB (Typ.) TRx (IMT Tx band)
- ◆ High linearity:                IIP3 = 68dBm
- ◆ Low voltage operation:       V<sub>DD</sub> = 2.5V
- ◆ No DC blocking capacitors
- ◆ Small package (Size):        VQFN-26P (3.0mm ×3.8mm × 0.85mm Max.)
- ◆ Lead-free and RoHS compliant

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### Structure

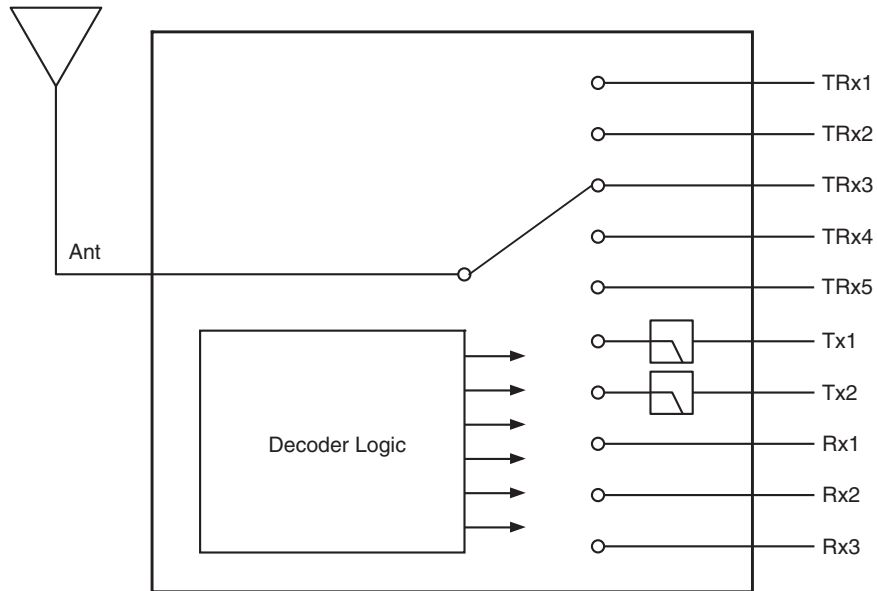
GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

This IC is ESD sensitive device. Special handling precautions are required.

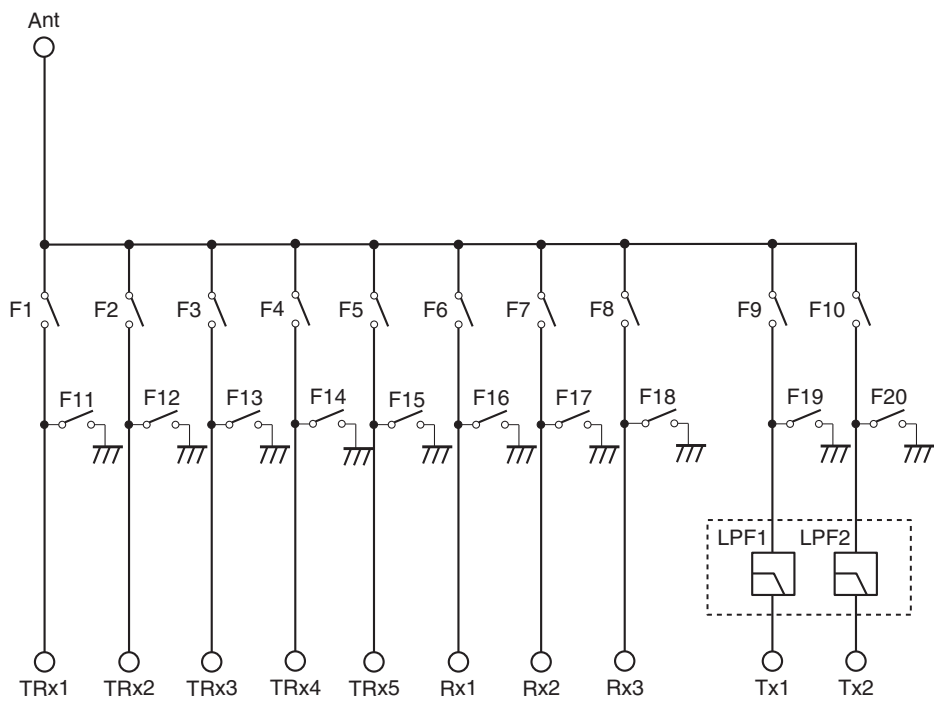
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Block Diagram

SP10T Antenna Switch Module



SP10T 5TRx/2Tx/3Rx

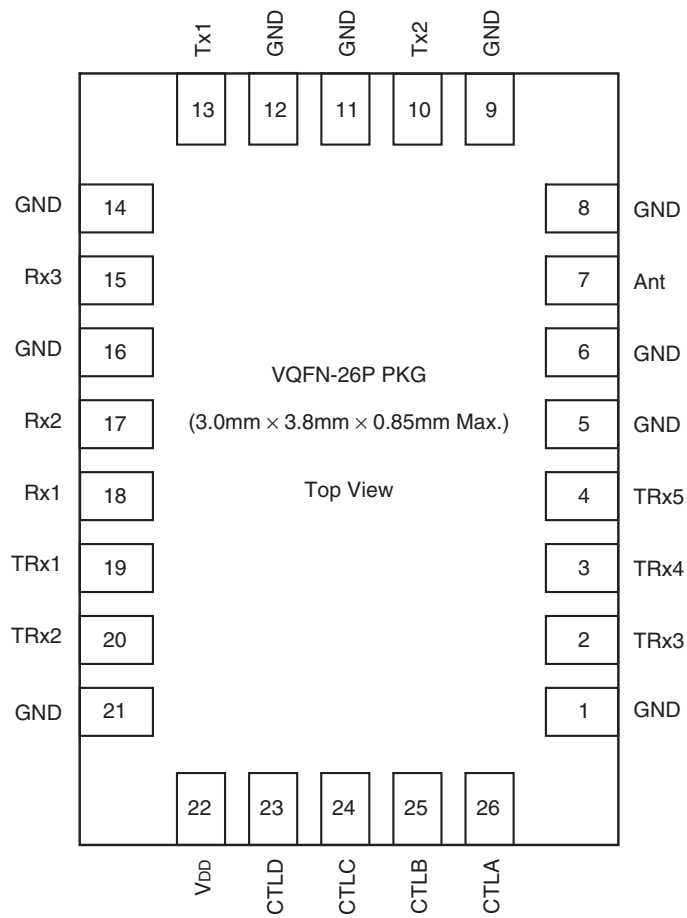


Truth Table

State	Active path	Vctl state				Switch state*1																				
		A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	
1	TRx1*2	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
2	TRx2*2	H	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H
3	TRx3*2	H	L	H	H	L	L	H	L	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
4	TRx4*2	H	H	H	H	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H
5	TRx5*2	H	L	L	H	L	L	L	L	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H
6	Rx1*3	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H
7	Rx2*3	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
8	Rx3*3	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H
9	Tx1	H	H	L	L	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	H	L	H
10	Tx2	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L

\*1 State "L" means a switch "OFF", state "H" means a switch "ON".  
 \*2 Each TRx path can be used over a wide frequency range from 452MHz to 2690MHz.  
 \*3 Each Rx path can be used over a wide frequency range from 869MHz to 1990MHz.

Pin Configuration



DC Bias Conditions

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	2.5	2.8	3.3	V
V <sub>ctl</sub> (H)	1.35	1.8	3.1	V
V <sub>ctl</sub> (L)	0	—	0.45	V



### Absolute Maximum Ratings

◆ Supply voltage	V <sub>DD</sub>	4	V	(Ta = 25°C)
◆ Control voltage	V <sub>ctl</sub>	4	V	(Ta = 25°C)
◆ Maximum input	[Tx1]	36	dBm	(Duty cycle = 12.5% to 50%) (Ta = 25°C)
	[Tx2]	34	dBm	(Duty cycle = 12.5% to 50%) (Ta = 25°C)
	[TRx]	32	dBm	(Ta = 25°C)
	[Rx]	13	dBm	(Ta = 25°C)
◆ Operating temperature	T <sub>opr</sub>	-35 to +90	°C	
◆ Storage temperature	T <sub>stg</sub>	-65 to +150	°C	

Electrical Characteristics

(V<sub>DD</sub> = 2.5V, T<sub>a</sub> = 25°C)

Item	Symbol	Path	Conditions	Min.	Typ.	Max.	Unit
Insertion loss	I.L	Ant-TRx1	*1, *2, *3	—	0.50	0.60	dB
			*4	—	0.64	0.79	
			*5	—	0.66	0.81	
			*6	—	0.78	0.98	
			*7	—	0.85	1.05	
		Ant-TRx2	*1, *2, *3	—	0.50	0.60	
			*4	—	0.63	0.78	
			*5	—	0.65	0.80	
			*6	—	0.74	0.94	
			*7	—	0.79	0.99	
		Ant-TRx3	*1, *3	—	0.40	0.50	
			*2	—	0.38	0.48	
			*4	—	0.51	0.66	
			*5	—	0.53	0.68	
			*6	—	0.62	0.82	
		Ant-TRx4	*1, *2, *3	—	0.48	0.58	
			*4	—	0.65	0.80	
			*5	—	0.68	0.83	
			*6	—	0.80	1.00	
			*7	—	0.85	1.05	
		Ant-TRx5	*1, *2, *3	—	0.49	0.59	
			*4	—	0.68	0.83	
*5	—		0.71	0.86			
*6	—		0.86	1.06			
*7	—		0.91	1.11			
Ant-Tx1		*8	—	1.00	1.15		
Ant-Tx2		*9	—	1.00	1.20		
Ant-Rx1, Rx2, Rx3		*10	—	0.84	0.94		
		*11	—	0.98	1.13		

Item	Symbol	Path	Conditions	Min.	Typ.	Max.	Unit
Isolation	ISO	Tx1-TRx1, 2, 3, 4, 5, Rx1, 2, 3 (Tx1 Active)	824 to 915MHz	35	—	—	dB
		Tx2-TRx1, 2, 3, 4, 5, Rx1, 2, 3 (Tx2 Active)	1710 to 1910MHz	32	—	—	
		TRx1, 2-TRx3, 4, 5 (TRx1, TRx2, TRx3 or TRx4 Active)	600 to 2170MHz	32	—	—	
		TRx1-TRx2 (TRx1 or TRx2 Active)	600 to 2170MHz	17	—	—	
		TRx3-TRx4 (TRx3 or TRx4 Active)	600 to 2170MHz	20	—	—	
		TRx3-TRx5 (TRx3 or TRx5 Active)	600 to 2170MHz	25	—	—	
		TRx4-TRx5 (TRx4 or TRx5 Active)	600 to 1990MHz	25	—	—	
		TRx1-Rx3 (TRx1 Active)	1920 to 1980MHz	30	—	—	
		Ant-Rx1 (Rx3 Active)	1805 to 1990MHz	40	—	—	
		Ant-Rx3 (Rx1 Active)	1805 to 1990MHz	40	—	—	
		Ant-Rx2 (Rx3 Active)	1805 to 1990MHz	37	—	—	
		Ant-Rx3 (Rx2 Active)	1805 to 1990MHz	40	—	—	
VSWR	VSWR	All ports active paths	600 to 2170MHz	—	—	1.50	—
Harmonics	2fo	Ant-TRx1, 2, 3, 4, 5	*3, *4	—	—	-36	dBm
	3fo			—	—	-36	
	2fo	Ant-Tx1	*8	—	—	-36	
	3fo			—	—	-36	
	2fo	Ant-Tx2	*9	—	—	-36	
	3fo			—	—	-36	
Attenuation	ATT	Tx1-Ant	1648 to 1830MHz	25	—	—	dB
			2472 to 2745MHz	25	—	—	
			3296 to 12750MHz	20	—	—	
		Tx2-Ant	3420 to 3820MHz	25	—	—	
			5130 to 5730MHz	25	—	—	
			6840 to 7000MHz	15	—	—	
Intermodulation distortion level in Rx band	IMD2	Ant-TRx1, 2, 3, 4, 5	*12,*13,*14,*17,*18,*21,*22	—	—	-105	dBm
	IMD3		*12,*15,*16,*19,*20,*23,*24	—	—	-105	
Input IP3	IIP3	Ant-TRx1, 2, 3, 4, 5	*12, *25	—	68	—	dBm
			*12, *26	—	68	—	
Switching time	Ts		50% ctl to 90% RF	—	3	5	μs
Control current	Ictl		Vctl = 1.80V	—	5	20	μA
Supply current	I <sub>DD</sub>		V <sub>DD</sub> = 2.50V	—	0.2	0.4	mA

Electrical characteristics are measured with all RF ports terminated in 50Ω

- \*1 Pin = 26dBm, 452 to 468MHz (Band class 5)
- \*2 Pin = 25dBm, 704 to 787MHz (Band 13, Band 17)
- \*3 Pin = 26dBm, 824 to 960MHz (Band 5, Band 8)
- \*4 Pin = 26dBm, 1710 to 1990MHz (Band 1 Tx, Band 2, Band 3, Band 4 Tx)
- \*5 Pin = 10dBm, 2110 to 2170MHz (Band 1 Rx, Band 4 Rx)
- \*6 Pin = 26dBm, 2300 to 2400MHz (Band 40)
- \*7 Pin = 26dBm, 2500 to 2690MHz (Band 7)
- \*8 Pin = 35dBm, 824 to 915MHz (GSM 850/900 Tx)
- \*9 Pin = 32dBm, 1710 to 1910MHz (GSM 1800/1900 Tx)
- \*10 Pin = 10dBm, 869 to 960MHz (GSM 850/900 Rx)
- \*11 Pin = 10dBm, 1805 to 1990MHz (GSM 1800/1900 Rx)
- \*12 Measured with the recommended circuit

**IMD Condition**

Band	fRx on TRx	fRx +20dBm on TRx	fBlocker -15dBm on Ant		IMD Condition
Band I	2140MHz	1950MHz	IMD2 (fRx-fTx)	190MHz	*13
			IMD2 (fRx-fTx)	4090MHz	*14
			IMD3 (2fTx-fRx)	1760MHz	*15
			IMD3 (2fTx-fRx)	6040MHz	*16
Band II	1960MHz	1880MHz	IMD2 (fRx-fTx)	80MHz	*17
			IMD2 (fRx-fTx)	3840MHz	*18
			IMD3 (2fTx-fRx)	1800MHz	*19
			IMD3 (2fTx-fRx)	5720MHz	*20
Band V	880MHz	835MHz	IMD2 (fRx-fTx)	45MHz	*21
			IMD2 (fRx-fTx)	1715MHz	*22
			IMD3 (2fTx-fRx)	790MHz	*23
			IMD3 (2fTx-fRx)	2550MHz	*24

**IIP3 Condition**

Band	f1 +27dBm on TRx	f2 +27dBm on TRx	IIP3 Condition IIP3 = (3 × Pout – IM3)/2
Band I	1950MHz	1951MHz	*25
Band V	835MHz	836MHz	*26



**Triple Beat Ratio**

(V<sub>DD</sub> = 2.5V, T<sub>a</sub> = 25°C)

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
Triple Beat Ratio	TBR		Tx1 at TRx* <sup>1</sup> 21.5dBm [MHz]	Tx2 at TRx* <sup>1</sup> 21.5dBm [MHz]	Jammer at Ant -30dBm [MHz]	Triple Beat Product at TRx* <sup>1</sup> [MHz]				dBc
		Ant-TRx1, 2, 3, 4, 5	835.5	836.5	881.5	881.5±1	81	—	—	
			1880	1881	1960	1960±1	81	—	—	

\*1 Electrical characteristics are measured with all RF ports terminated in 50Ω.  
Measured with the recommended circuit

**IIP2**

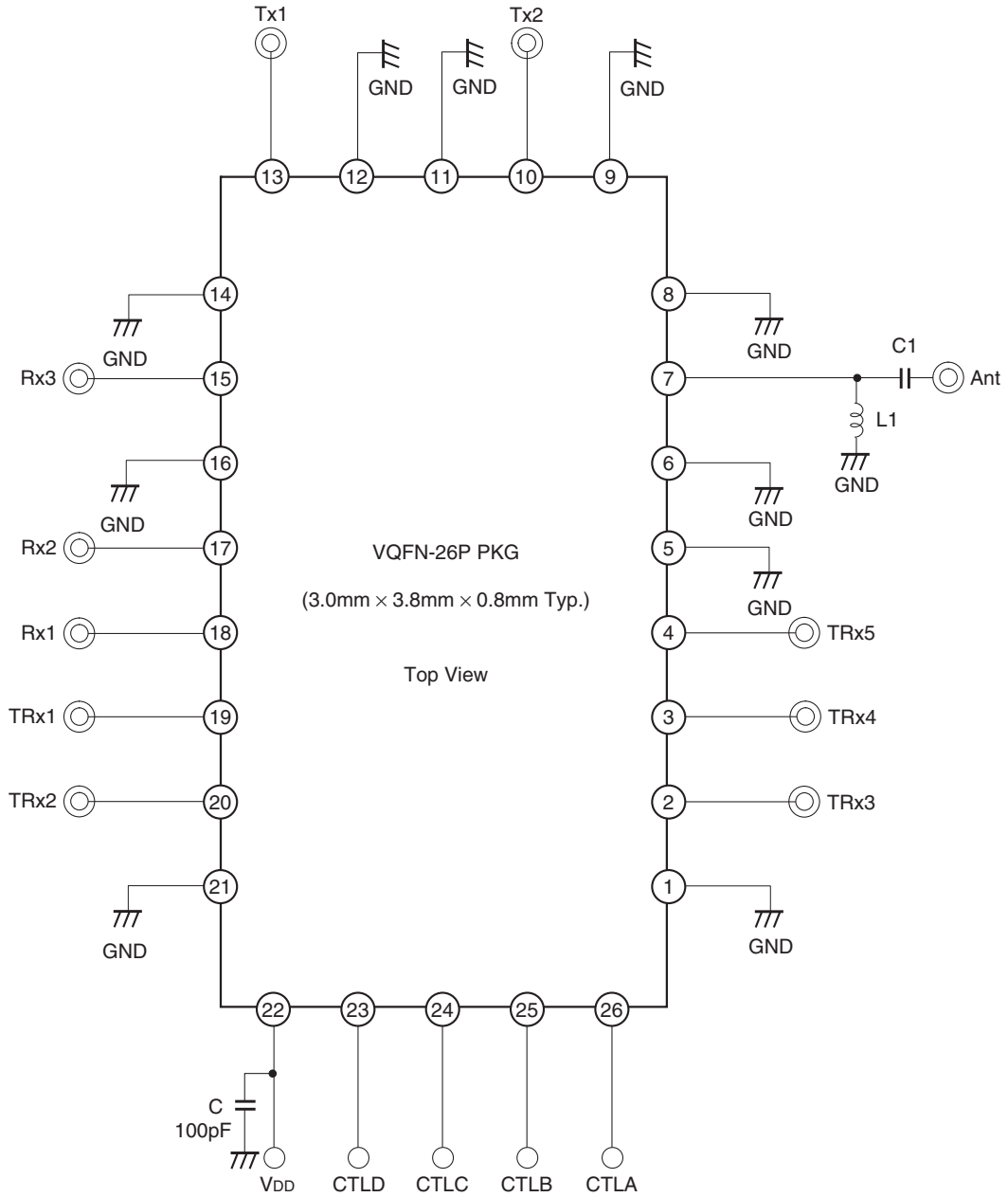
(V<sub>DD</sub> = 2.5V, T<sub>a</sub> = 25°C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Input IP2	IIP2		Tx at TRx* <sup>1</sup> 24dBm [MHz]	Jammer at Ant -20dBm [MHz]	IM2 Product at TRx* <sup>1</sup> [MHz]				dBm
		Ant-TRx1, 2, 3, 4, 5	836.61	1718.61	881.61	113.5	—	—	
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

\*1 Electrical characteristics are measured with all RF ports terminated in 50Ω.  
Measured with the recommended circuit

Recommended Circuit 1

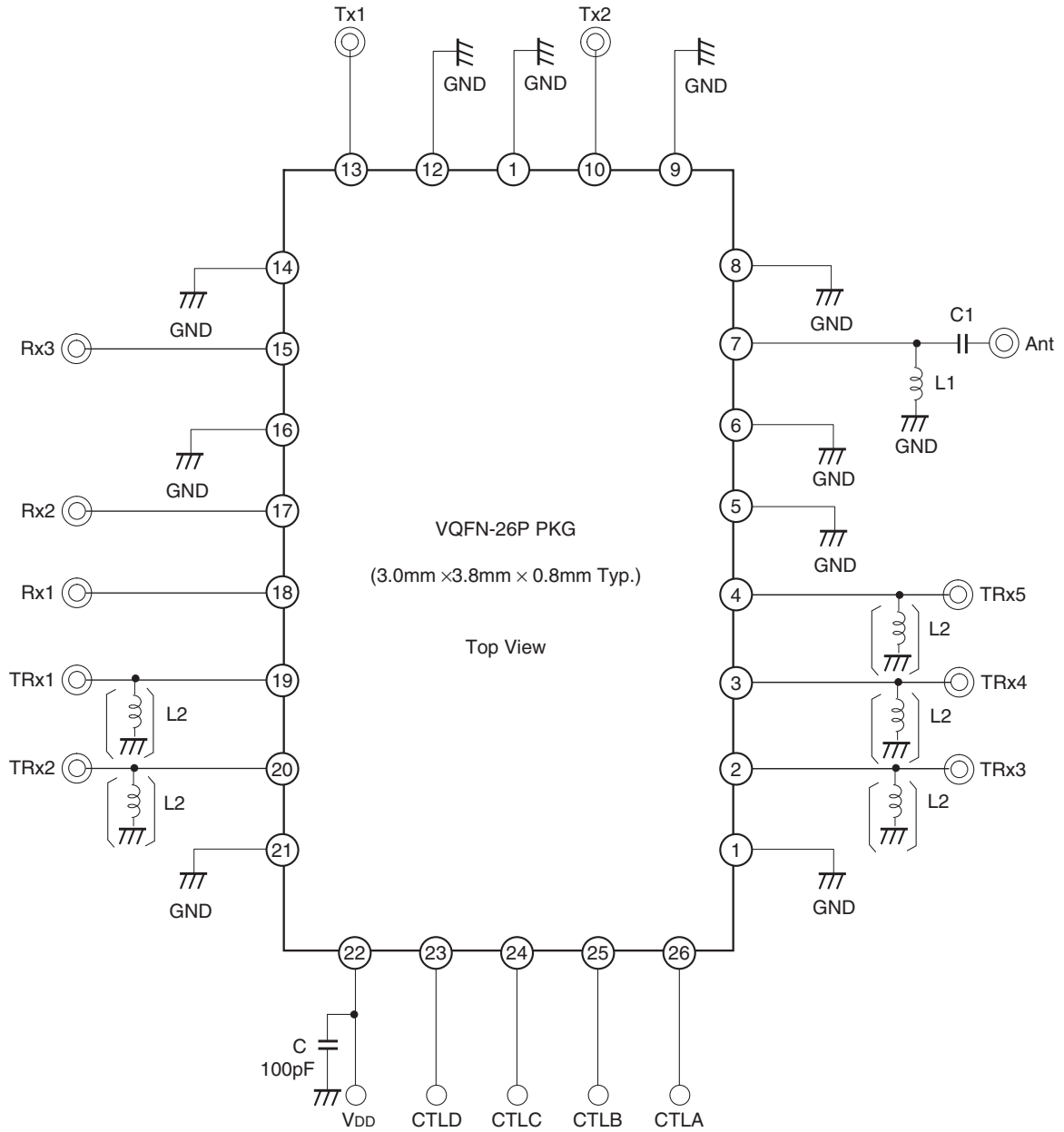
Operation frequency range: 0.8-2.7GHz



- \*1 No DC blocking capacitors are required on all RF ports.
- \*2 The DC levels of all RF ports are GND.
- \*3 L1 (33nH) and C1 (22pF) are recommended on Ant port for ESD protection.

Recommended Circuit 2

Operation frequency range: 0.45-2.7GHz



- \*1 No DC blocking capacitors are required on all RF ports.
- \*2 The DC levels of all RF ports are GND.
- \*3 L1 (47nH) and C1 (22pF) are recommended on Ant port for ESD protection.
- \*4 L2 (12nH) is recommended on TRx port for Band I to improve IMD2 performance. (Rx-Tx(190MHz))

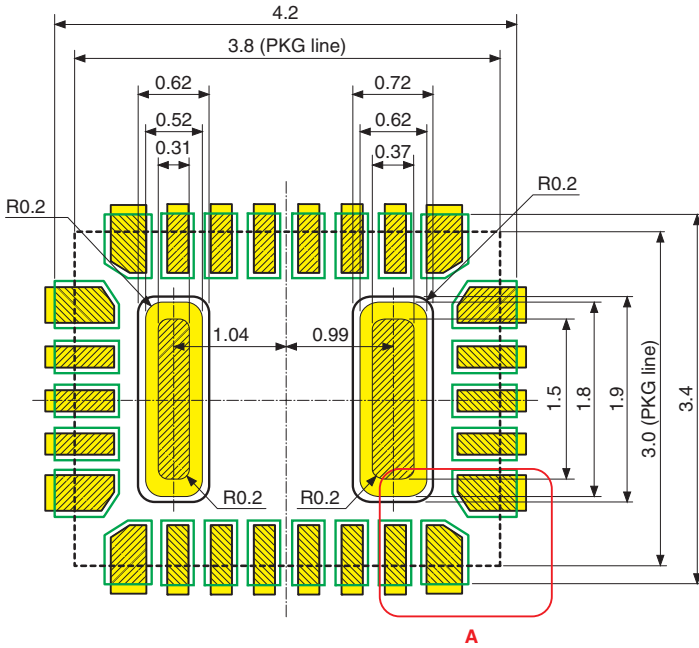
PCB Layout

Foot Pattern

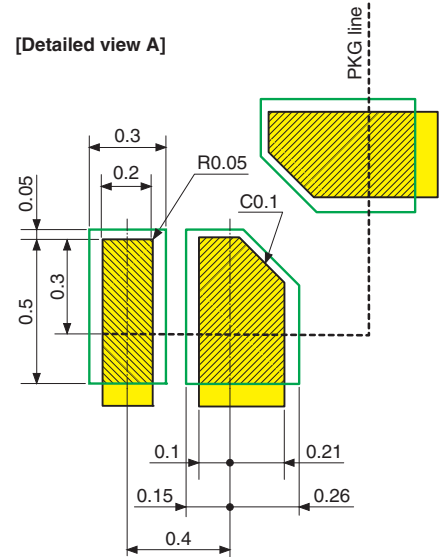
- PKG size : 3.8mm × 3.0mm
- Pin pitch : 0.4mm

- : Land
- ▨ : Mask (Open area)
- : Resist (Open area)

\* Metal mask thickness: 110µm

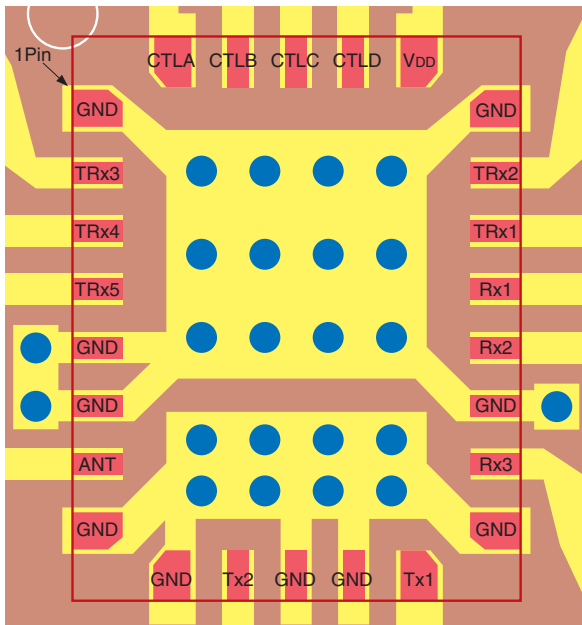


[Detailed view A]



\* Mask corner R = 0.05mm

Recommended PCB Design



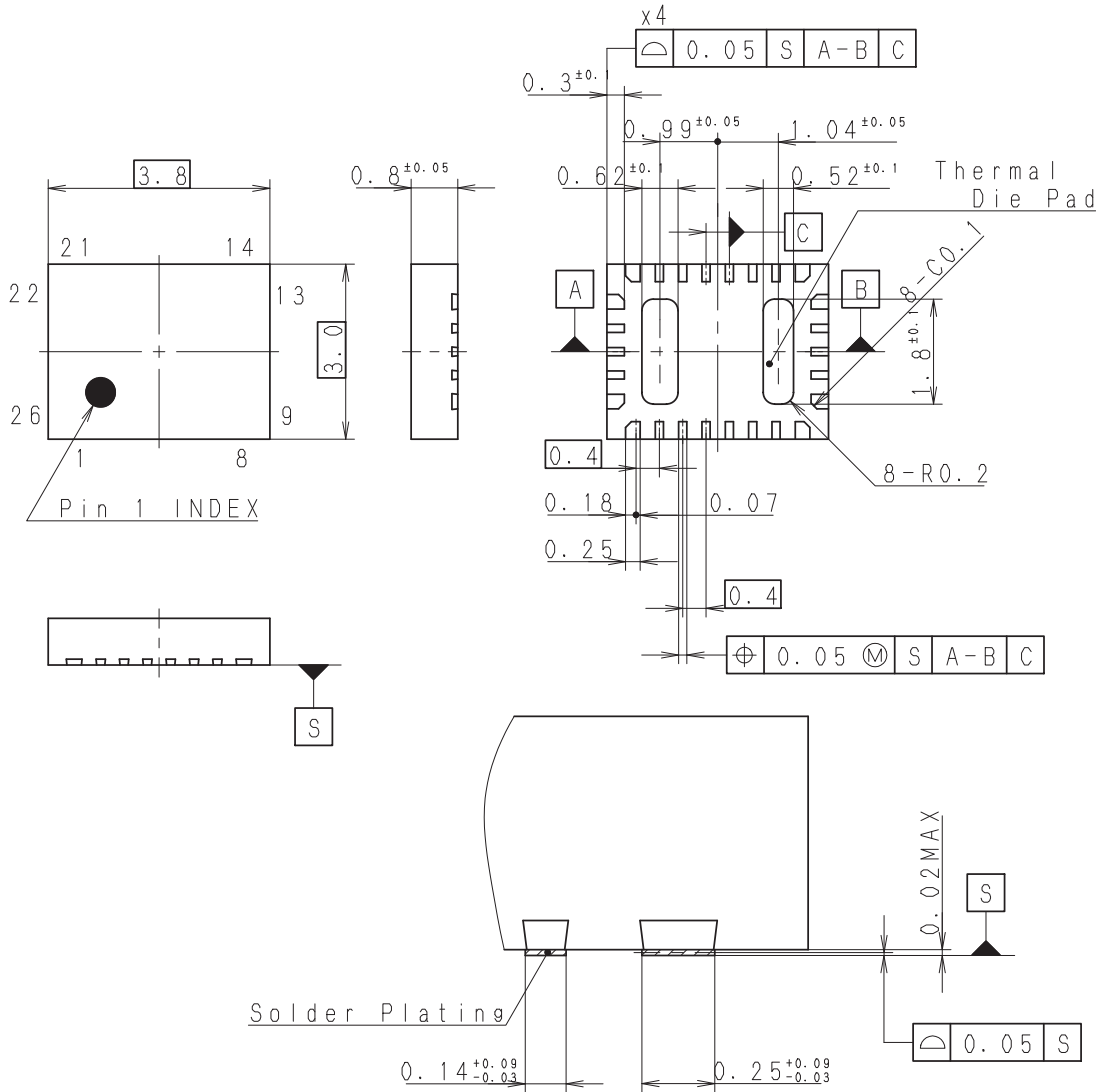
- GND Via hole
- VQFN-26P package
- Pin

Package Outline

(Unit: mm)

Product Code: 875336252/875342099

26 PIN VQFN (PLASTIC)



Note:Cutting burr of lead are 0.05mm MAX.

TERMINAL SECTION  
PACKAGE STRUCTURE

SONY CODE	VQFN-26P-01
JEITA CODE	—
JEDEC CODE	—

AP-4000-26008S

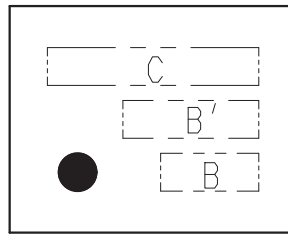
Rev. 0

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm




**Marking**


MARKING C : **M3555**

- 注1) C部は製品名 (Max 6文字) を配置する。  
 (6文字を超える場合は製品名省略標示規定に従う。)
- 2) B, B' 部はロット番号 (Max 7文字) を配置する。  
 (但し B部Max 3文字, B' 部Max 4文字とする。規定文字数未満につき省略は省略規定に従う。)
- 3) 文字位置は、右詰めとする。

< INSTRUCTIONS >

- 1) TYPE NO. ( MAX 6 CHARACTERS ) IN SECTION C.  
 ( FOR MORE THAN 6 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS. )
- 2) LOT NO. ( MAX 7 CHARACTERS ) IN SECTION B, B'.  
 ( B: 3 CHARACTERS , B' : 4 CHARACTERS. FOLL RULES FOR ABBREVIATIONS. )
- 3) PUT THE POSITION OF A CHARACTER REFERENCE FROM THE RIGHT SIDE.