SONY

SP10T Antenna Switch Module for 8TRx/2Tx

CXM3572ER

Description

The CXM3572ER is a SP10T antenna switch module for GSM/UMTS/CDMA/LTE multi-mode handset.
The CXM3572ER has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking Capacitor.

Features

- Low Insertion Loss: 0.45 dB (Typ.) TRx (Cellular Band)
  0.60 dB (Typ.) TRx (IMT Tx Band)
- High Linearity: IIP3 = 68 dBm
- Low Voltage Operation: V_{DD} = 2.5 V
- No DC Blocking Capacitors (Except sourcing DC bias)
- Small Package Size: VQFN-24P (2.4 mm × 3.2 mm × 0.85 mm Max.)
- Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

Absolute Maximum Ratings

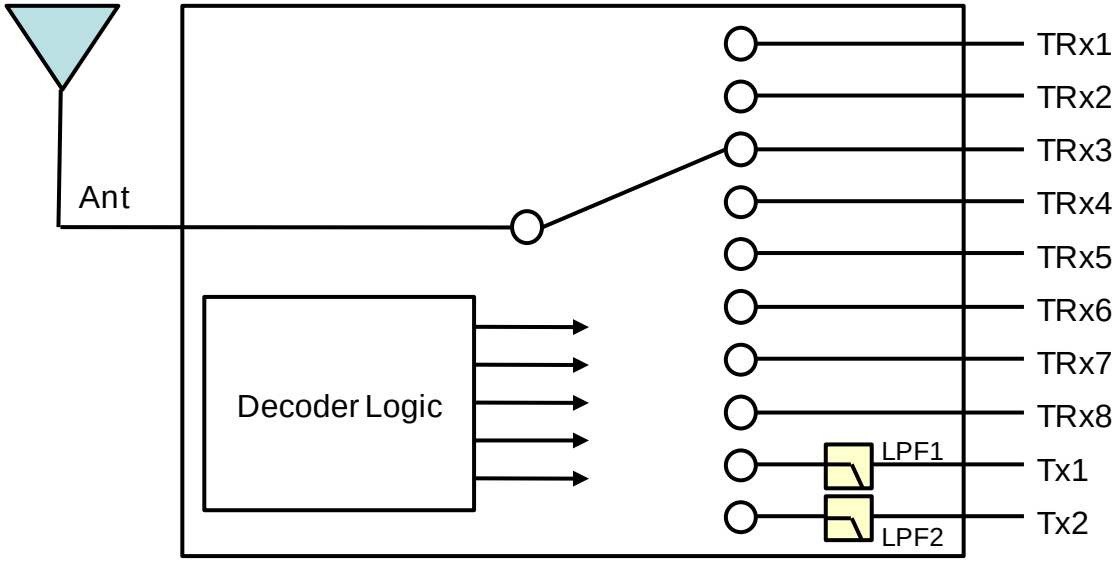
◆ Supply voltage	V_{DD}	6	V	(Ta = 25 °C)
◆ Control voltage	Vctl	4	V	(Ta = 25 °C)
◆ Maximum input	[Tx1]	36	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[Tx2]	34	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[TRx]	32	dBm	(Ta = 25 °C)
◆ Operating temperature	Topr	–35 to +90	°C	
◆ Storage temperature	Tstg	–65 to +150	°C	

This IC is ESD sensitive device. Special handling precautions are required.

E12514

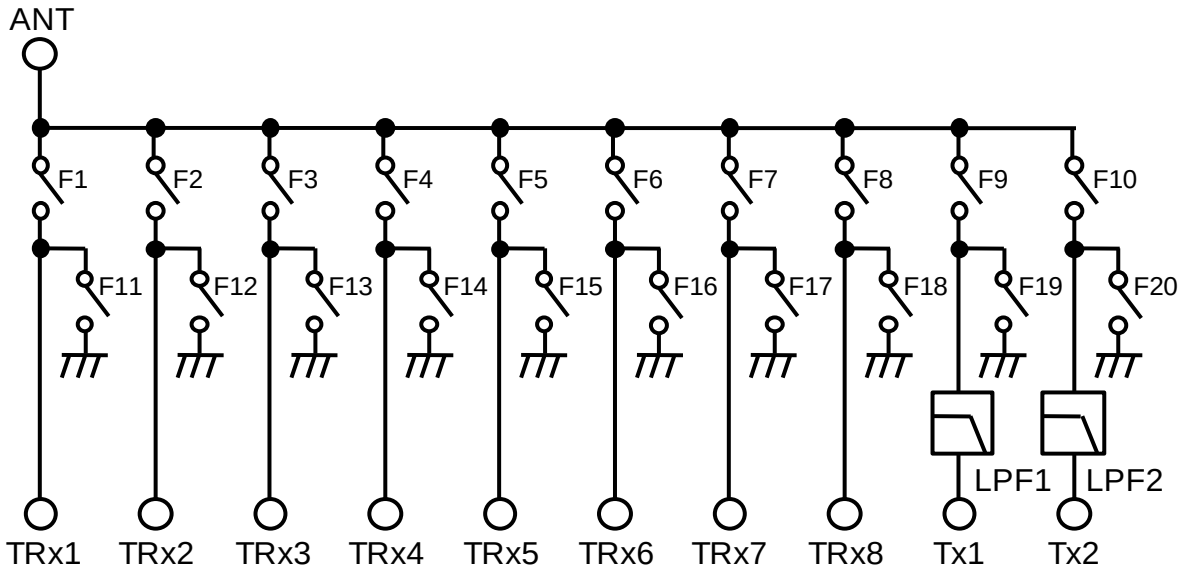
Block Diagram

SP10T Antenna Switch Module



Block Diagram

SP10T 8TRx/2Tx

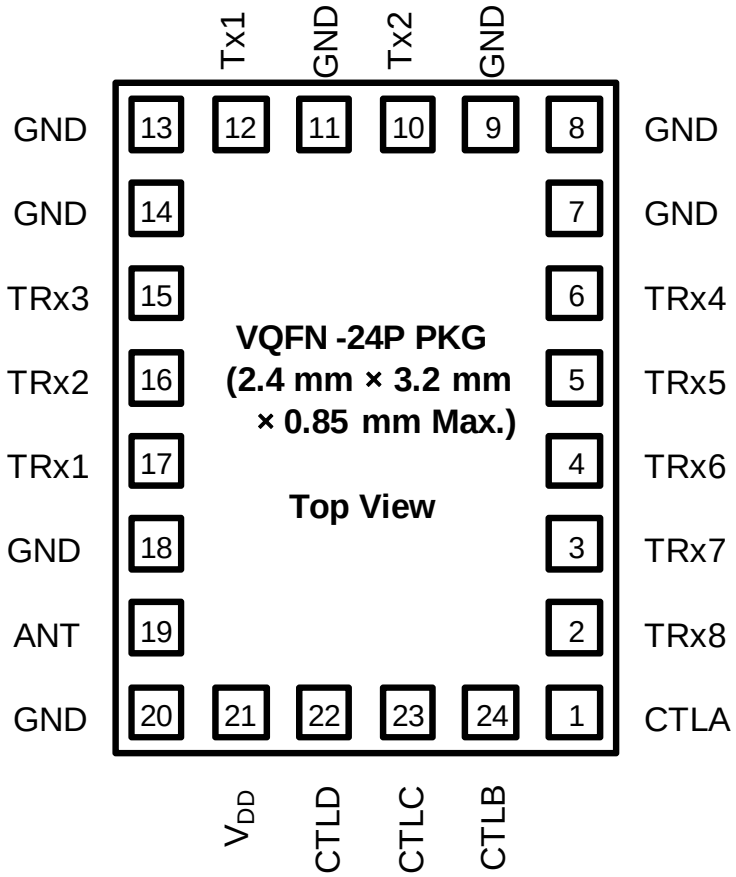


Truth Table

State	Active Path	CTL state				SW state(*1)																			
		CLTA	CTLB	CLTC	CTLD	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20
1	TRx1	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
2	TRx2	H	L	H	L	L	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H
3	TRx3	H	H	H	L	L	L	H	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
4	TRx4	H	L	H	H	L	L	L	H	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H
5	TRx5	H	H	H	H	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H
6	TRx6	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
7	TRx7	L	H	H	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H
8	TRx8	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	L	H	H
9	Tx1	H	H	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L	H
10	Tx2	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L

(*1) State ”L” means a switch “OFF”, State ”H” means a switch “ON”

Pin Configuration



DC Bias Conditions

(Ta = 25 °C)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.8	5.0	V
Vctl (H)	1.35	1.8	3.3	V
Vctl (L)	0	—	0.45	V

Electrical Characteristics

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	ANT - TRx1	*1, *2, *3, *11	-	0.45	0.55	dB
			*4	-	0.54	0.69	
			*5, *12	-	0.58	0.73	
			*6	-	0.64	0.79	
			*7, *8	-	0.85	1.05	
		ANT - TRx2	*1, *2, *3, *11	-	0.45	0.55	
			*4	-	0.54	0.69	
			*5, *12	-	0.58	0.73	
			*6	-	0.62	0.77	
			*7, *8	-	0.75	0.95	
		ANT - TRx3	*1, *2, *3, *11	-	0.47	0.57	
			*4	-	0.54	0.69	
			*5, *12	-	0.58	0.73	
			*6	-	0.61	0.76	
			*7, *8	-	0.75	0.95	
		ANT - TRx4	*1, *2, *3, *11	-	0.49	0.59	
			*4	-	0.55	0.70	
			*5, *12	-	0.59	0.74	
			*6	-	0.61	0.76	
			*7, *8	-	0.73	0.93	
		ANT - TRx5	*1, *2, *3, *11	-	0.47	0.57	
			*4	-	0.54	0.69	
			*5, *12	-	0.58	0.73	
			*6	-	0.61	0.76	
			*7, *8	-	0.75	0.95	
		ANT - TRx6	*1, *2, *3, *11	-	0.47	0.57	
			*4	-	0.54	0.69	
			*5, *12	-	0.58	0.73	
			*6	-	0.61	0.76	
			*7, *8	-	0.75	0.95	
		ANT - TRx7	*1, *2, *3, *11	-	0.55	0.65	
			*4	-	0.65	0.80	
			*5, *12	-	0.70	0.85	
			*6	-	0.75	0.90	
			*7, *8	-	1.00	1.20	
		ANT - TRx8	*1, *2, *3, *11	-	0.55	0.65	
			*4	-	0.64	0.79	
			*5, *12	-	0.68	0.83	
			*6	-	0.73	0.88	
			*7, *8	-	0.95	1.15	
		ANT - Tx1	*8	-	1.20	1.30	
		ANT - Tx2	*9	-	1.27	1.42	

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO.	Tx1 - TRx1, 2, 3, 4, 5, 6 (Tx1 Active)	*9	33	-	-	dB
		Tx1 - TRx7, 8 (Tx1 Active)		40	-	-	
		Tx2 - TRx1, 2, 3, 4, 5, 6 (Tx2 Active)	*10	28	-	-	
		Tx2 - TRx7, 8 (Tx2 Active)		40	-	-	
		TRx1 - TRx4, 5, 6, 7, 8 (The input port is Active)	*1, *2, *3, *11	33	-	-	
			*4, *5, *6, *12	27	-	-	
		TRx2, 3 - TRx4, 5, 6, 7, 8 (The input port is Active)	*1, *2, *3, *11	40	-	-	
			*4, *5, *6, *12	33	-	-	
		TRx5 - TRx1, 2, 3 (TRx5 Active)	*7, *8	26	-	-	
		TRx1 - TRx2 (TRx1, 2 Active)	*1, *2, *3, *11	29	-	-	
			*4, *5, *6, *12	19	-	-	
		TRx1 - TRx3 (TRx1, 3 Active)	*1, *2, *3, *11	36	-	-	
			*4, *5, *6, *12	26	-	-	
		TRx2 - TRx3 (TRx2, 3 Active)	*1, *2, *3, *11	28	-	-	
			*4, *5, *11	19	-	-	
		TRx4 - TRx5 (TRx4, 5 Active)	*1, *2, *3, *11	26	-	-	
			*4, *5, *6, *12	18	-	-	
			*7, *8	16	-	-	
		TRx4 - TRx6 (TRx4, 6 Active)	*1, *2, *3, *11	33	-	-	
			*4, *5, *6, *12	24	-	-	
		TRx4 - TRx7, 8 (TRx4, 7, 8 Active)	*1, *2, *3, *11	35	-	-	
			*4, *5, *6, *12	30	-	-	
		TRx5 - TRx6 (TRx4, 5 Active)	*1, *2, *3, *11	25	-	-	
			*4, *5, *6, *12	18	-	-	
			*7, *8	15	-	-	
		TRx5 - TRx7, 8 (TRx5, 7, 8 Active)	*1, *2, *3, *11	30	-	-	
			*4, *5, *6, *12	25	-	-	
		TRx7 - TRx 8 (TRx7, 8 Active)	*1, *2, *3, *10	25	-	-	
			*4, *5, *6, *12	18	-	-	

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
VSWR	VSWR	ANT - Tx1	824 to 915 MHz	-	-	2.00	-
		ANT - Tx2	1710 to 1910 MHz	-	-	1.50	
		ANT - TRx1, 2, 3, 4, 5, 6, 7, 8	600 to 2170 MHz	-	-	1.50	
Harmonics	2fo	ANT - TRx1, 2, 3, 4, 5, 6, 7, 8	*3, *4, *5	-	-	-40	dBm
	3fo			-	-	-40	
	2fo	ANT - Tx1	*9	-	-	-36	
	3fo			-	-	-36	
	2fo	ANT - Tx2	*10	-	-	-36	
	3fo			-	-	-36	
Attenuation	ATT	Tx1 - ANT	1648 to 1830 MHz	25	-	-	dB
			2472 to 2745 MHz	25	-	-	
			3290 to 4120 MHz	20	-	-	
			4120 to 6405 MHz	14	-	-	
			6405 to 10000 MHz	20	-	-	
			10000 to 12750 MHz	15	-	-	
		Tx2 - ANT	3420 to 3820 MHz	25	-	-	
			5130 to 5730 MHz	25	-	-	
			6840 to 12750 MHz	20	-	-	
Inter Modulation Product Power in Rx Band	IMD2	ANT - TRx1, 2, 3, 4, 5, 6, 7, 8	*13, *26, *27	-	-	-105	dBm
	IMD3		*13, *28, *29	-	-	-105	
	IMD2	ANT - TRx1, 2, 3, 4, 5, 6	*13,*14,*15,*18,*19,*22,*23	-	-	-105	
	IMD3		*13,*16,*17,*20,*21,*24,*25	-	-	-105	
	IMD2	ANT - TRx7, 8	*13,*14,*15,*18,*19,*22,*23	-	-	-99	
	IMD3		*13,*16,*17,*20,*21,*24,*25	-	-	-105	
Input IIP3	IIP3	ANT - TRx1, 2, 3, 4, 5, 6, 7, 8	*13, *30, *31	-	68	-	
Switching Time	Ts	Active mode	50 % Ctl to 90 % RF	-	3	5	µs
Strat UP Time	Tst		V_{DD} = 0 to 2.8 V	-	6	50	
Control Current	Ictl		Vctl = 1.8 V	-	1	5	µA
Supply Current	Idd	Active mode	V_{DD} =2.8 V	-	0.23	0.40	mA

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of TRx (UMTS / CDMA)

*1 Pin = 26 dBm, 452 to 468 MHz (Band Class 5)

*2 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)

*3 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)

*4 Pin = 26 dBm, 1428 to 1511 MHz (Band 11, Band 21)

*5 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band4 Tx)

*6 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)

*7 Pin = 26 dBm, 2300 to 2400 MHz (Band 40)

*8 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)

*9 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)

*10 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)

*11 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)

*12 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)

*13 Measured with the recommended circuit 1

IMD Condition

Band	fRx on RF [MHz]	fTx +20 dBm on RF [MHz]	fBlocker -15 dBm on ANT [MHz]		IMD Condition
Band 1	2140	1950	IMD2 (fRx - fTx)	190	*14
			IMD2 (fRx + fTx)	4090	*15
			IMD3 (2fTx - fRx)	1760	*16
			IMD3 (2fTx + fRx)	6040	*17
Band 2	1960	1880	IMD2 (fRx - fTx)	80	*18
			IMD2 (fRx + fTx)	3840	*19
			IMD3 (2fTx - fRx)	1800	*20
			IMD3 (2fTx + fRx)	5720	*21
Band 11	1486	1438	IMD2 (fRx - fTx)	48	*22
			IMD2 (fRx + fTx)	2924	*23
			IMD3 (2fTx - fRx)	1390	*24
			IMD3 (2fTx + fRx)	4362	*25
Band 5	880	835	IMD2 (fRx - fTx)	45	*26
			IMD2 (fRx + fTx)	1715	*27
			IMD3 (2fTx - fRx)	790	*28
			IMD3 (2fTx + fRx)	2550	*29

IIP3 Condition

Band	f1 +27 dBm on RF [MHz]	f2 +27 dBm on RF [MHz]	IIP3 Condition IIP3 = (3 × Pout - IMD3)/2 [dBm]
Band 1	1950	1951	*30
Band 5	835	836	*31

Electrical Characteristics of Triple Beat Ratio

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
			Tx1 at TRx 21.5 dBm [MHz]	Tx2 at TRx 21.5 dBm [MHz]	Jammer at ANT –30 dBm [MHz]	Triple Beat Product at TRx [MHz]				
Triple Beat Ratio	TBR	ANT-TRx1, 2, 3, 4, 5, 6, 7, 8	835.5	836.5	881.5	881.5 ± 1	81	—	—	dBc
			1880	1881	1960	1960 ± 1	81	—	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit 1

Electrical Characteristics of Input IP2

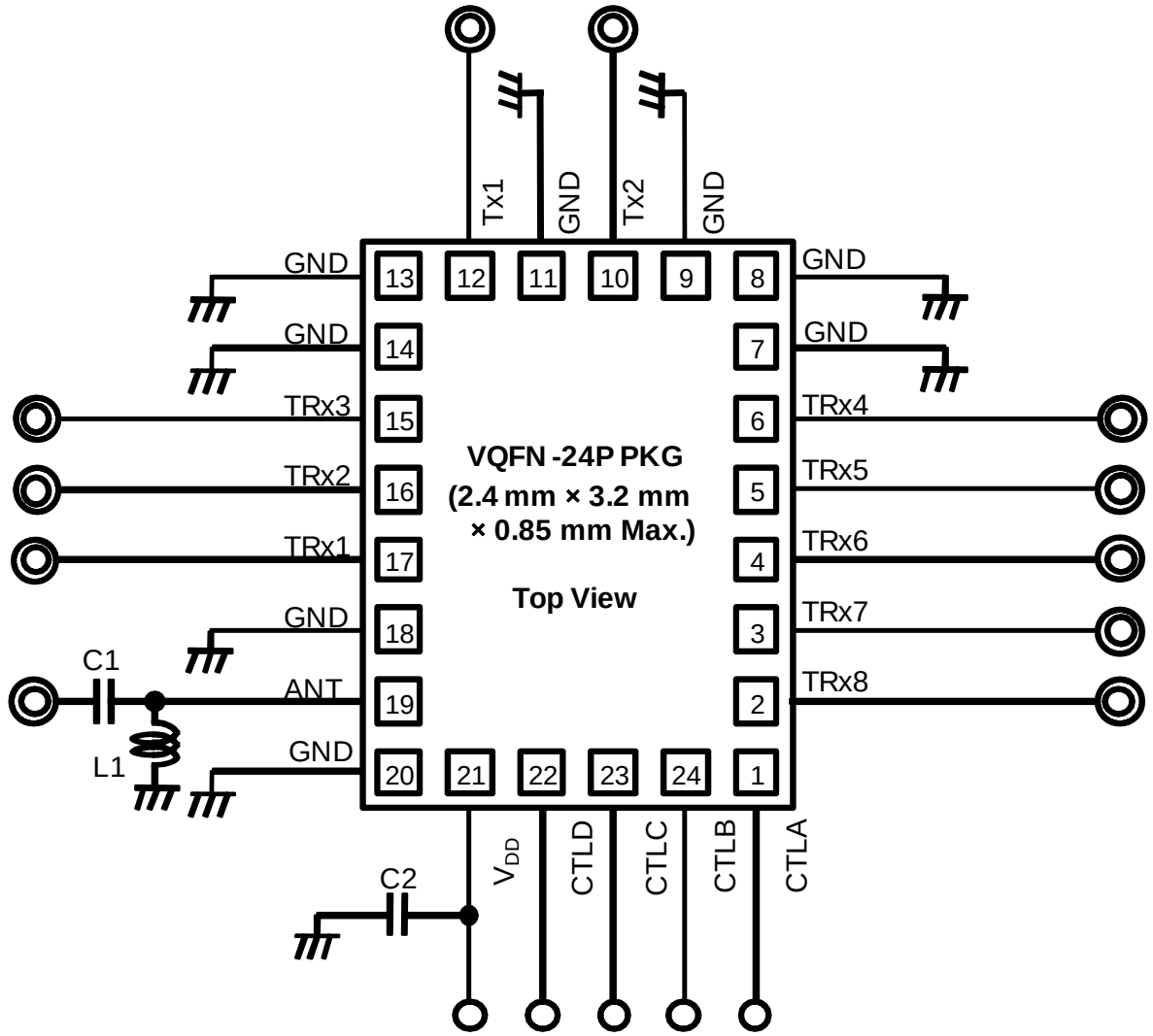
V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at TRx 24 dBm [MHz]	Jammer at ANT –20 dBm [MHz]	IM2 Product at TRx [MHz]				
Input IP2	IIP2	ANT-TRx1, 2, 3, 4, 5, 6, 7, 8	836.61	1718.61	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit 1

Recommended Circuit 1

Operation Frequency Range: 0.7 to 2.7 GHz



*1: No DC blocking capacitors are required on all RF ports.

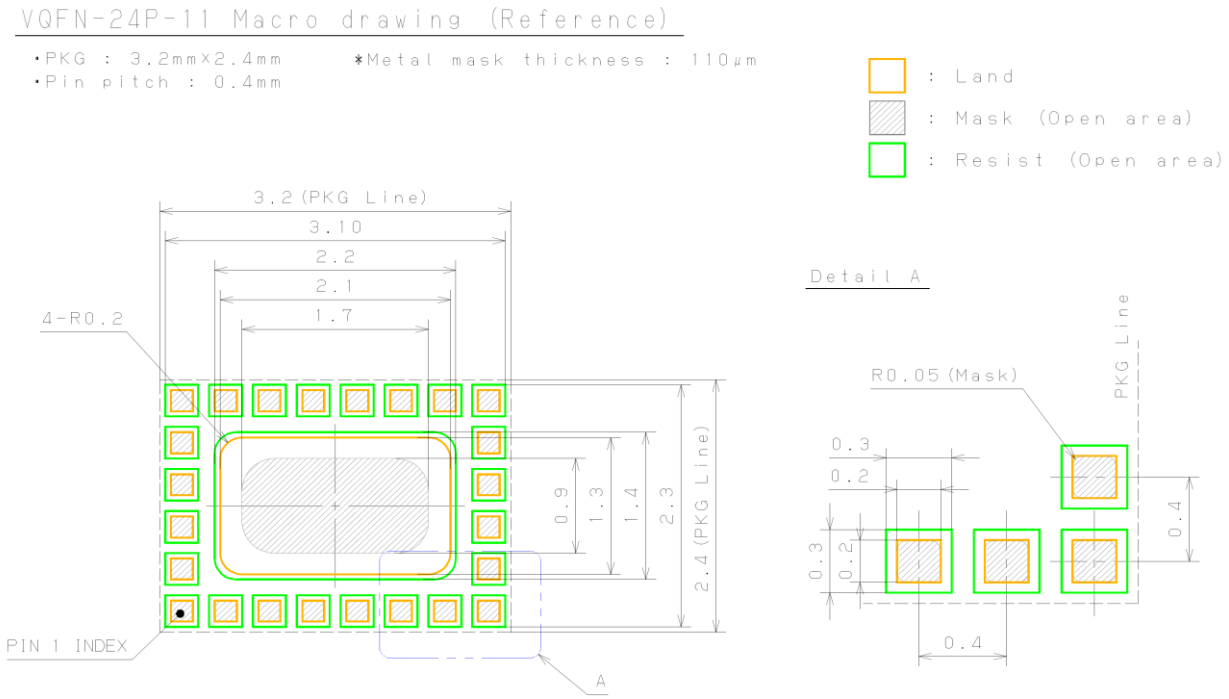
*2: DC levels of all RF ports are GND.

*3: L1 (22 nH) and C1 (10 pF) are recommended on Ant port for ESD protection.

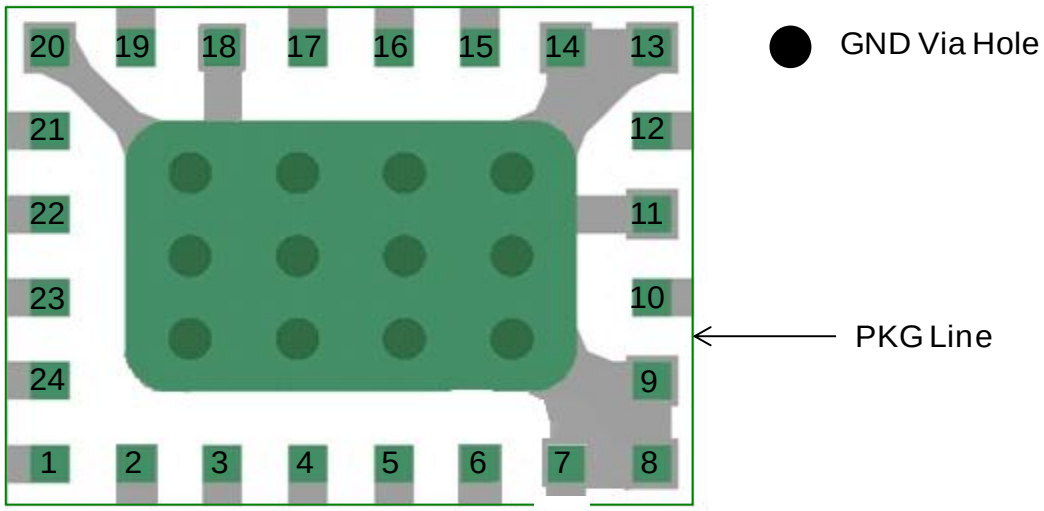
*4: C2 (100 pF) is recommended.

PCB Layout

Foot Pattern

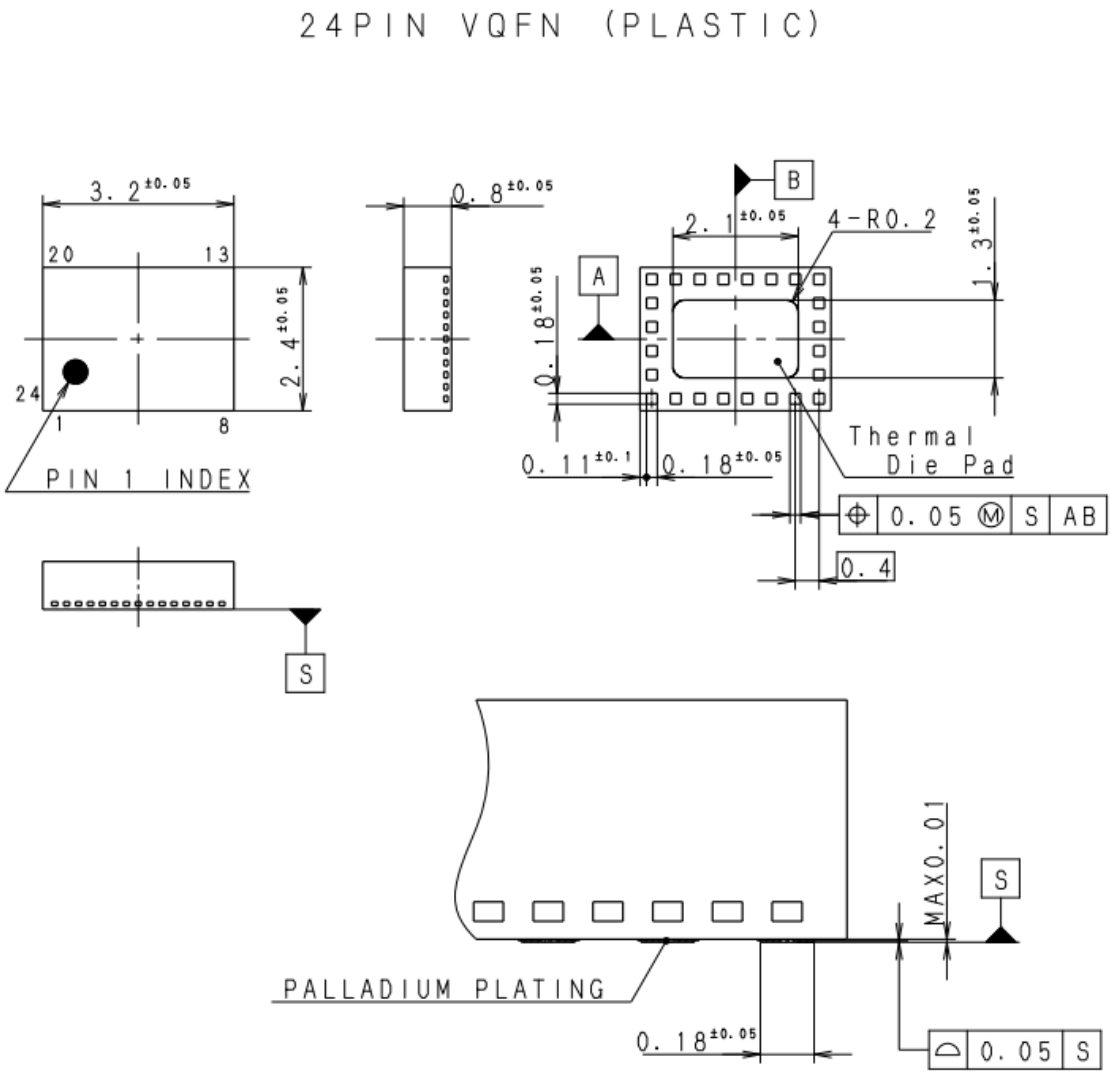


Recommended PCB Design



Package Outline

(Unit: mm)



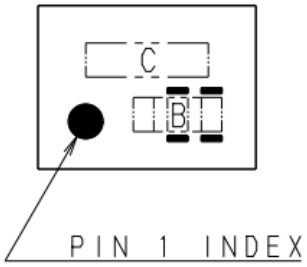
PACKAGE STRUCTURE

SONY CODE	VQFN-24P-11
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.018g

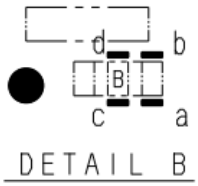
PART No. AP-4000-24Q49S		Rev. 0
ISSUED '12.02.15	REVISED	
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR	
REMARKS PKG CODE:ER-24-BB		

Marking



MARKING C: 3572

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ４文字）を配置する。
（４文字を超える場合は製品名省略標示規定に従う。）



< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 4 CHARACTERS) IN SECTION C.
(FOR MORE THAN 4 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits