SONY

SP4T + SP6T Antenna Switch Module for 6TRx/2Tx/2Rx with SPI I/F

CXM3580AUR

Description

The CXM3580AUR is a SP4T+ SP6T antenna switch module for GSM/UMTS/CDMA /LTE multi-mode handset. The CXM3580AUR has a +1.8 V CMOS compatible decoder with SPI function.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking Capacitor
(Application: GSM/UMTS/CDMA/LTE Multi-mode Handsets)

Features

- ◆ Low insertion loss: 0.37 dB (Typ.) TRx (Cellular band)
  0.95 dB (Typ.) TRx (IMT Tx band)
- ◆ High linearity: IIP3 = 68 dBm
- ◆ Low voltage operation: V_{DD} = 2.5 V
- ◆ Supports CMOS control for serial interface
- ◆ No DC blocking capacitor
- ◆ Small packing (size): UQFN-26P (2.6 mm × 3.4 mm × 0.625 mm Max.)
- ◆ Lead-free and RoHS compliant

Structure

- ◆ GaAs Junction gate pHEMT (JPHEMT) MMIC switch, CMOS decoder

This IC is ESD sensitive device. Special handling precautions are required.

E11614B1Z

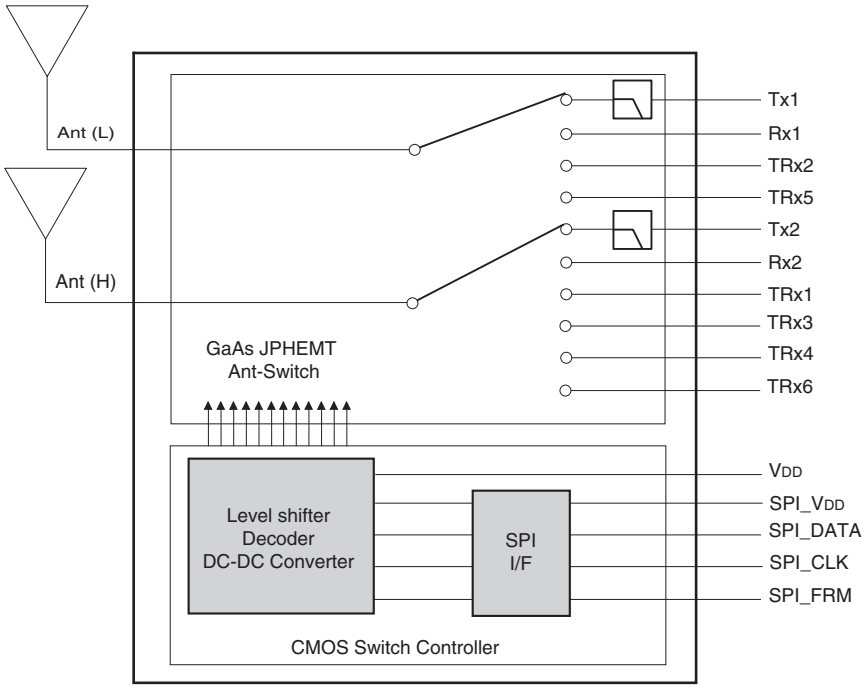
Absolute Maximum Ratings

(Ta = 25 ℃)

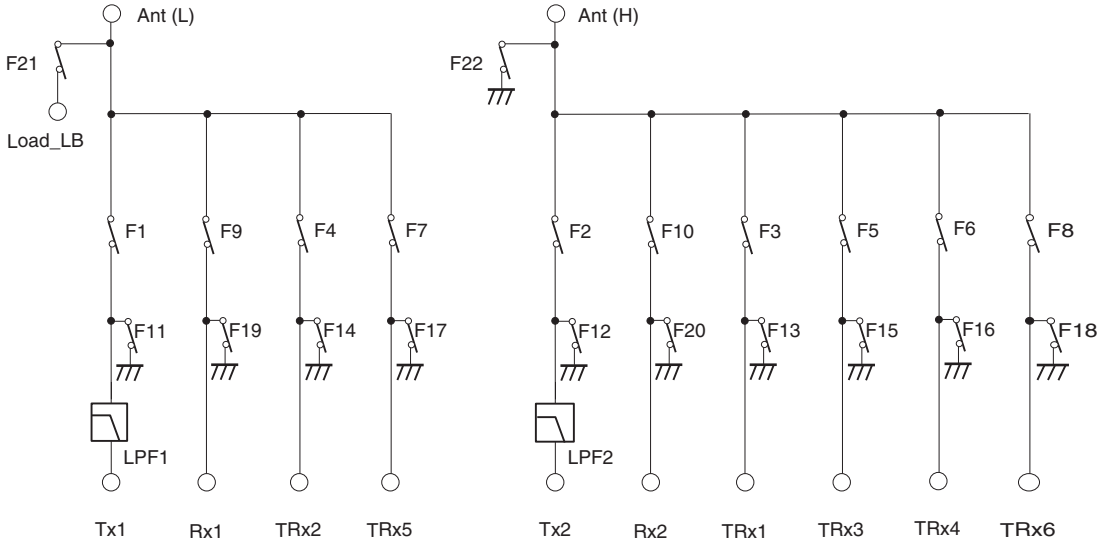
Bias voltage	V_{DD}	4	V
Supply voltage for SI	SPI_V_{DD}	3.6	V
Control voltage for SI	SPI_CLK, FRM, DATA	3.6	V
Input power max. (Tx1)		36	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (Tx2)		34	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (TRx)		32	dBm
Input power max. (Rx)		13	dBm
Operating temperature range		–35 to +90	℃
Storage temperature range		–65 to +150	℃

Block Diagram

SP4T + SP6T Antenna Switch Module with SPI



SP4T + SP6T 6TRx/2Tx/2Rx



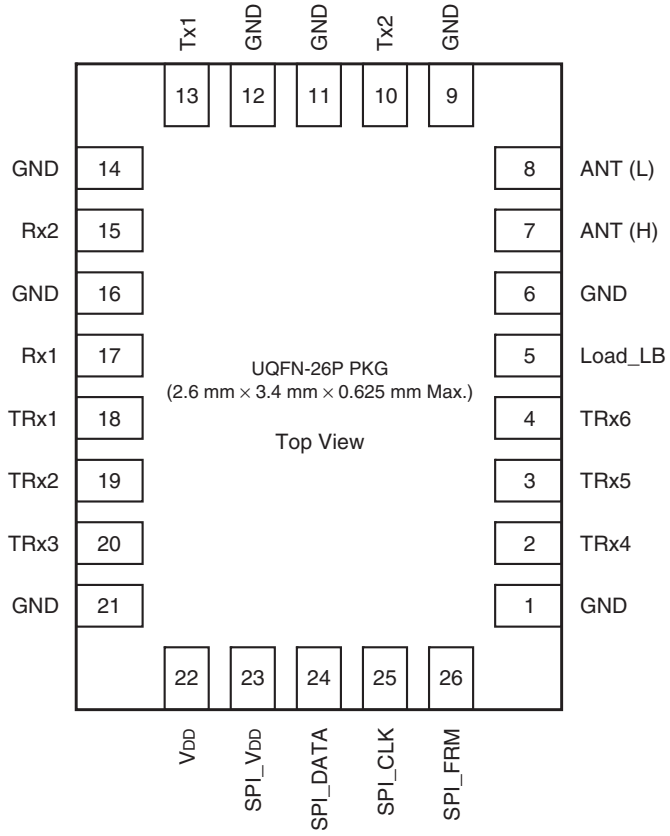
Truth Table

State	Active Path	SPI_Bit				SW State (*1)																					
		D14	D13	D12	D11	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22
1	Tx1-ANT (L)	0	0	1	0	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H
2	Tx2-ANT (H)	0	0	0	1	L	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	L
3	TRx1-ANT (H)	0	1	0	0	L	L	H	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	L
4	TRx2-ANT (L)	0	1	0	1	L	L	L	H	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H
5	TRx3-ANT (H)	0	1	1	0	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L
6	TRx4-ANT (H)	1	0	0	0	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	L
7	TRx5-ANT (L)	1	0	0	1	L	L	L	L	L	L	H	J	J	L	H	H	H	H	H	H	L	H	H	H	L	H
8	TRx6-ANT (H)	1	0	1	0	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	L	H	H	H	L
9	Rx1-ANT (L)	1	1	0	0	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L	H	L	H
10	Rx2-ANT (H)	1	1	0	1	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	L
11	Idle (*2)	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	Isolation	1	1	1	1	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

*1 State “L” means a switch “OFF”, state “H” means a switch “ON”.

*2 State “Idle” means that the DC/DC converter is “OFF”, and the switch paths are in an undefined state.

Pin Configuration



DC Bias Conditions

(Ta = 25 ℃)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.9	3.3	V
SPI_V_{DD}	1.35	1.8	1.98	V
SPI_Vctl (H)	SPI_V_{DD} × 0.7	—	SPI_V_{DD} + 0.3	V
SPI_Vctl (L)	–0.3	—	SPI_V_{DD} × 0.3	V

Electrical Characteristics

(V_{DD} = 2.5 V, Ta = 25 ℃)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	ANT (L) – Tx1	*1	—	1.00	1.25	dB
		ANT (H) – Tx2	*2	—	1.00	1.30	
		ANT (L) – Rx1	*3	—	0.35	0.45	
		ANT (H) – Rx2	*4	—	0.68	0.83	
		ANT (L) – TRx2	*5	—	0.35	0.45	
		ANT (L) – TRx5	*5	—	0.37	0.47	
		ANT (H) – TRx1	*6, *7	—	0.73	0.93	
		ANT (H) – TRx3	*6, *7	—	0.72	0.92	
		ANT (H) – TRx4	*6, *7	—	0.77	0.97	
		ANT (H) – TRx6	*6, *7	—	0.95	1.15	
VSWR	VSWR	All ports in Active paths	600 to 2170 MHz	—	—	1.50	—
Harmonics	2fo	ANT (L) – Tx1	*1	—	—	–45	dBm
	3fo			—	—	–42	
	2fo	ANT (H) – Tx2	*2	—	—	–50	
	3fo			—	—	–40	
	2fo	ANT (L) – TRx2, TRx5	*5	—	—	–50	
	3fo			—	—	–50	
	2fo	ANT (H) – TRx1, TRx3, TRx4, TRx6	*6	—	—	–50	
	3fo			—	—	–50	
Attenuation	ATT	ANT (L) – Tx1	1648 to 1830 MHz	30	—	—	dB
			2472 to 2745 MHz	27	—	—	
			3296 to 3520 MHz	20	—	—	
			3530 to 6340 MHz	15	—	—	
			6350 to 12750 MHz	20	—	—	
		ANT (H) – Tx2	3420 to 3820 MHz	25	—	—	
			5130 to 5730 MHz	25	—	—	
			6840 to 12750 MHz	20	—	—	
Inter modulation product power in Rx band	IMD2	ANT– TRx1, 2, 3, 4, 5, 6	*8, *9, *13, *17 *18	—	—	–105	dBm
			*8, *10, *14	—	—	–101	
	IMD3		*8, *11, *12, *15, *16, *19, *20	—	—	–105	
Input IP3	IIP3	ANT– TRx1, 2, 3, 4, 5, 6	*8, *21	—	68	—	dBm
			*8, *22	—	68	—	
Switching time	Ts		50 % Ctl to 90 % RF	—	3	5	μs
Supply current	IDD	Active or Isolation mode	V_{DD} = 2.5 V	—	—	0.40	mA
		Idel mode		—	—	20	μA

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	ANT (H) – ANT (L) (TRx1 Active)	824 MHz –960 MHz	22	25	—	dB
			1710 MHz –2170 MHz	16	19	—	
		TRx1 – TRx2 (TRx1 Active)	824 MHz –960 MHz	28	31	—	
			1710 MHz –2170 MHz	20	23	—	
		TRx1 – TRx3, 4, 5, 6 (TRx1 Active)	824 MHz –960 MHz	41	44	—	
			1710 MHz –2170 MHz	28	31	—	
		TRx1 – Rx1 (TRx1 Active)	824 MHz –960 MHz	32	35	—	
			1710 MHz –2170 MHz	21	24	—	
		TRx1 – Rx2 (TRx1 Active)	824 MHz –960 MHz	35	38	—	
			1710 MHz –2170 MHz	23	26	—	
		ANT (L) – ANT (H) (TRx2 Active)	824 MHz –960 MHz	23	26	—	
			1710 MHz –2170 MHz	17	20	—	
		TRx2 – TRx1, 3 (TRx2 Active)	824 MHz –960 MHz	29	32	—	
			1710 MHz –2170 MHz	21	24	—	
		TRx2 – Rx4, 5, 6 (TRx2 Active)	824 MHz –960 MHz	56	59	—	
			1710 MHz –2170 MHz	35	38	—	
		TRx2 – Rx1 (TRx2 Active)	824 MHz –960 MHz	37	40	—	
			1710 MHz –2170 MHz	28	31	—	
		TRx2 – Rx2 (TRx2 Active)	824 MHz –960 MHz	36	39	—	
			1710 MHz –2170 MHz	22	25	—	
		ANT (H) – ANT (L) (TRx3 Active)	824 MHz –960 MHz	22	25	—	
			1710 MHz –2170 MHz	16	19	—	
		TRx3 – TRx1, 4, 5, 6 (TRx3 Active)	824 MHz –960 MHz	42	45	—	
			1710 MHz –2170 MHz	28	31	—	
		TRx3 – TRx2 (TRx3 Active)	824 MHz –960 MHz	32	35	—	
			1710 MHz –2170 MHz	22	25	—	
		TRx3– Rx1 (TRx3 Active)	824 MHz –960 MHz	50	53	—	
			1710 MHz –2170 MHz	41	44	—	
		TRx3 – Rx2 (TRx3 Active)	824 MHz –960 MHz	38	41	—	
			1710 MHz –2170 MHz	20	23	—	
		ANT (H) – ANT (L) (TRx4 Active)	824 MHz –960 MHz	22	25	—	
			1710 MHz –2170 MHz	16	19	—	
		TRx4 – TRx1, 2, 3 (TRx4 Active)	824 MHz –960 MHz	50	53	—	
			1710 MHz –2170 MHz	35	38	—	
		TRx4 – TRx5, 6 (TRx4 Active)	824 MHz –960 MHz	32	35	—	
			1710 MHz –2170 MHz	20	23	—	
		TRx4 – Rx1 (TRx4 Active)	824 MHz –960 MHz	55	58	—	
			1710 MHz –2170 MHz	44	47	—	
		TRx4 – Rx2 (TRx4 Active)	824 MHz –960 MHz	43	46	—	
			1710 MHz –2170 MHz	27	30	—	

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	ANT (L) – ANT (H) (TRx5 Active)	824 MHz –960 MHz	23	26	—	dB
			1710 MHz –2170 MHz	17	20	—	
		TRx5 – TRx1, 2, 3 (TRx5 Active)	824 MHz –960 MHz	57	60	—	
			1710 MHz –2170 MHz	34	37	—	
		TRx5 – TRx4, 6 (TRx5 Active)	824 MHz –960 MHz	32	35	—	
			1710 MHz –2170 MHz	22	25	—	
		TRx5 – Rx1 (TRx5 Active)	824 MHz –960 MHz	55	58	—	
			1710 MHz –2170 MHz	38	41	—	
		TRx5 – Rx2 (TRx5 Active)	824 MHz –960 MHz	40	43	—	
			1710 MHz –2170 MHz	28	31	—	
		ANT (H) – ANT (L) (TRx6 Active)	824 MHz –960 MHz	21	24	—	
			1710 MHz –2170 MHz	15	18	—	
		TRx6 – TRx1, 2, 3 (TRx6 Active)	824 MHz –960 MHz	53	56	—	
			1710 MHz –2170 MHz	34	37	—	
		TRx6 – TRx4 (TRx6 Active)	824 MHz –960 MHz	44	47	—	
			1710 MHz –2170 MHz	25	28	—	
		TRx6 – TRx5 (TRx6 Active)	824 MHz –960 MHz	33	36	—	
			1710 MHz –2170 MHz	21	24	—	
		TRx6 – Rx1 (TRx6 Active)	824 MHz –960 MHz	59	62	—	
			1710 MHz –2170 MHz	41	44	—	
		TRx6 – Rx2 (TRx6 Active)	824 MHz –960 MHz	41	44	—	
			1710 MHz –2170 MHz	31	34	—	
		ANT (L) – ANT (H) (Tx1 Active)	824 MHz –915 MHz	22	25	—	
		Tx1 – TRx1, 2, 3, 4, 5, 6 (Tx1 Active)	824 MHz –915 MHz	55	58	—	
		Tx1 – Rx1, Rx2 (Tx1 Active)	824 MHz –915 MHz	35	38	—	
		Tx1 – Tx2 (Tx1 Active)	824 MHz –915 MHz	20	23	—	
			1648 MHz –1830 MHz	23	26	—	
		ANT (H) – ANT (L)	1710 MHz –1910 MHz	16	19	—	
		Tx2 – TRx1 (Tx2 Active)	1710 MHz –1910 MHz	37	40	—	
		Tx2 – TRx2, 3 (Tx2 Active)	1710 MHz –1910 MHz	41	44	—	
		Tx2 – TRx4, 5 (Tx2 Active)	1710 MHz –1910 MHz	34	37	—	
		Tx2 – TRx6 (Tx2 Active)	1710 MHz –1910 MHz	32	35	—	
		Tx2 – Rx1 (Tx2 Active)	1710 MHz –1910 MHz	41	44	—	
		Tx2 – Rx2 (Tx2 Active)	1710 MHz –1910 MHz	27	30	—	

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	Tx2 – Tx1 (Tx2 Active)	1710 MHz –1910 MHz	27	30	—	dB
		ANT (L) – ANT (H) (Rx1 Active)	869 MHz –960 MHz	22	25	—	
			1805 MHz –1990 MHz	17	20	—	
		ANT (H) – ANT (L) (Rx2 Active)	869 MHz –960 MHz	22	25	—	
			1805 MHz –1990 MHz	16	19	—	
		Tx1 – ANT (L), ANT (H)	824MHz –915 MHz	29	32	—	
		Tx2 – ANT (L), ANT (H)	1710 MHz –1910 MHz	22	25	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of GSM Tx/Rx (GSM).

*1 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
*2 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
*3 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
*4 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)

Corresponding Band of TRx (UMTS/CDMA).

*5 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 6, Band 8)
*6 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 4 Tx)
*7 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
*8 Measured with the recommended circuit

IMD Condition

Band	fRx on TRx	fRx +20dBm on TRx	fBlocker –15dBm on Ant		IMD Condition
Band I	2140 MHz	1950 MHz	IMD2 (fRx-fTx)	190 MHz	*9
			IMD2 (fRx+fTx)	4090 MHz	*10
			IMD3 (2fTx-fRx)	1760 MHz	*11
			IMD3 (2fTx+fRx)	6040 MHz	*12
Band II	1960 MHz	1880 MHz	IMD2 (fRx-fTx)	80 MHz	*13
			IMD2 (fRx+fTx)	3840 MHz	*14
			IMD3 (2fTx-fRx)	1800 MHz	*15
			IMD3 (2fTx+Rx)	5720 MHz	*16
Band V	880 MHz	835 MHz	IMD2 (fRx-fTx)	45 MHz	*17
			IMD2 (fRx+fTx)	1715 MHz	*18
			IMD3 (2fTx-fRx)	790 MHz	*19
			IMD3 (2fTx+fRx)	2550 MHz	*20

IIP3 Condition

Band	f1 +27 dBm on TRx	f2 +27 dBm on TRx	IIP3 Condition IIP3 = (3 × Pout – IM3)/2
Band I	1950 MHz	1951 MHz	*21
Band V	835 MHz	836 MHz	*22

Triple Beat Ratio

(V_{DD} = 2.5 V, Ta = 25 ˚C)

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
Triple Beat Ratio	TBR		Tx1 at TRx* 21.5 dBm [MHz]	Tx2 at TRx* 21.5 dBm [MHz]	Jammer at Ant –30 dBm [MHz]	Triple Beat Product at TRx* [MHz]				dBc
		ANT-TRx1, 2, 3, 4, 5, 6	835.5	836.5	881.5	881.5±1	81	—	—	
			1880	1881	1960	1960±1	81	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

IIP2

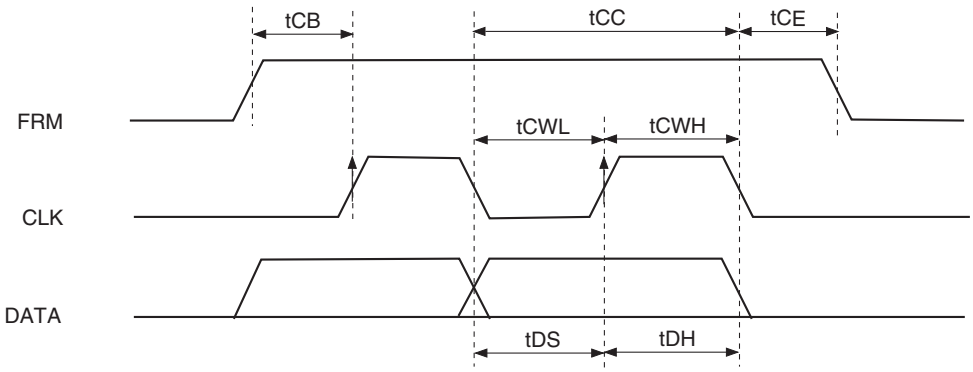
(V_{DD} = 2.5 V, Ta = 25 ˚C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Input IP2	IIP2		Tx at TRx* 24 dBm [MHz]	Jammer at Ant –20 dBm [MHz]	IM2 Product at TRx* [MHz]				dBm
		ANT-TRx1, 2, 3, 4, 5, 6	836.61	1718.61	881.61	113.5	—	—	
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

SPI Timing Characteristic

Item	Symbol	Condition	SPEC			Unit
			Min.	Min.	Min.	
SPI bias current	SPI_I_{DD}	SPI_V_{DD} = 1.8 V	—	200	400	μA
SPI Ctrl current	SPI_Ictl	SPI_V_{DD} = 1.8 V	—	—	10	μA
SPI_Enable	SPI_EN	SPI_V_{DD} ↑ (90 %)	10	—	—	μs
Clock freaquency	CLK_Freq	SPI_V_{DD} Enable	—	—	26	MHz
Clock cycle	tCC	CLK_Freq = 26 MHz	34	38.4	42	ns
Clock begin time	tCB		tCC/2	—	—	ns
Clock end time	tCE		tCC/2	—	—	ns
Clock width High	tCWH		tCC × 0.4	—	—	ns
Clock width Low	tCWL		tCC × 0.4	—	—	ns
Data setup time	tDS		5	—	—	ns
Data hold time	tDH		5	—	—	ns
SPI_V_{DD} rise time	T_{SPI_VDD} Rise	10 % to 90 % SPI_V_{DD}	2.2	—	—	μs



SPI Control Specification

Item	Specification
Address bits	14 bits
Data bits	16 bits
Total bits	30 bits total
Clock edge (data sampling)	Rising edge

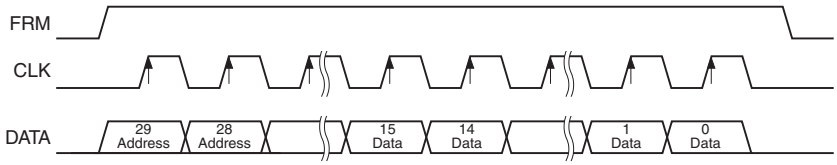
Address		Control Data	
29	16	15	0
MSB			LSB

Port symbol	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R/W	Device address								Register address				
Idle1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Tx1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Tx2	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx2	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx3	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx4	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx5	0	0	0	1	0	0	0	1	0	0	0	0	0	0
TRx6	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Rx1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Rx2	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Isolation	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Idle2	0	1	1	1	1	1	1	1	1	1	1	1	1	1

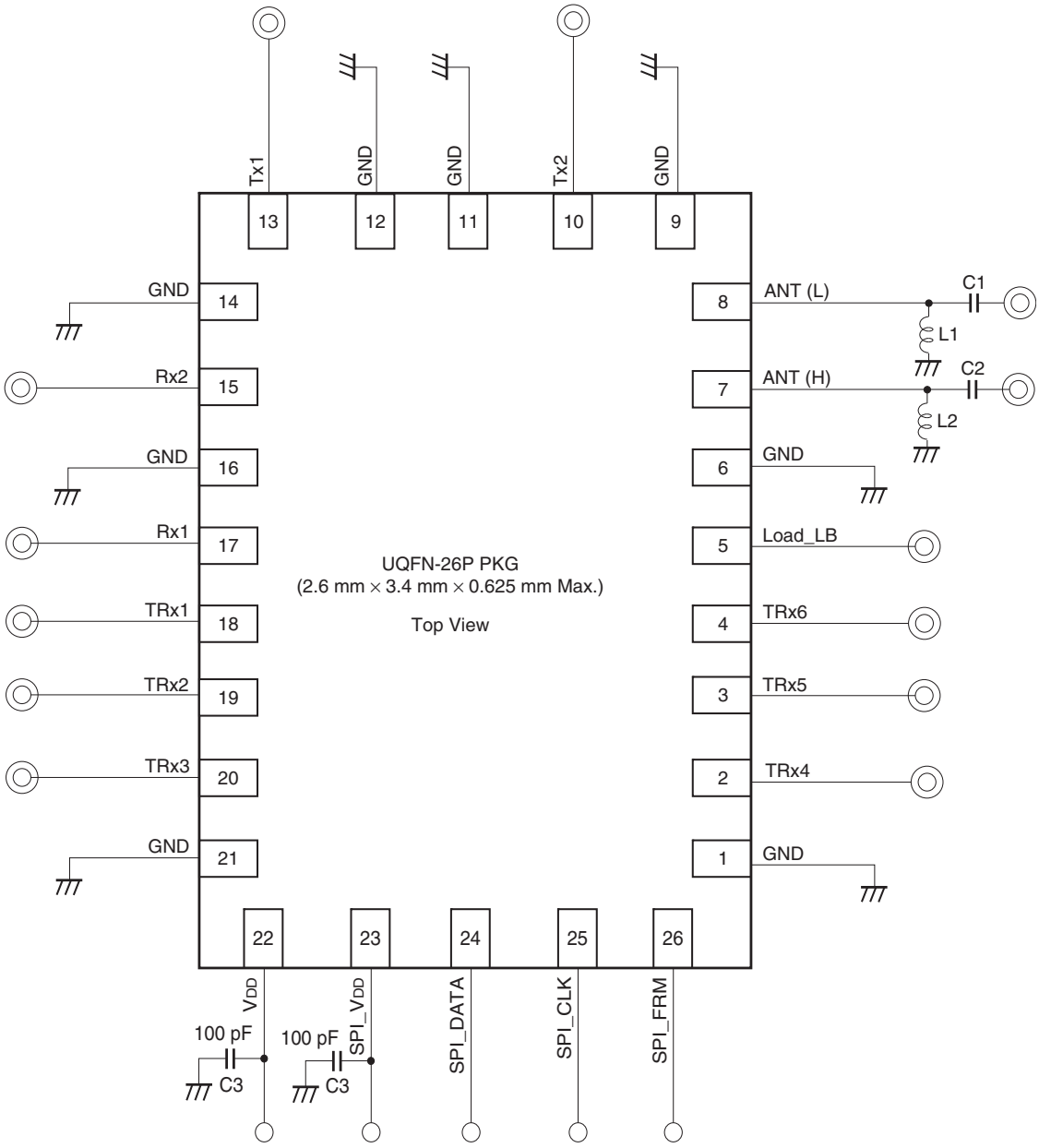
Port symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Idle1	X	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X
Tx1	X	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X
Tx2	X	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X
TRx1	X	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X
TRx2	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X
TRx3	X	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X
TRx4	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X
TRx5	X	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X
TRx6	X	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X
Rx1	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X
Rx2	X	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X
Isolation	X	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X
Idle2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

* Either idle state D11 to D14 is 0000, or XXXX.

Clock Block Diagram

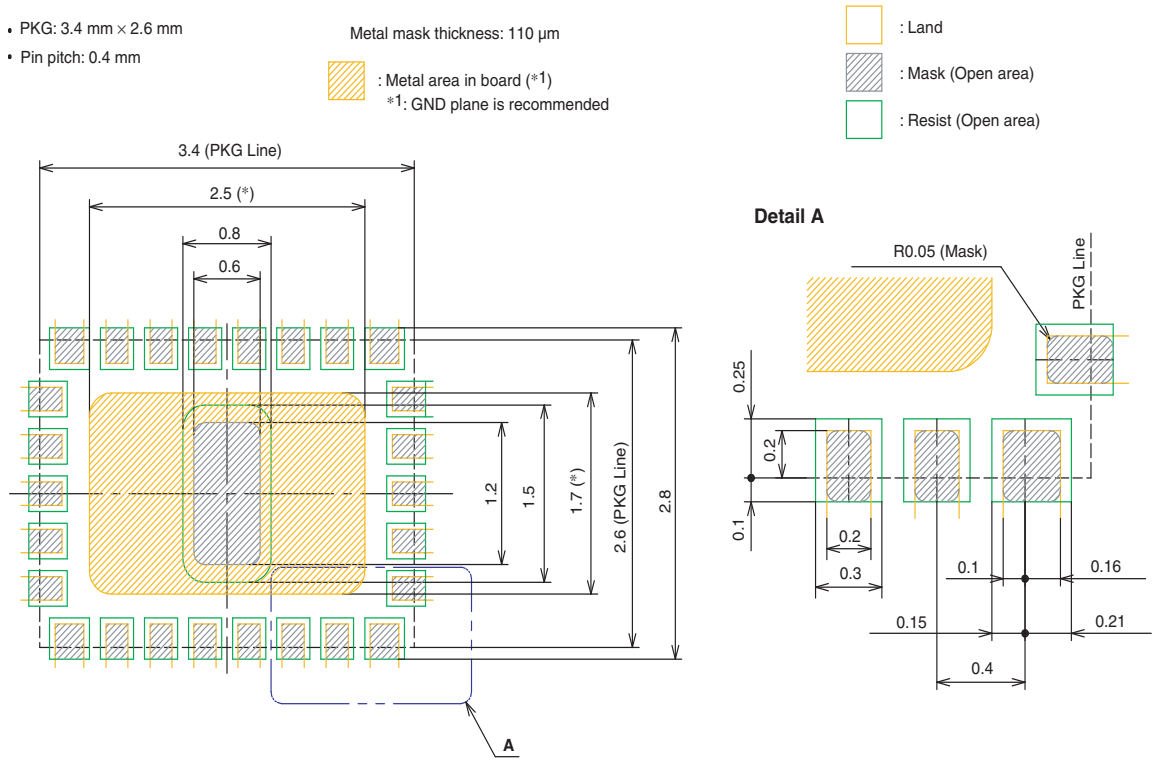


Recommended Circuit

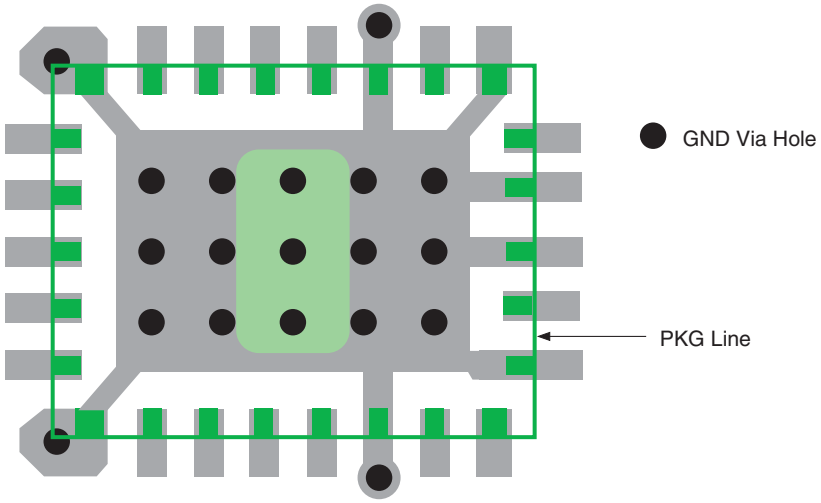


Note) 1. No DC blocking capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 (22 nH) and C1 (12 pF) are recommended on Ant port for ESD protection.
4. L2 (12 nH) and C2 (12 pF) are recommended on Ant port for ESD protection.
5. C3 capacitor (100 pF) is recommended.

Recommended Land Pattern



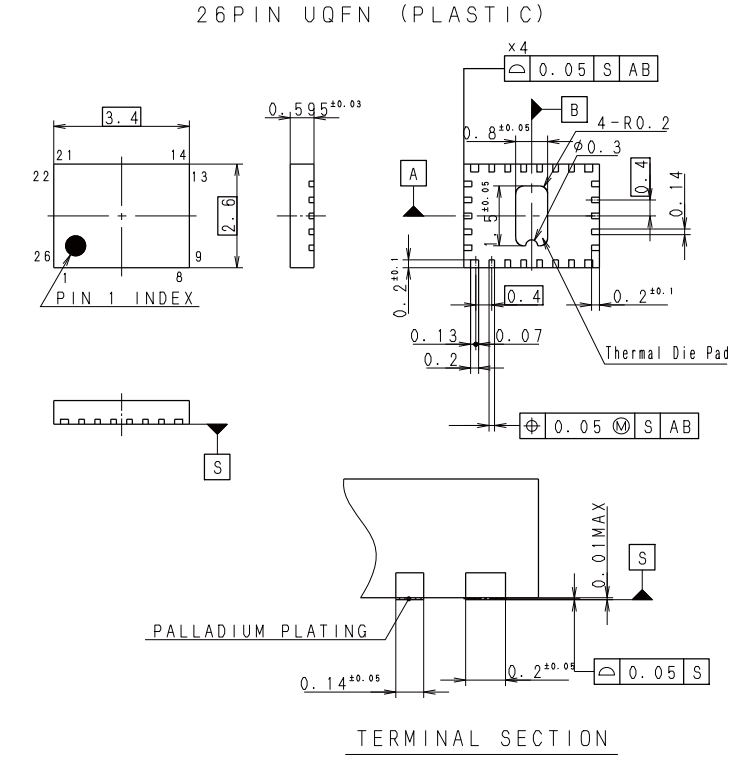
PCB GND Design for UQFN-26P (Image)



Package Outline

(Unit: mm)

Product Code: 875340753



Note:Terminal burr height 0.05mm MAX.

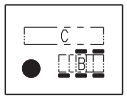
SONY CODE	UQFN-26P-541
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

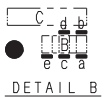
PART No. AP-2000-26QNBE3	Rev. 0
ISSUED '11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-26-CBE	

Marking



MARKING C:3580A

注1) B部はロット番号(Max3文字で通し記号)を配置する。
(規定文字数未満につき省略は省略規定に従う。)
製造年は下記2進法ビット方式により表示する。)
a部年コード(2進法ビット方式の1ビット目を表示)を配置する。
b部年コード(2進法ビット方式の2ビット目を表示)を配置する。
c部年コード(2進法ビット方式の3ビット目を表示)を配置する。
d部年コード(2進法ビット方式の4ビット目を表示)を配置する。
注2) C部は製品名(Max5文字)を配置する。
(5文字を超える場合は製品名省略標示規定に従う。)
注3) e部は組立場所表記を配置する。



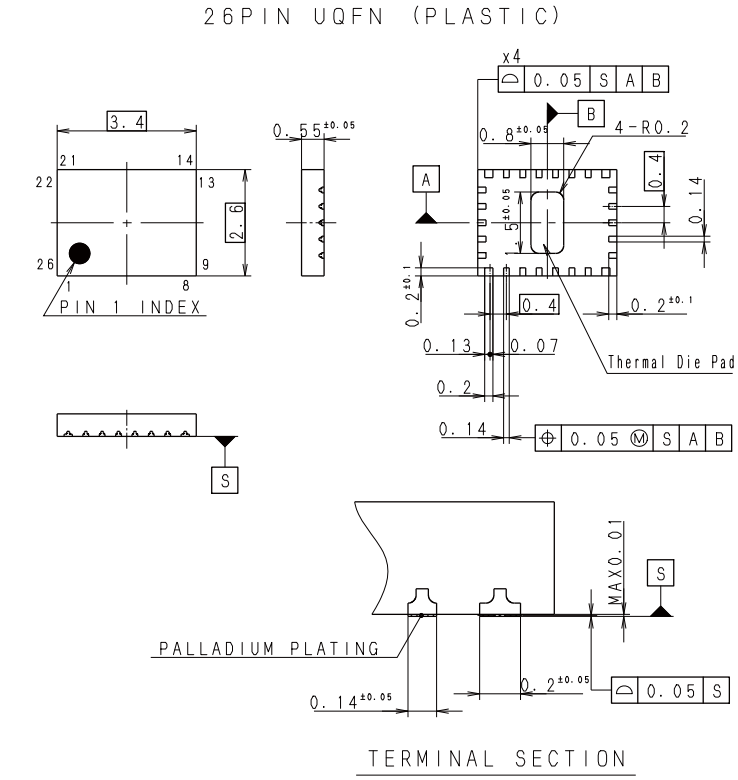
DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) ASSEMBLY PLACE IN SECTION e.

Package Outline

(Unit: mm)

Product Code: 875339308



Note:Terminal burr height 0.05mm MAX.

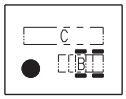
SONY CODE	UQFN-26P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

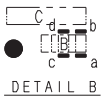
PART No. AP-4000-26011S	Rev. 0
ISSUED '11.06.20	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CORD:UR-26-1	

Marking



MARKING C: 3580A

注1) B部はロット番号（Max3文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記2進法ビット方式により表示する。）
a部年コード（2進法ビット方式の1ビット目を表示）を配置する。
b部年コード（2進法ビット方式の2ビット目を表示）を配置する。
c部年コード（2進法ビット方式の3ビット目を表示）を配置する。
d部年コード（2進法ビット方式の4ビット目を表示）を配置する。
注2) C部は製品名（Max5文字）を配置する。
（5文字を超える場合は製品名省略標示規定に従う。）
注3) マーク深さは、MAX0.05mmの事.



< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm