SONY

SP4T + SP5T Antenna Switch Module for GSM/UMTS/CDMA/LTE Multi-mode

CXM3580UR

Description

The CXM3580UR is a SP4T+ SP5T antenna switch module for GSM/UMTS/CDMA /LTE multi-mode handset.
The CXM3580UR has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder.
The Sony GaAs Junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking capacitor.
（Application: GSM/UMTS/CDMA/LTE multi-mode handset）

Features

- ◆ Low insertion loss: 0.40 dB (Typ.) TRx (Cellular band)
  0.58 dB (Typ.) TRx (IMT Tx band)
- ◆ High linearity: IIP3 = 68 dBm
- ◆ Low voltage operation: V_{DD} = 2.5 V
- ◆ No DC blocking capacitor
- ◆ Small packing (size): UQFN-26P (2.6 mm × 3.4 mm × 0.625 mm Max.)
- ◆ Lead-free and RoHS compliant

Structure

- ◆ GaAs Junction gate pHEMT (JPHEMT) MMIC switch, CMOS decoder

This IC is ESD sensitive device. Special handling precautions are required.

E11510A1Z

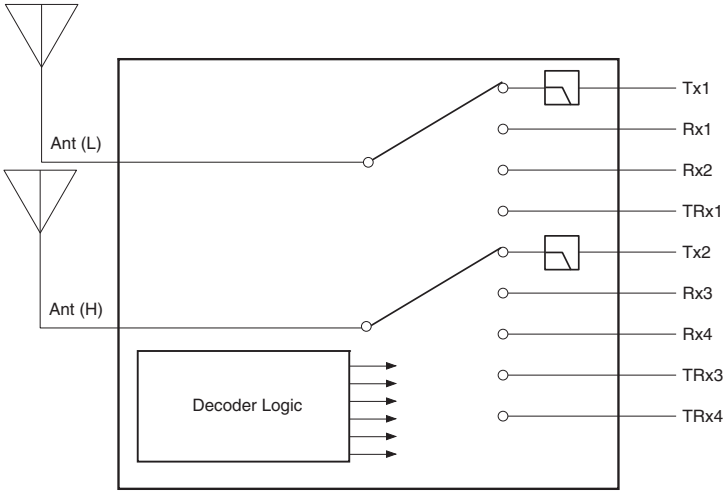
Absolute Maximum Ratings

(Ta = 25 ℃)

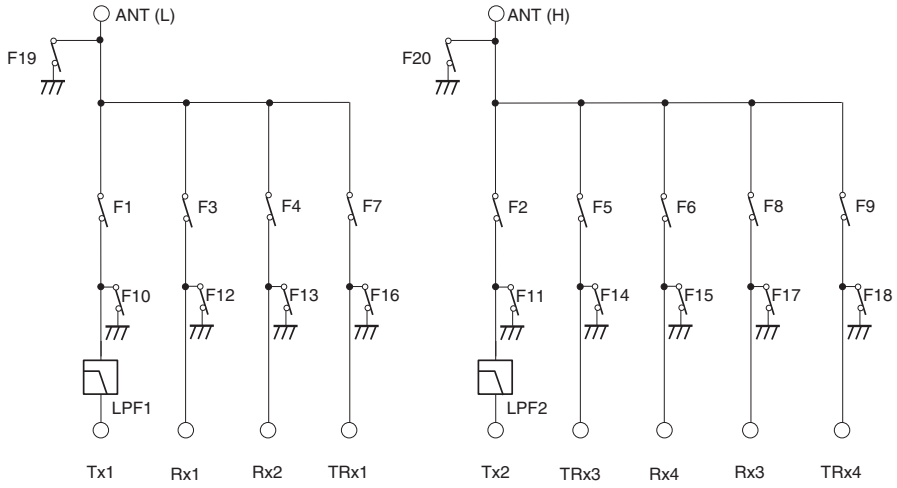
Bias voltage	V_{DD}	4	V
Control voltage	Vctl	4	V
Input power max. (Tx1)		36	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (Tx2)		34	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (TRx)		32	dBm
Input power max. (Rx)		13	dBm
Operating temperature range		–35 to +90	℃
Storage temperature range		–65 to +150	℃

Block Diagram

SP4T + SP5T Antenna Switch Module



SP4T + SP5T 3TRx/2Tx/4Rx

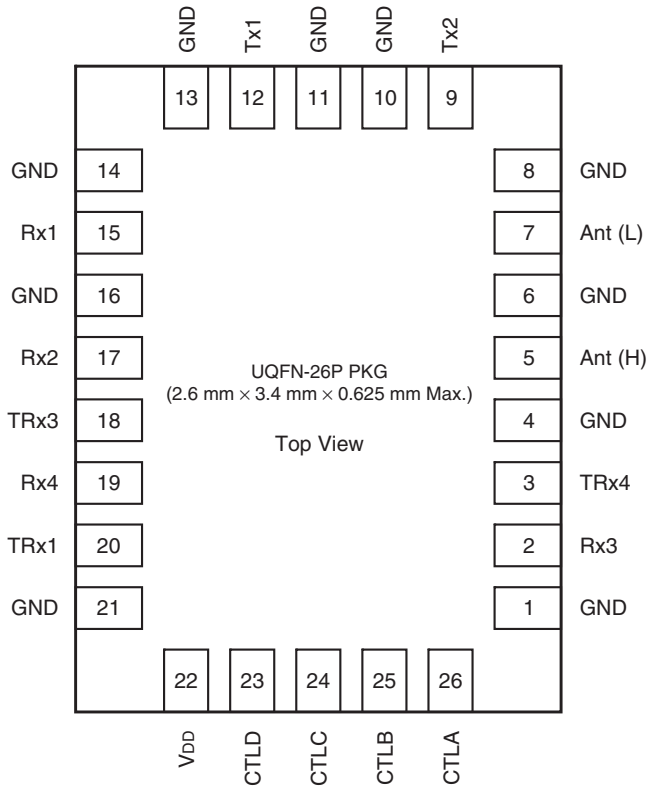


Truth Table

State	Active Path	CTL Sate				SW State (*1)																			
		CTLA	CTLB	CTLC	CTLD	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20
1	Tx1-ANT (L)	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H
2	Tx2-ANT (H)	H	L	L	L	L	H	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L
3	Rx1-ANT (L)	L	L	L	L	L	L	H	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	L	H
4	Rx2-ANT (L)	L	L	H	L	L	L	L	H	L	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H
5	TRx3-ANT (H)	L	H	H	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L	H	H	H	H	H	L
6	Rx4-ANT (H)	J	H	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	L	H	H	H	H	L
7	TRx1-ANT (L)	H	L	H	J	L	L	L	L	L	L	H	J	J	H	H	H	H	H	H	L	H	H	L	H
8	Rx3-ANT (H)	H	L	H	H	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	L	H	H	L
9	TRx4-ANT (H)	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	L

*1 State “L” means a switch “OFF”, state “H” means a switch “ON”.

Pin Configuration



DC Bias Conditions

(Ta = 25 ℃)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.8	3.3	V
Vctl (H)	1.35	1.8	3.1	V
Vctl (L)	0	—	0.45	V

Electrical Characteristics

(V_{DD} = 2.5 V, Ta = 25 ℃)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant (L) – Tx1	*1	—	1.00	1.25	dB
		Ant (H) – Tx2	*2	—	0.95	1.25	
		Ant (L) – Rx1	*3	—	0.63	0.73	
		Ant (L) – Rx2	*3	—	0.63	0.73	
		Ant (H) – Rx3	*4	—	0.55	0.70	
		Ant (H) – Rx4	*4	—	0.82	0.97	
		Ant (L) – TRx1	*5	—	0.40	0.50	
		Ant (H) – TRx3	*6, *7	—	0.53	0.73	
		Ant (H) – TRx4	*6, *7	—	0.58	0.78	
VSWR	VSWR	All ports in Active paths	600 to 2170 MHz	—	—	1.50	—
Harmonics	2fo	Ant (L) – Tx1	*1	—	—	–40	dBm
	3fo			—	—	–43	
	2fo	Ant (H) – Tx2	*2	—	—	–45	
	3fo			—	—	–40	
	2fo	Ant (L) – Tx1	*5	—	—	–50	
	3fo			—	—	–50	
	2fo	Ant (H) – TRx3, TRx4	*6	—	—	–50	
	3fo			—	—	–50	
Attenuation	ATT	Ant (L) – Tx1	1648 to 1830 MHz	30	—	—	dB
			2472 to 2745 MHz	27	—	—	
			3296 to 3660 MHz	20	—	—	
			4120 to 12750 MHz	17	—	—	
		Ant (H) – Tx2	3420 to 3820 MHz	25	—	—	
			5130 to 5730 MHz	25	—	—	
			6840 to 12750 MHz	20	—	—	
Inter modulation product power in Rx band	IMD2	Ant – TRx1, TRx3, TRx4	*8, *9, *10, *13, *14, *17, *18	—	—	–105	dBm
	IMD3		*8,*11,*12, *15, *16, *19, *20	—	—	–105	
Input IP3	IIP3	Ant – TRx1, TRx3, TRx4	*8, *21	—	68	—	dBm
			*8, *22	—	68	—	
Switching time	Ts		50 % Ctl to 90 % RF	—	3	5	μs
Control current	Ictl		V_{ctl} = 1.8 V	—	5	20	μA
Supply current	IDD		V_{DD} = 2.5 V	—	0.20	0.40	mA

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	Ant (L) – Ant (H) (TRx1 Active)	824 MHz –960 MHz	33	36	—	dB
			1710 MHz –2170 MHz	28	31	—	
		TRx1 – TRx3, TRx4 (TRx1 Active)	824 MHz –960 MHz	43	46	—	
			1710 MHz –2170 MHz	29	32	—	
		TRx1 – Rx1, Rx2, Rx3 (TRx1 Active)	824 MHz –960 MHz	50	53	—	
			1710 MHz –2170 MHz	40	43	—	
		TRx1 – Rx4 (TRx1 Active)	824 MHz –960 MHz	31	34	—	
			1710 MHz –2170 MHz	23	26	—	
		Ant (H) – Ant (L) (TRx3 Active)	824 MHz –960 MHz	36	39	—	
			1710 MHz –2170 MHz	28	31	—	
		TRx3 – TRx1, TRx4 (TRx3 Active)	824 MHz –960 MHz	44	47	—	
			1710 MHz –2170 MHz	36	39	—	
		TRx3 – Rx1, Rx3 (TRx3 Active)	824 MHz –960 MHz	51	54	—	
			1710 MHz –2170 MHz	39	42	—	
		TRx3 – Rx2, Rx4 (TRx3 Active)	824 MHz –960 MHz	33	36	—	
			1710 MHz –2170 MHz	25	28	—	
		Ant (H) – Ant (L) (TRx4 Active)	824 MHz –960 MHz	38	41	—	
			1710 MHz –2170 MHz	29	32	—	
		TRx4 – TRx1, TRx3 (TRx4 Active)	824 MHz –960 MHz	57	60	—	
			1710 MHz –2170 MHz	33	36	—	
		TRx4 – Rx1, Rx2, Rx4 (TRx4 Active)	824 MHz –960 MHz	63	66	—	
			1710 MHz –2170 MHz	43	46	—	
		TRx4 – Rx3 (TRx4 Active)	824 MHz –960 MHz	31	34	—	
			1710 MHz –2170 MHz	23	26	—	
		Ant (L) – Ant (H) (Rx1, Rx2 Active)	869 MHz –960 MHz	34	37	—	
			1805 MHz –1990 MHz	29	32	—	
		Ant (H) – Ant (L) (Rx3, Rx4 Active)	869 MHz –960 MHz	36	39	—	
			1805MHz –1990 MHz	29	32	—	
		Tx1 – Ant (L), Ant (H) (Rx1, Rx2, Rx3, Rx4)	824 MHz –915MHz	27	30	—	
		Tx2 – Ant (L), Ant (H) (Rx1, Rx2, Rx3, Rx4)	1710 MHz –1910 MHz	23	26	—	
		Ant (L) – Ant (H) (Tx1 Active)	824 MHz –915 MHz	34	37	—	
		Tx1 – Rx1, Rx2, Rx3, Rx4 (Tx1 Active)	824MHz – 915 MHz	47	50	—	
		Tx1 – TRx1, TRx3, TRx4 (Tx1 Active)	824 MHz –915 MHz	61	64	—	
		Tx1 – Tx2 (Tx1 Active)	824 MHz –915 MHz	21	24	—	
			1648 MHz –1830 MHz	22	25	—	

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	Ant (H) – Ant (L) (Tx2 Active)	1710 MHz –1910 MHz	27	30	—	dB
		Tx2 – Rx1, Rx2, Rx3, Rx4 (Tx2 Active)	1710 MHz –1910 MHz	45	48	—	
		Tx2 – TRx1, TRx4 (Tx2 Active)	1710 MHz –1910 MHz	46	49	—	
		Tx2 – TRx3 (Tx2 Active)	1710 MHz –1910 MHz	37	40	—	
		Tx2 – Tx1 (Tx2 Active)	1710 MHz –1910 MHz	26	29	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of GSM Tx/Rx (GSM).

*1 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
*2 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
*3 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
*4 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)

Corresponding Band of TRx (UMTS/CDMA).

*5 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 6, Band 8)
*6 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 4 Tx)
*7 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
*8 Measured with the recommended circuit

IMD Condition

Band	fRx on TRx	fRx +20dBm on TRx	fBlocker –15dBm on Ant		IMD Condition
Band I	2140 MHz	1950 MHz	IMD2 (fRx-fTx)	190 MHz	*9
			IMD2 (fRx+fTx)	4090 MHz	*10
			IMD3 (2fTx-fRx)	1760 MHz	*11
			IMD3 (2fTx+fRx)	6040 MHz	*12
Band II	1960 MHz	1880 MHz	IMD2 (fRx-fTx)	80 MHz	*13
			IMD2 (fRx+fTx)	3840 MHz	*14
			IMD3 (2fTx-fRx)	1800 MHz	*15
			IMD3 (2fTx+Rx)	5720 MHz	*16
Band V	880 MHz	835 MHz	IMD2 (fRx-fTx)	45 MHz	*17
			IMD2 (fRx+fTx)	1715 MHz	*18
			IMD3 (2fTx-fRx)	790 MHz	*19
			IMD3 (2fTx+fRx)	2550 MHz	*20

IIP3 Condition

Band	f1 +27 dBm on TRx	f2 +27 dBm on TRx	IIP3 Condition IIP3 = (3 × Pout – IM3)/2
Band I	1950 MHz	1951 MHz	*21
Band V	835 MHz	836 MHz	*22

Triple Beat Ratio

(V_{DD} = 2.5 V, Ta = 25 ˚C)

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
Triple Beat Ratio	TBR		Tx1 at TRx*1 21.5 dBm [MHz]	Tx2 at TRx*1 21.5 dBm [MHz]	Jammer at Ant –30 dBm [MHz]	Triple Beat Product at TRx*1 [MHz]				dBc
		Ant-TRx1,3, 4	835.5	836.5	881.5	881.5±1	81	—	—	
			1880	1881	1960	1960±1	81	—	—	

*1 Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

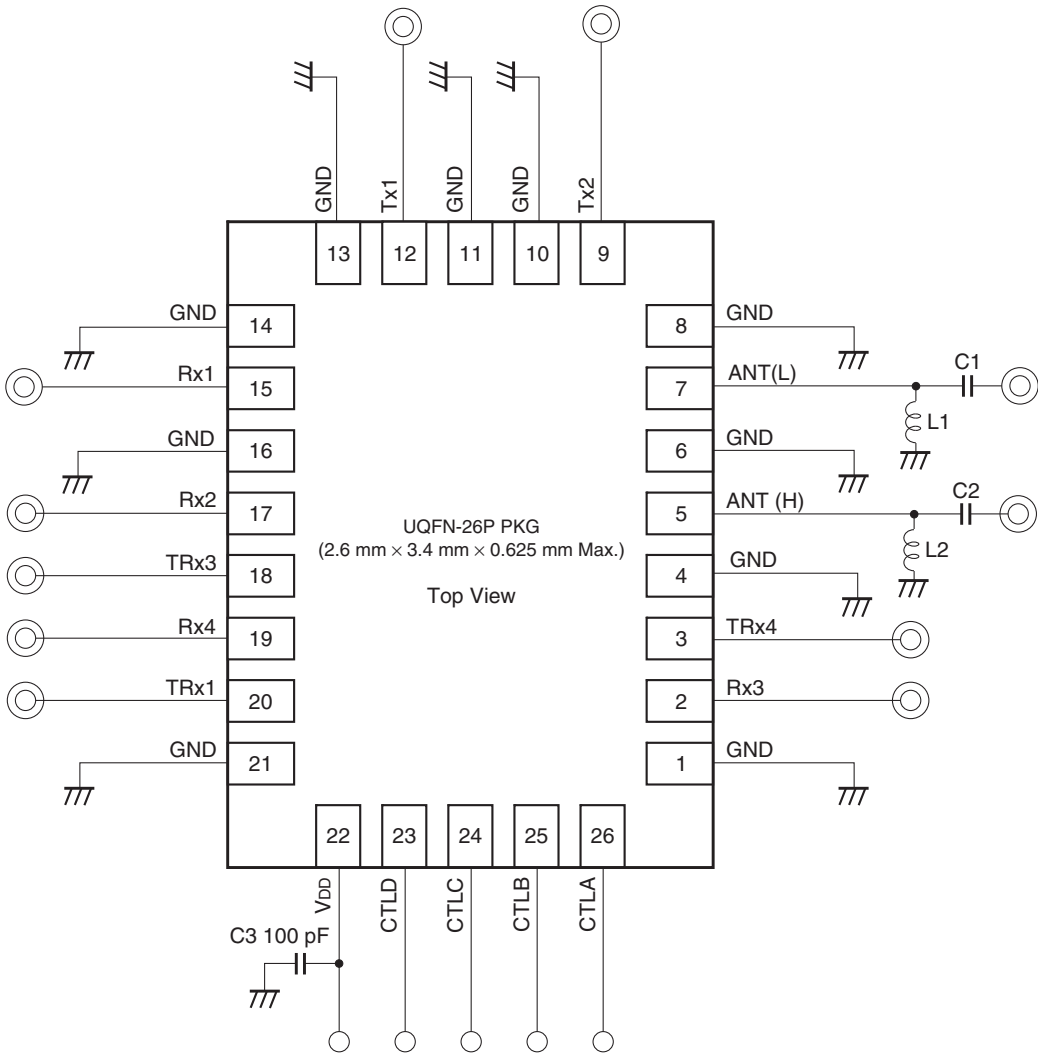
IIP2

(V_{DD} = 2.5 V, Ta = 25 ˚C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Input IP2	IIP2		Tx at TRx*1 24 dBm [MHz]	Jammer at Ant –20 dBm [MHz]	IM2 Product at TRx*1 [MHz]				dBm
		Ant-TRx1, 3, 4	836.61	1718.61	881.61	113.5	—	—	
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

*1 Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

Recommended Circuit



Note) 1. No DC blocking capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 (22 nH) and C1 (12 pF) are recommended on Ant port for ESD protection.
4. L2 (12 nH) and C2 (12 pF) are recommended on Ant port for ESD protection.
5. C3 capacitor (100 pF) is recommended.

Recommended Land Pattern

- PKG: 3.4 mm × 2.6 mm
- Pin pitch: 0.4 mm

Metal mask thickness: 110 µm

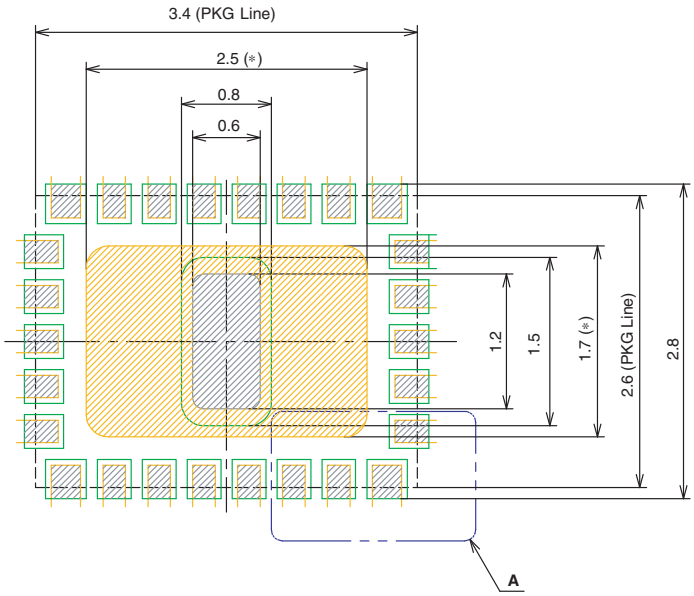
: Metal area in board (*1)

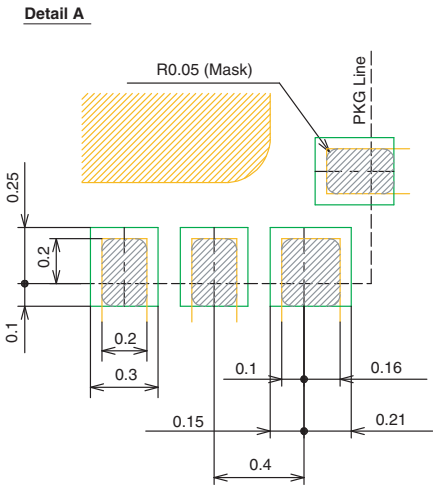
*1: GND plane is recommended

: Land

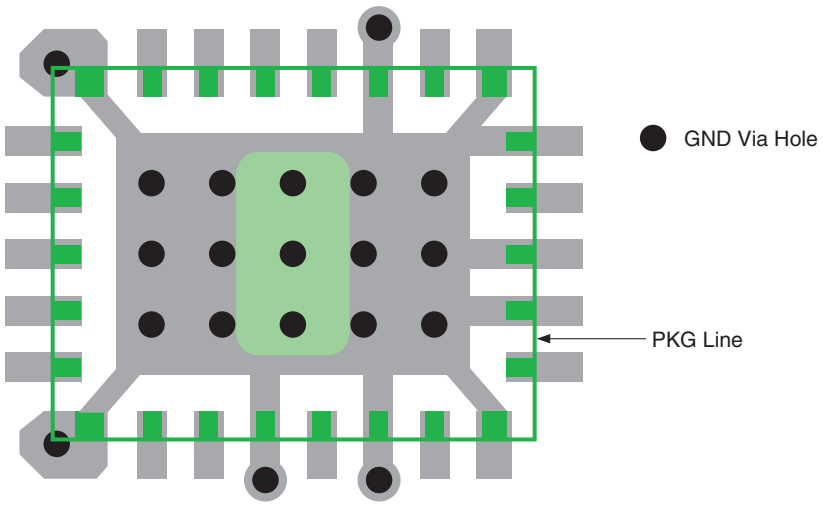
: Mask (Open area)

: Resist (Open area)





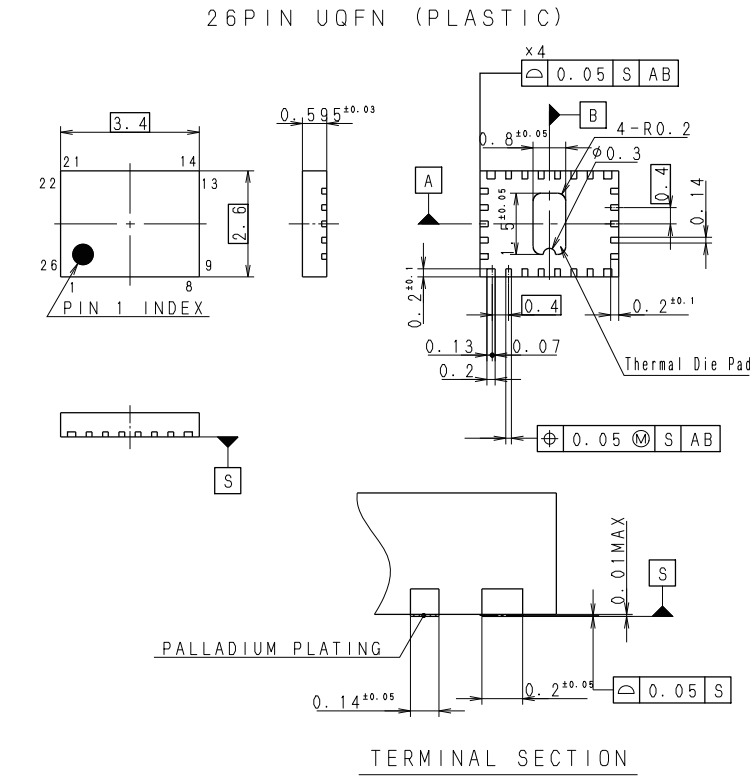
PCB GND Design for UQFN-26P (Image)



Package Outline

(Unit: mm)

Product Code: 875340541



Note:Terminal burr height 0.05mm MAX.

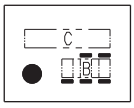
SONY CODE	UQFN-26P-541
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

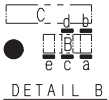
PART No. AP-2000-26QNBE3	Rev. 0
ISSUED '11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-26-CBE	

Marking



MARKING C: M3580

注1) B部はロット番号（Max3文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記2進法ビット方式により表示する。）
a部年コード（2進法ビット方式の1ビット目を表示）を配置する。
b部年コード（2進法ビット方式の2ビット目を表示）を配置する。
c部年コード（2進法ビット方式の3ビット目を表示）を配置する。
d部年コード（2進法ビット方式の4ビット目を表示）を配置する。
注2) C部は製品名（Max5文字）を配置する。
（5文字を超える場合は製品名省略標示規定に従う。）
注3) e部は組立場所表記を配置する。



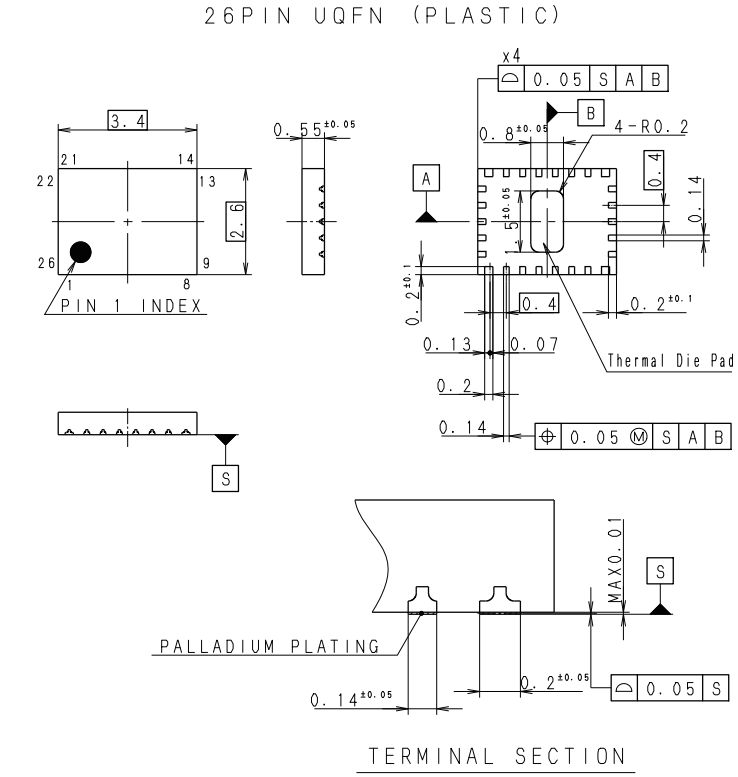
DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) ASSEMBLY PLACE IN SECTION e.

Packag Outline

(Unit: mm)

Product Code: 875338200



Note:Terminal burr height 0.05mm MAX.

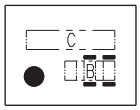
SONY CODE	UQFN-26P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

PART No. AP-4000-26011S	Rev. 0
ISSUED '11.06.20	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CORD:UR-26-1	

Marking



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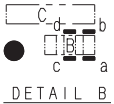
（5文字を超える場合は製品名省略標示規定に従う。）
注3) マーク深さは、MAX0.05mmの事.



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(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm