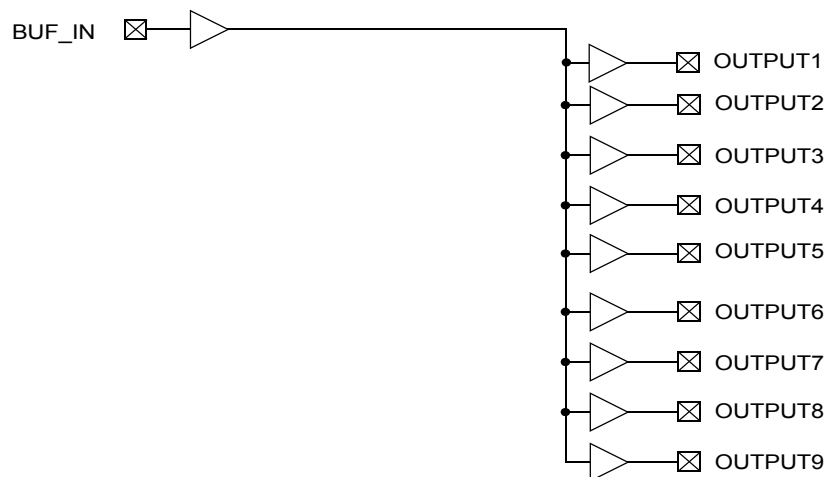


Features

- One-input to nine-output buffer/driver
- Supports two DIMMs or four SO-DIMMs with one additional output for feedback to an external or chipset phase-locked loop (PLL)
- Low power consumption for mobile applications
 - Less than 32 mA at 66.6 MHz with unloaded outputs
- 1-ns Input-output delay
- Buffers all frequencies from DC to 133.33 MHz
- Output-output skew less than 250 ps
- Multiple V_{DD} and V_{SS} pins for noise and electromagnetic interference (EMI) reduction
- Space-saving 16-pin 150-mil small-outline integrated circuit (SOIC) package
- 3.3 V operation
- Industrial temperature available

Logic Block Diagram



Functional Description

The CY2309NZ is a low-cost buffer designed to distribute high-speed clocks in mobile PC systems and desktop PC systems with SDRAM support. The part has nine outputs, eight of which can be used to drive two DIMMs or four SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133.33 MHz.

The CY2309NZ is designed for low EMI and power optimization. It has multiple V_{SS} and V_{DD} pins for noise optimization and consumes less than 32 mA at 66.6 MHz, making it ideal for the low-power requirements of mobile systems. It is available in an ultra-compact 150-mil 16-pin SOIC package.

Contents

Pinouts	3	Acronyms	8
Maximum Ratings	4	Document Conventions	8
Operating Conditions	4	Units of Measure	8
Electrical Characteristics	4	Document History Page	9
Switching Characteristics	4	Sales, Solutions, and Legal Information	10
Switching Waveforms	5	Worldwide Sales and Design Support	10
Ordering Information	6	Products	10
Ordering Code Definition	6	PSoC Solutions	10
Package Diagram	7		

Pinouts

Figure 1. CY2309NZ - 16 SOIC-Top View

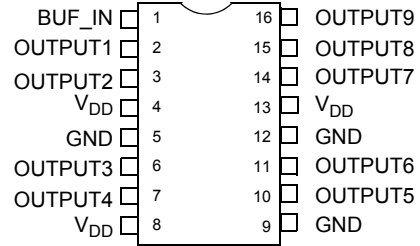


Table 1. Pin Description for CY2309NZ

Pin	Signal	Description
4, 8, 13	V _{DD}	3.3 V Digital voltage supply
5, 9, 12	GND	Ground
1	BUF_IN	Input clock
2, 3, 6, 7, 10, 11, 14, 15, 16	OUTPUT [1:9]	Outputs

Maximum Ratings

Supply voltage to ground potential	-0.5 V to +7.0 V	Storage temperature	-65 °C to +150 °C
DC input voltage	-0.5 V to 7.0 V	Junction temperature.....	150 °C
		Static discharge voltage (per MIL-STD-883, Method 3015)	>2,000 V

Operating Conditions for Commercial and Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V _{DD}	Supply voltage	3.0	3.6	V
T _A	(Ambient operating temperature) commercial	0	70	°C
	(Ambient operating temperature) industrial	-40	85	°C
C _L	Load capacitance, Fout < 100 MHz	-	30	pF
	Load capacitance, 100 MHz < Fout < 133.33 MHz	-	15	pF
C _{IN}	Input capacitance	-	7	pF
BUF_IN, OUTPUT [1:9]	Operating frequency	DC	133.33	MHz
t _{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for Commercial and Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V _{IL}	Input LOW voltage ^[1]		-	0.8	V
V _{IH}	Input HIGH voltage ^[1]		2.0	-	V
I _{IL}	Input LOW current	V _{IN} = 0 V	-	50.0	μA
I _{IH}	Input HIGH current	V _{IN} = V _{DD}	-	100.0	μA
V _{OL}	Output LOW voltage ^[2]	I _{OL} = 8 mA	-	0.4	V
V _{OH}	Output HIGH voltage ^[2]	I _{OH} = -8 mA	2.4	-	V
I _{DD}	Supply current	Unloaded outputs at 66.66 MHz	-	32	mA

Switching Characteristics for Commercial and Industrial Temperature Devices^[3]

Parameter	Name	Description	Min	Typ	Max	Unit
	Duty cycle ^[2] = t ₂ ÷ t ₁	Measured at 1.4 V	40.0	50.0	60.0	%
t ₃	Rise time ^[2]	Measured between 0.8 V and 2.0 V	-	-	1.50	ns
t ₄	Fall time ^[2]	Measured between 0.8 V and 2.0 V	-	-	1.50	ns
t ₅	Output to output skew ^[2]	All outputs equally loaded	-	-	250	ps
t ₆	Propagation delay, BUF_IN Rising edge to Output Rising edge ^[2]	Measured at V _{DD} /2	1	5	9.2	ns

Notes

1. BUF_IN input has a threshold voltage of V_{DD}/2.
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.
3. All parameters specified with loaded outputs.

Switching Waveforms

Figure 2. Duty Cycle Timing

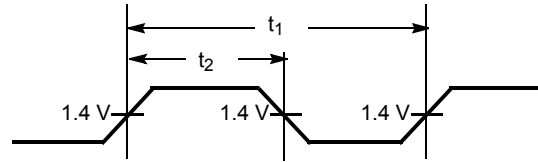


Figure 3. All Outputs Rise/Fall Time

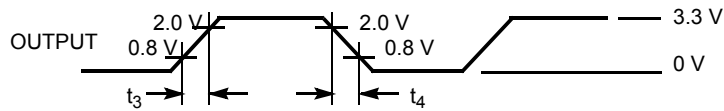


Figure 4. Output-Output Skew

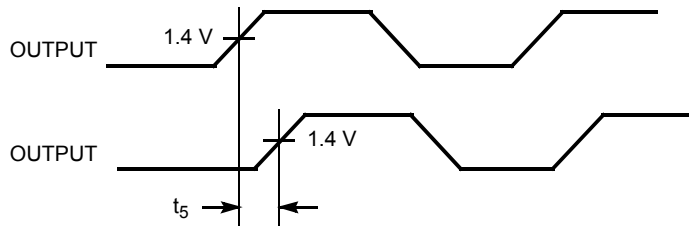
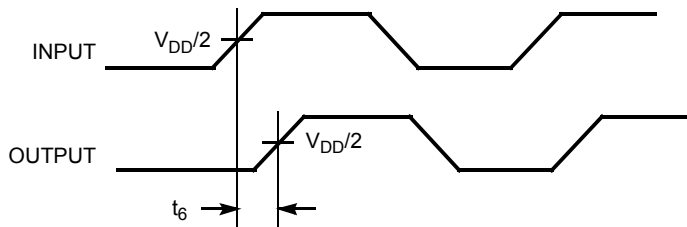
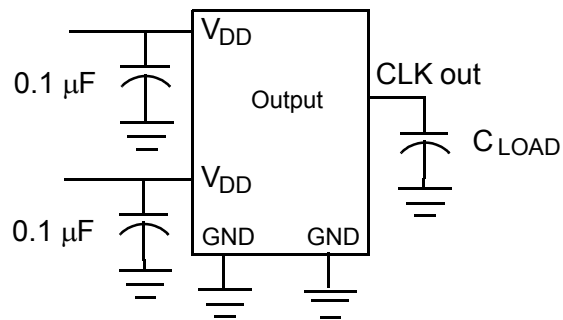


Figure 5. Input-Output Propagation Delay



Test Circuits



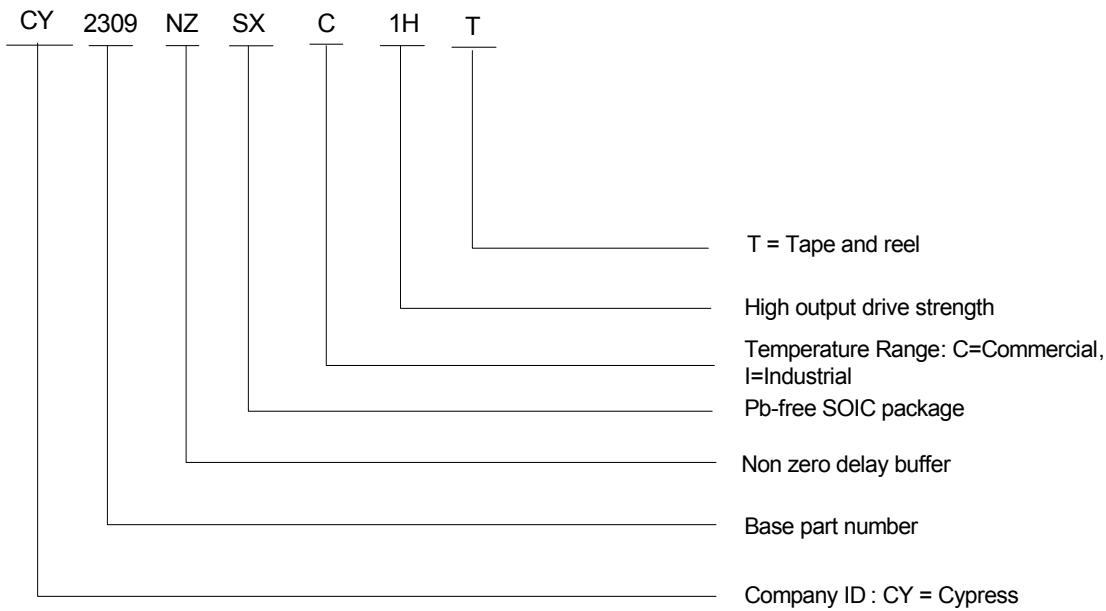
Note

4. Not recommended for new designs.

Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2309NZSXC-1H	16-pin 150-mil SOIC	Commercial
CY2309NZSXC-1HT	16-pin 150-mil SOIC – Tape and reel	Commercial
CY2309NZSXI-1H	16-pin 150-mil SOIC	Industrial
CY2309NZSXI-1HT	16-pin 150-mil SOIC – Tape and reel	Industrial

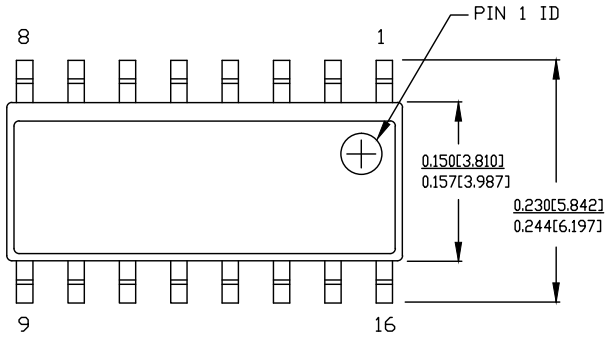
Ordering Code Definition



Package Diagram

Figure 6. 16-Pin (150-Mil) SOIC S16

16 Lead (150 Mil) SOIC

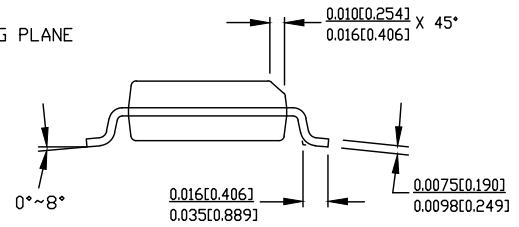
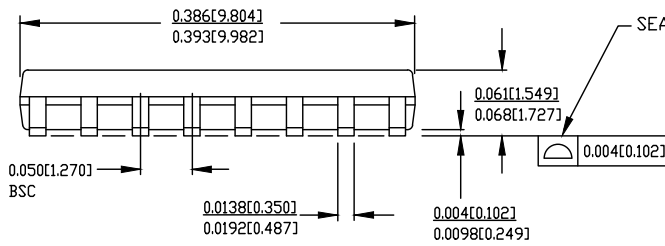


DIMENSIONS IN INCHES[MM] MIN. MAX.

REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.



51-85068 °C

Acronyms

Acronym	Description
PLL	phase-locked loop
SOIC	small-outline integrated circuit
EMI	Electromagnetic interference

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
mA	milliampere
μA	microamperes
MHz	megahertz
ms	milliseconds
mV	millivolts
ns	nanoseconds
pF	picofarads
V	volts

Document History Page

Document Title: CY2309NZ Nine-Output 3.3 V Buffer Document Number: 38-07182				
REV.	ECN	Orig. of Change	Submission Date	Description of Change
**	111858	DSG	12/09/01	Change from Spec number: 38-00709 to 38-07182
*A	121834	RBI	12/14/02	Power-up requirements added to Operating Conditions Information
*B	130563	SDR	10/23/03	Added industrial operating temperature to operating conditions
*C	212991	RGL/GGK	03/30/04	Updated the propagation delay T ₆ spec to 9.2 ns in the Switching Characteristics table
*D	270149	RGL	10/04/04	Added Lead-free devices Replaced 8.7ns Input/Output Delay to 1ns Input/Output Delaying the features section
*E	2568533	AESA	09/23/08	Updated template. Added Note "Not recommended for new designs." Changed "SDRAM [1:9]" to "OUTPUT [1:9]" in Operating Conditions table. Removed part number CY2309NZSI-1H and CY2309NZSI-1HT.
*F	2904715	CXQ	04/05/10	Removed parts CY2309NZSC-1H,CY2309NZSC-1HT from Ordering Information. Updated Package Diagram
*G	3082147	CXQ	11/10/2010	Maximum Rating section on page 2, change the following from: "DC Input Voltage (Except REF) -0.5 V to VDD + 0.5 V" "DC Input Voltage REF-0.5 V to 7.0 V" to: "DC Input Voltage-0.5 V to 7.0 V" Updated datasheet as per new template Updated footnotes Added Acronyms and Units of Measure table Added Ordering Code Definition

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2008-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.