CY28354

200-MHz 24-Output Buffer for 4 DDR DIMMS

Features

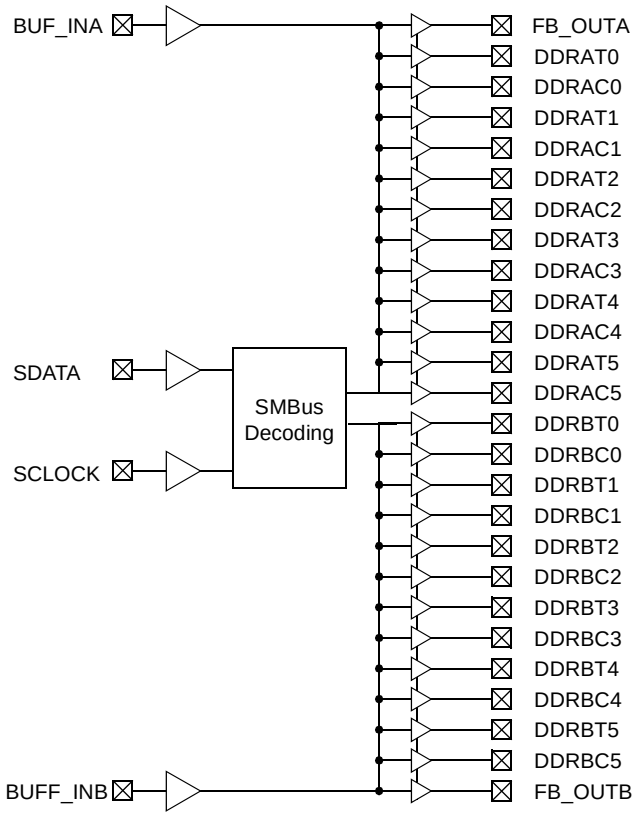
- **Dual 1- to 12-output buffer/driver**
- **Supports up to 4 DDR DIMMs**
- **Outputs are individually enabled/disabled**
- **Low-skew outputs (< 100 ps)**
- **Supports 266-MHz, 333-MHz and 400-MHz DDR SDRAM**
- **SMBus Read and Write support**
- **Space-saving 48-pin SSOP package**

Functional Description

The CY28354 is a 2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 24 outputs. Designers can configure these outputs to support four unbuffered DDR DIMMS or to support 3 unbuffered standard SDRAM DIMMs and 2 DDR DIMMS. The CY28354 can be used in conjunction with the W250 or similar clock synthesizer for the VIA Pro 266 chipset.

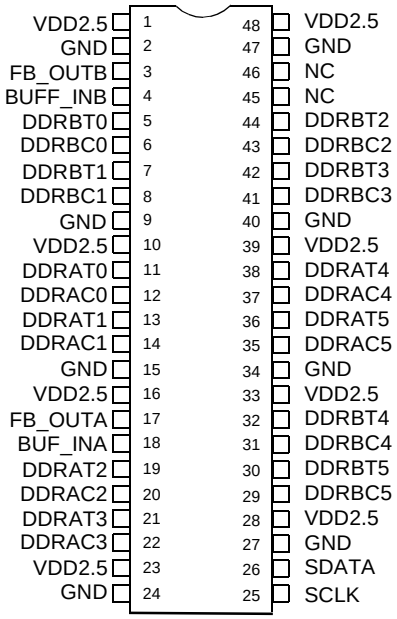
The CY28354 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled.

Block Diagram



Pin Configuration

SSOP
Top View



Pin Description

Pin	Name	PWR	I/O	Description
11, 13, 19, 21, 38, 36, 5, 7, 44, 42, 32, 30	DDRA[0:5]T DDRB[0:5]T	VDD2.5	O	**Clock outputs**. These outputs provide copies of BUF_INA & BUF_INB, respectively.
12, 14, 20, 22, 37, 35, 6, 8, 43, 41, 31, 29	DDRA[0:5]C DDRB[0:5]C	VDD2.5	O	**Clock outputs**. These outputs provide complementary copies of BUF_INA & BUF_INB, respectively.
18, 4	BUF_INA, BUF_INB	VDD2.5	I	**Reference input from chipset**. 2.5V input.
17, 3	FB_OUTA FB_OUTB	VDD2.5	O	**Feedback clock for chipset**
46, 45	NC			**Not Connected**
25	SCLK	VDD2.5	I	**SMBus clock input**
26	SDATA	VDD2.5	I/O	**SMBus data input**
1, 10, 16, 23, 28, 33, 39, 48	VDD2.5			**2.5V voltage supply**
2, 9, 15, 24, 27, 34, 40, 47	GND			**Ground**

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*. The block write and block read protocol is outlined in *Table 2*.The slave receiver address is D2 depending on the state of the ADDRSEL pin.

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ’0000000’

Table 2. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 from master – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte 1 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0”.
- SMBus Address for the CY28354 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7		Input Threshold Control 00: Normal (1.25V) 01: 1.20V 10: 1.15V 11: 1.35V	0
Bit 6			0
Bit 5	17	FBOUTA Control, 0 = Enable, 1 = Disable	0
Bit 4	3	FBOUTB Control, 0 = Enable, 1 = Disable	0
Bit 3	30, 29	DDRBT5, DDRBC5	1
Bit 2	32, 31	DDRBT4, DDRBC4	1
Bit 1	42, 41	DDRBT3, DDRBC3	1
Bit 0	44, 43	DDRBT2, DDRBC2	1

Byte 1: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	7, 8	DDRBT1, DDRBC1	1
Bit 6	5, 6	DDRBT0, DDRBC0	1
Bit 5	36, 35	DDRAT5, DDRAC5	1
Bit 4	38, 37	DDRAT4, DDRAC4	1
Bit 3	21, 22	DDRAT3, DDRAC3	1
Bit 2	19, 20	DDRAT2, DDRAC2	1
Bit 1	13, 14	DDRAT1, DDRAC1	1
Bit 0	11, 12	DDRAT0, DDRAC0	1

Absolute Maximum Ratings[1]

Supply Voltage to Ground Potential .....–0.5 to +7.0V

DC Input Voltage (except BUF_IN) ..... –0.5V to V_{DD}+0.5

Storage Temperature .....–65°C to +150°C

Static Discharge Voltage .....>2000V (per MIL-STD-883, Method 3015)

This device contains circuitry designed to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

Table 3. Absolute Maximum Ratings

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage to Ground Potential	–0.5		7.0	V
V_{in}	DC Input Voltage (except BUFF_IN)	–0.5		V_{DD}+0.5	V
V_{out}	Output Voltage				
T_s	Temperature, Storage	–65		+150	°C
T_a	Temperature, Operating Ambient	0		70	°C
ESD_h	ESD Protection (Human Body Model)			2000	V

Table 4. DC Parameter

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD2.5}$	Supply Voltage	2.375		2.625	V
T_A	Operating Temperature (Ambient Temperature)	0		70	°C
C_{OUT}	Output Capacitance		6		pF
C_{IN}	Input Capacitance		5		pF

Table 5. Electrical Characteristics Over the Operating Range

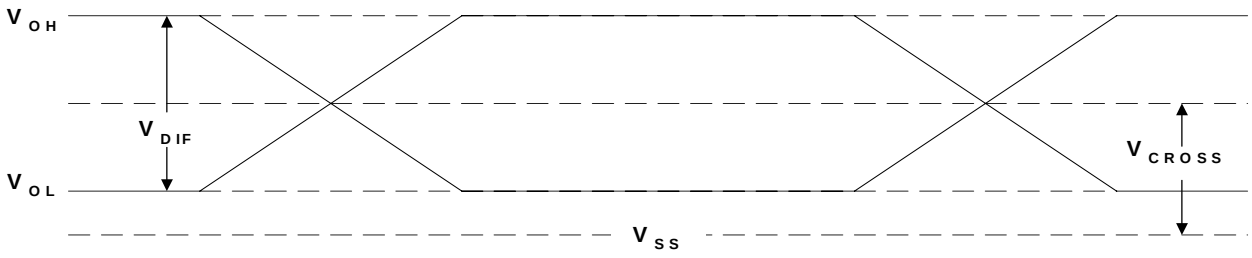
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	For all pins except SMBus			0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$			50	µA
I_{OH}	Output HIGH Current	V_{DD} = 2.375V, V_{OUT} = 1V	–18	–32		mA
I_{OL}	Output LOW Current	V_{DD} = 2.375V, V_{OUT} = 1.2V	26	35		mA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 12 mA, V_{DD} = 2.375V			0.6	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –12 mA, V_{DD} = 2.375V	1.7			V
I_{DD}	Supply Current[2]	Unloaded outputs, 133 MHz			400	mA
I_{DD}	Supply Current	Loaded outputs, 133 MHz			500	mA
V_{OUT}	Output Voltage Swing	See Test Circuity. See *Figure 1*	0.7		V_{DD} + 0.6	V
V_{OC}	Output Crossing Voltage		1.0	1.25	1.5	V
IN_{DC}	Input Clock Duty Cycle		48		52	%

Note:
1. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

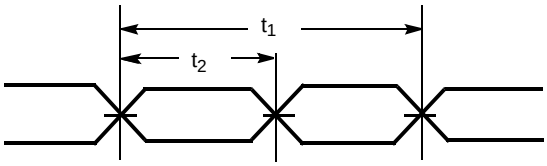
Table 6. Switching Characteristics[3]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
--	Operating Frequency		66		200	MHz
--	Duty Cycle[2, 4] = $t_2 \div t_1$	Measured differentially at V_{CROSS}	IN_{DC} –5%		IN_{DC} +5%	%
t_{3d}	DDR Rising Edge Rate[2]	Measured single ended at 20% to 80% of V_{DIF}	1.0	1.5	2.0	V/ns
t_{4d}	DDR Falling Edge Rate[2]	Measured single ended at 80% to 20% of V_{DIF}	1.0	1.5	2.0	V/ns
t_5	Output to Output Skew for DDR[2]	All outputs equally loaded. See *Figure 1*.			100	ps

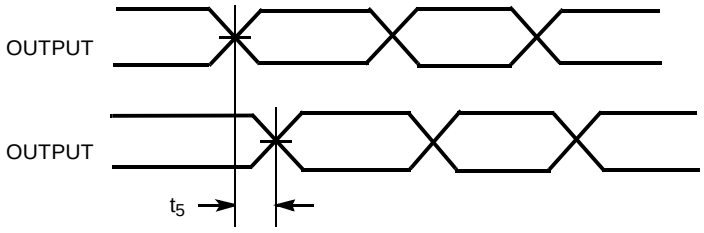
Switching Waveforms



Duty Cycle Timing



Output-Output Skew



Notes:
3. All parameters specified with loaded outputs.
4. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

Figure 1 shows the differential clock directly terminated by a 120Ω resistor.

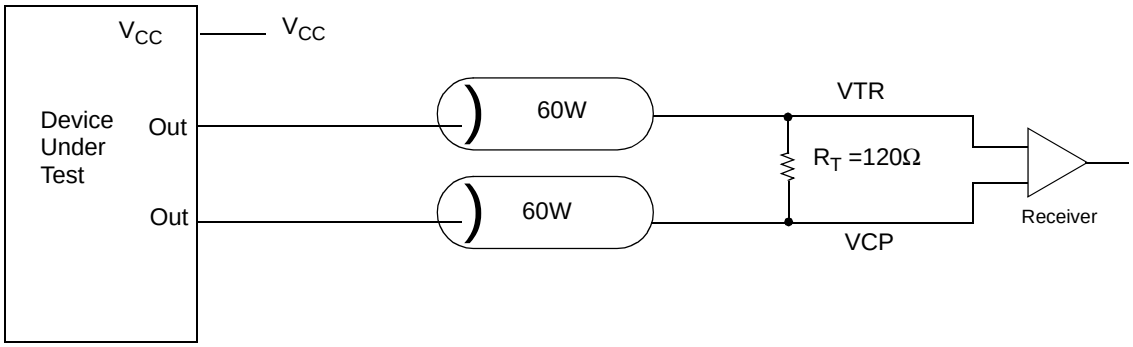
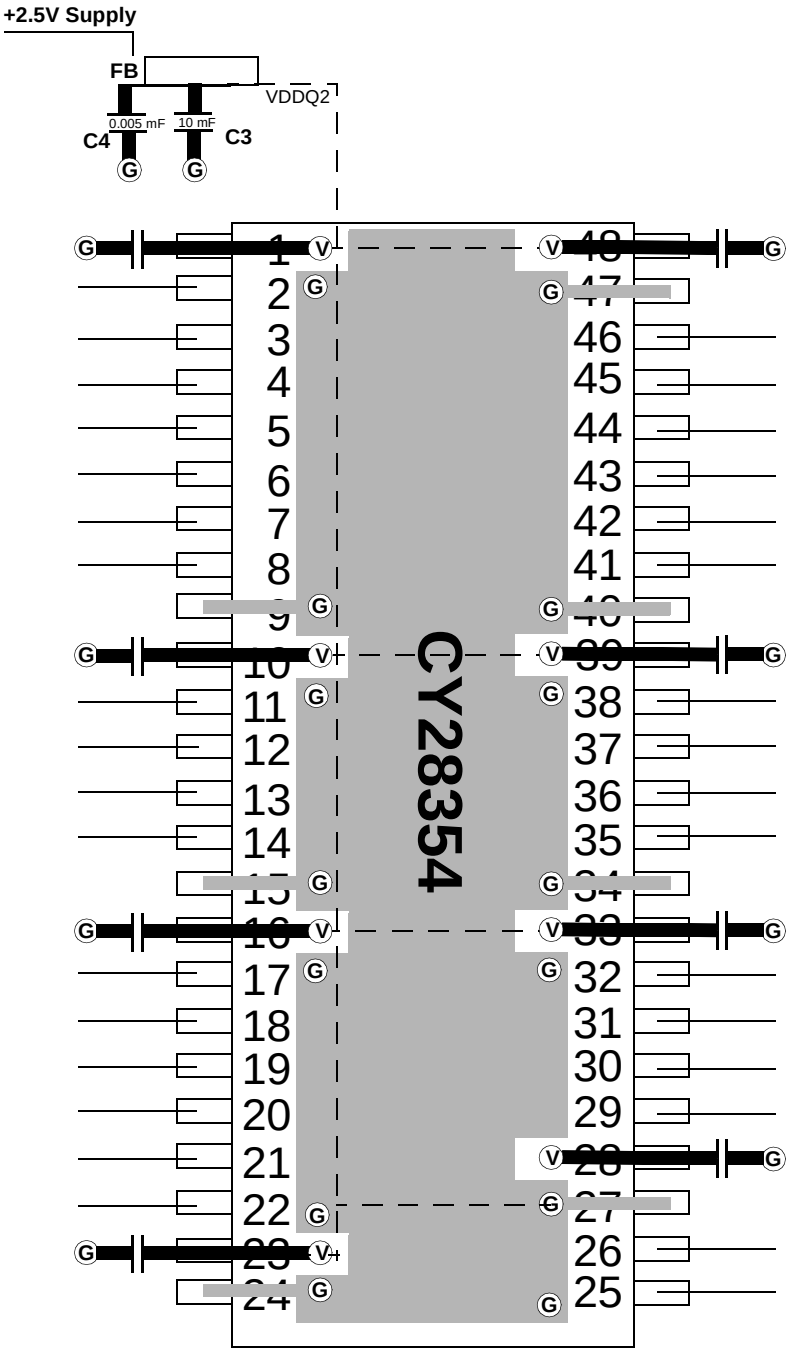


Figure 1. Differential Signal Using Direct Termination Resistor

Layout Example for DDR 2.5V



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120
Ceramic Caps C3 = 10–22 µF C4 = 0.005 µF

Ⓖ = VIA to GND plane layer Ⓥ =VIA to respective supply plane layer

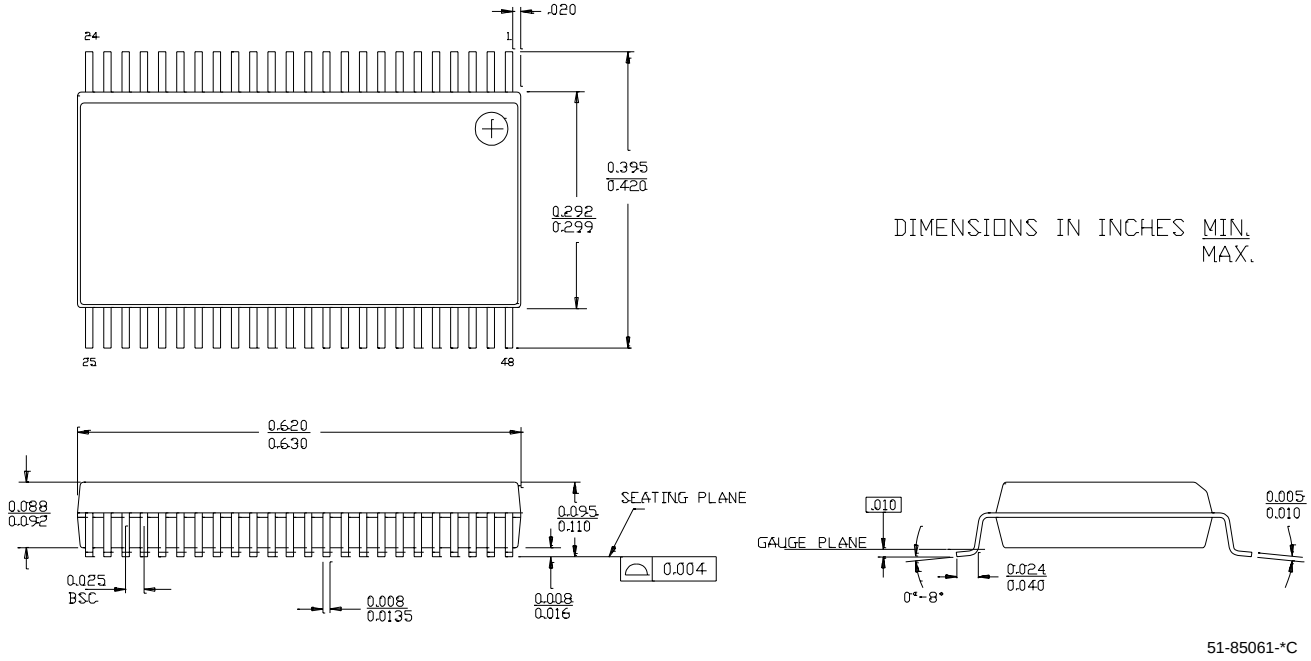
Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = 0.1 µF ceramic

Ordering Information

Ordering Code	Package Type	Operating Range
CY28354OC	48-pin SSOP	Commercial, 0°C to 70 °C
CY28354OCT	48-pin SSOP (Tape & Reel)	Commercial, 0°C to 70 °C

Package Diagram

48-Lead Shrunk Small Outline Package O48



All product and company names mentioned in this document may be the trademarks of their respective holders.

Document Title: CY28354 200-MHz 24-Output Buffer for 4 DDR DIMMS Document Number: 38-07423				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115054	08/29/02	INA	New Data Sheet
*A	122926	12/19/02	RBI	Add power up requirements to maximum ratings information.