

1:10 Differential LVDS Fanout Buffer with Selectable Clock Input

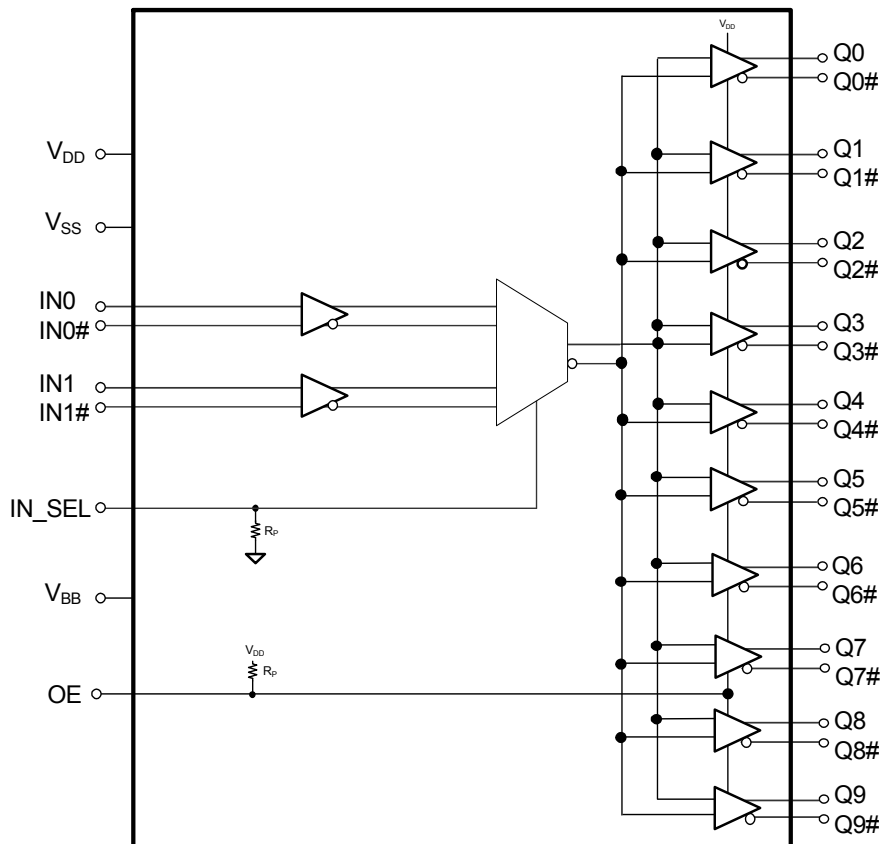
Features

- Select one of two low-voltage differential signal (LVDS) input pairs to distribute to 10 LVDS output pairs
- 40-ps maximum output-to-output skew
- 600-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- Asynchronous output enable function
- 32-pin thin quad flat pack (TQFP) package
- 2.5-V or 3.3-V operating voltage ^[1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DL15110 is an ultra-low noise, low skew, low propagation delay 1:10 LVDS fanout buffer targeted to meet the requirements of high speed clock distribution applications. The CY2DL15110 can select between two separate LVDS input clock pairs using the IN_SEL pin. The output enable function allows the outputs to be asynchronously driven to a high-impedance state. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

Logic Block Diagram



Note

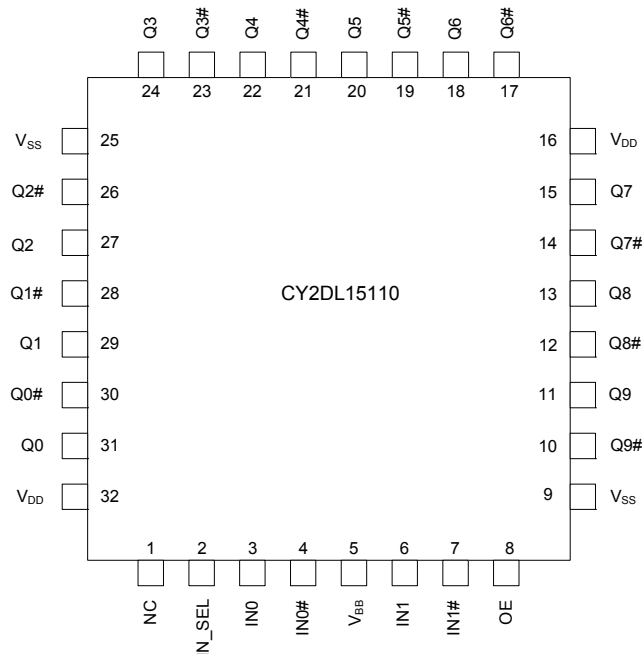
1. Input AC-coupling capacitors are required for voltage-translation applications.

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Pinouts

Figure 1. Pin Diagram - CY2DL15110



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1	NC		No connection
2	IN_SEL	Input	Input clock select pin. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTTL). When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
3	IN0	Input	LVDS input clock. Active when IN_SEL = Low
4	IN0#	Input	LVDS complementary input clock. Active when IN_SEL = Low
5	V _{BB}	Output	LVDS reference voltage output
6	IN1	Input	LVDS input clock. Active when IN_SEL = High
7	IN1#	Input	LVDS complementary input clock. Active when IN_SEL = High
8	OE	Input	Output enable. LVCMOS/LVTTTL; When OE = Low, Q(0:9) and Q(0:9)# outputs are disabled
9, 25	V _{SS}	Power	Ground
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	Q(0:9)#	Output	LVDS complementary output clocks
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q(0:9)	Output	LVDS output clocks
16, 32	V _{DD}	Power	Power supply

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	-0.5	4.6	V
$V_{IN}^{[2]}$	Input voltage, relative to V_{SS}	Nonfunctional	-0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
$V_{OUT}^{[2]}$	DC output or I/O Voltage, relative to V_{SS}	Nonfunctional	-0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
T_S	Storage temperature	Nonfunctional	-55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	-	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL-94	Flammability rating	At 1/8 in.	V-0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	-40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum supply voltage (power ramp must be monotonic.)	0.05	500	ms
$t_{STARTUP}$	Start up time	Time taken from V_{DD} reaching 95% of its minimum supply voltage to the device being operational.	1	-	ms

Note

2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

DC Electrical Specifications

($V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ (Commercial) or $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVDS outputs terminated with $100\ \Omega$ load [3, 4]	–	125	mA
V_{IH1}	Input high Voltage, LVDS input clocks, IN0, IN0#, IN1, and IN1#		–	$V_{DD} + 0.3$	V
V_{IL1}	Input low voltage, LVDS input clocks, IN0, IN0#, IN1, and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, IN_SEL and OE	$V_{DD} = 3.3\text{ V}$	2.0	$V_{DD} + 0.3$	V
V_{IL2}	Input low voltage, IN_SEL and OE	$V_{DD} = 3.3\text{ V}$	–0.3	0.8	V
V_{IH3}	Input high voltage, IN_SEL and OE	$V_{DD} = 2.5\text{ V}$	1.7	$V_{DD} + 0.3$	V
V_{IL3}	Input low voltage, IN_SEL and OE	$V_{DD} = 2.5\text{ V}$	–0.3	0.7	V
V_{ID} ^[5]	Input differential amplitude	See Figure 3 on page 7	0.4	0.8	V
V_{ICM}	Input common mode voltage	See Figure 3 on page 7	0.5	$V_{DD} - 0.2$	V
I_{IH}	Input high current, All inputs	Input = V_{DD} ^[6]	–	150	μA
I_{IL}	Input low current, All inputs	Input = V_{SS} ^[6]	–150	–	μA
V_{PP}	LVDS differential output voltage peak to peak, single-ended	$V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between Q and Q# pairs [3, 7]	250	470	mV
ΔV_{OCM}	Change in V_{OCM} between complementary output states	$V_{DD} = 3.3\text{ V}$ or 2.5 V , $R_{TERM} = 100\ \Omega$ between Q and Q# pairs [3, 7]	–	50	mV
V_{BB}	Output reference voltage	0 to $150\ \mu\text{A}$ output current	1.125	1.375	V
I_{OZ}	Output leakage current	OE = V_{SS} , $V_{OUT} = 0.75\text{ V}$ to 1.75 V	–15	15	μA
R_P	Internal pull-up / pull-down resistance, LVCMOS logic input	IN_SEL pin has pull-down only OE pin has pull-up only	60	140	$\text{k}\Omega$
C_{IN}	Input capacitance	Measured at 10 MHz per pin	–	3	pF

Notes

3. Refer to [Figure 2 on page 7](#).
4. I_{DD} includes current that is dissipated externally in the output termination resistors.
5. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
6. Positive current flows into the input pin, negative current flows out of the input pin.
7. Refer to [Figure 4 on page 7](#).

AC Electrical Specifications

($V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ (Commercial) or $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
$t_{PD}^{[8]}$	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	600	ps
$t_{ODC}^{[9]}$	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
$t_{SK1}^{[10]}$	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
$t_{SK1D}^{[10]}$	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25-MHz input Rise/fall time < 150 ps (20% to 80%) $V_{ID} > 400\text{ mV}$	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–135	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
$t_{JIT}^{[11]}$	Additive RMS phase jitter (Random)	Offset = 20 MHz	–	–	–155	dBc/Hz
		156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400\text{ mV}$	–	–	0.11	ps
$t_R, t_F^{[12]}$	Output rise/fall time, single-ended	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz	–	–	300	ps

Notes

8. Refer to [Figure 5 on page 7](#).
9. Refer to [Figure 6 on page 7](#).
10. Refer to [Figure 7 on page 8](#).
11. Refer to [Figure 8 on page 8](#).
12. Refer to [Figure 9 on page 8](#).

Figure 2. LVDS Output Termination

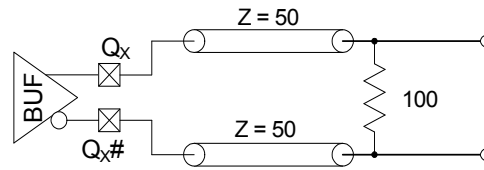


Figure 3. Input Differential and Common Mode Voltages

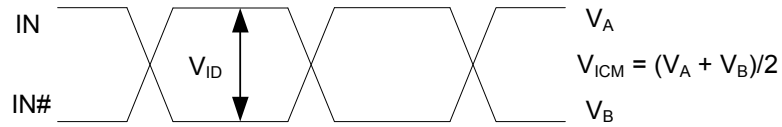


Figure 4. Output Differential and Common Mode Voltages

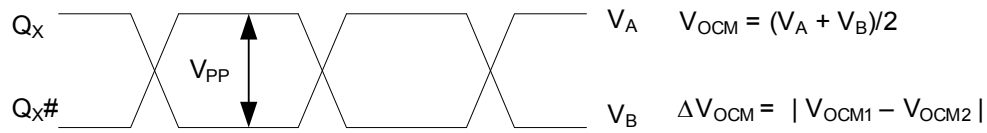


Figure 5. Input to Any Output Pair Propagation Delay

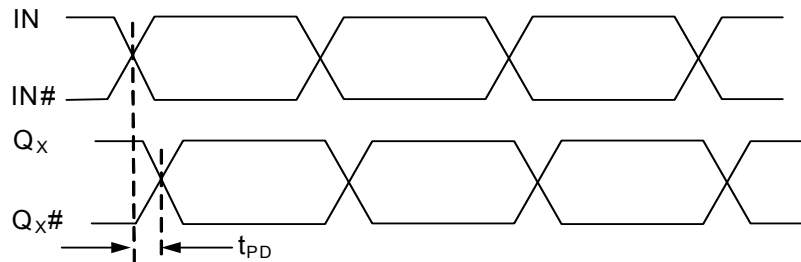


Figure 6. Output Duty Cycle

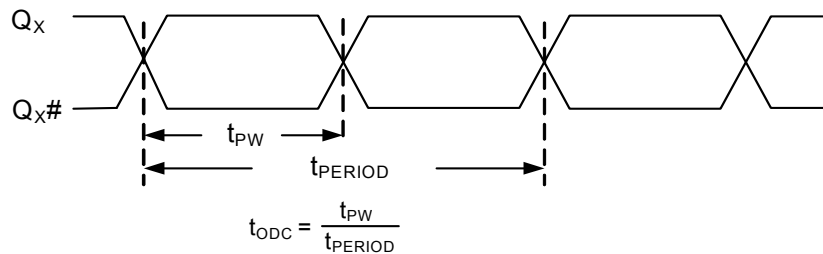


Figure 7. Output-to-output and Device-to-device Skew

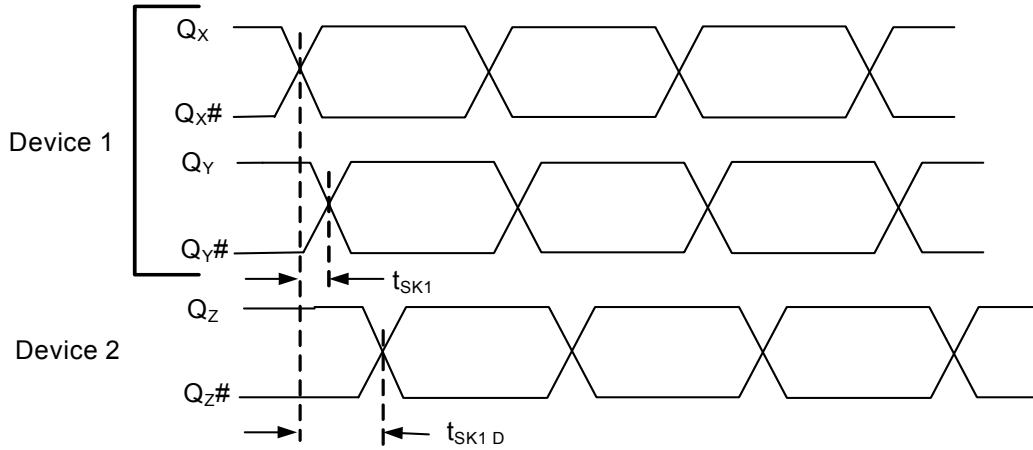


Figure 8. RMS Phase Jitter

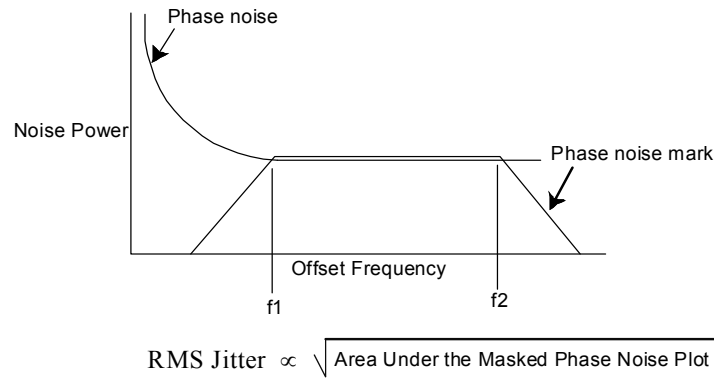
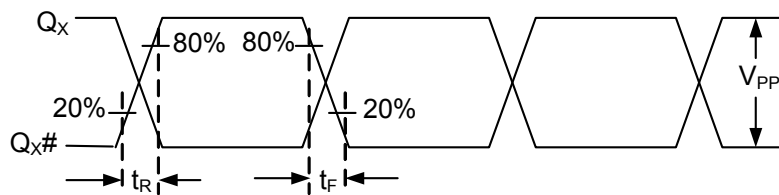


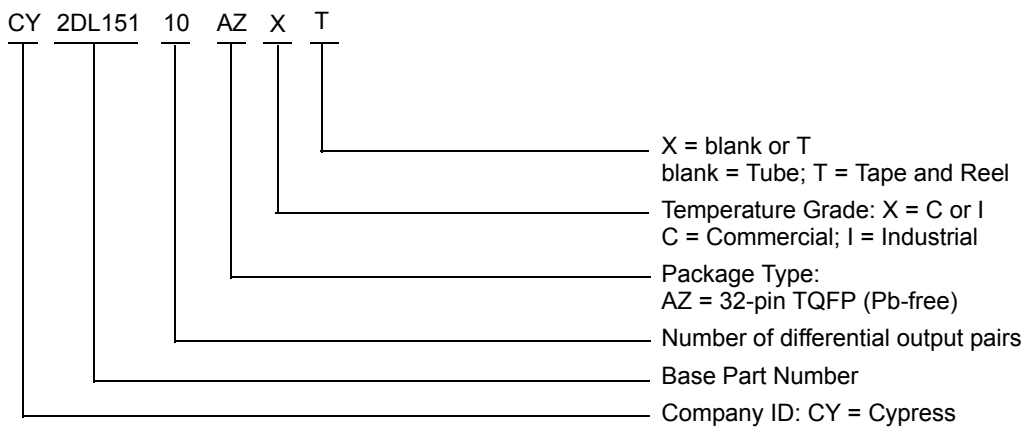
Figure 9. Output Rise/Fall Time



Ordering Information

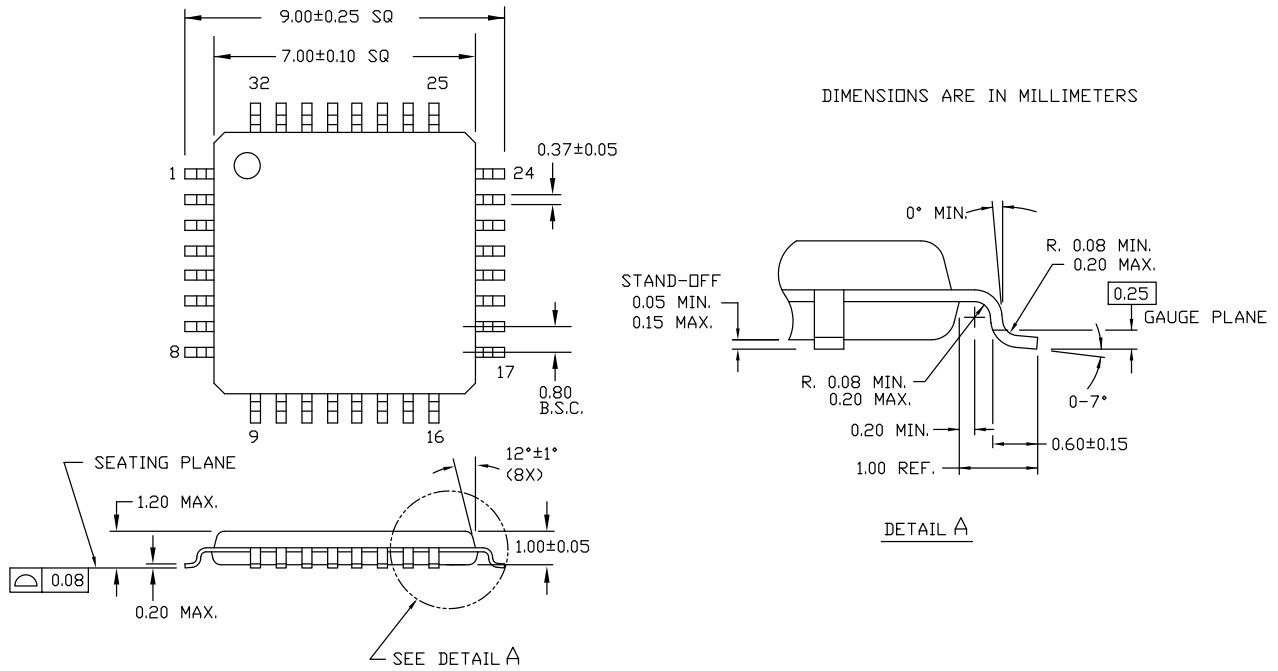
Part Number	Type	Production Flow
Pb-free		
CY2DL15110AZC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY2DL15110AZCT	32-pin TQFP tape and reel	Commercial, 0 °C to 70 °C
CY2DL15110AZI	32-pin TQFP	Industrial, -40 °C to 85 °C
CY2DL15110AZIT	32-pin TQFP tape and reel	Industrial, -40 °C to 85 °C

Ordering Code Definitions



Package Dimension

Figure 10. 32-pin TQFP (7 × 7 × 1.0 mm) A3210 Package Outline, 51-85063



51-85063 *D

Acronyms

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
I/O	input/output
JEDEC	joint electron devices engineering council
LVDS	low-voltage differential signal
LVC MOS	low-voltage complementary metal oxide semiconductor
LV TTL	low-voltage transistor-transistor logic
OE	output enable
RMS	root mean square
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
I/O	input/output
kHz	kilohertz
kΩ	kilohm
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DL15110, 1:10 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-69398				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3269680	CXQ	06/02/2011	New Datasheet.
*A	3292902	CXQ	06/27/2011	Minor edits in Logic Block Diagram (changed the OE resistor value from 100k to R _P). Minor edits in Figure 2 and Figure 4 (Replaced "Q" and "Q#" with "Q _X " and "Q _X #"). Deleted the Notes "Refer to Figure 2. " and "Refer to Figure 4. " in page 7 and their references in Figure 2 and Figure 4 .
*B	3357978	BASH	09/07/2011	Updated Operating Conditions (Added a parameter t _{STARTUP} and its details). Updated Package Dimension .
*C	3548521	BASH	03/12/2012	Changed status from Advance to Final. Post to external web.

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