Pin Summary

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1, 2]

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↴	L	L
H	L	↴	H	H
H	L	H	X	B[3]
H	L	L	X	B[4]

Maximum Ratings[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[8]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND.			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[9]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance, ↴ = HIGH-to-LOW Transition.
2. A-to-B data flow is shown, B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description		CY74FCT16500AT/ CY74FCT162500AT		CY74FCT16500CT/ CY74FCT162500CT		Unit	Fig. No.[15]
			Min.[14]	Max.	Min.[14]	Max.		
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency			150		150	MHz	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLKBA}$ to A, $\overline{CLKAB}$ to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	6.0	1.5	5.4	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	5.6	1.5	5.2	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		3.0		3.0		ns	9
t_H	Hold Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		0		0		ns	9
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0		ns	4
		Clock LOW	1.5		1.5		ns	4
t_H	Hold Time, HIGH or LOW A to LEAB, B to LEBA		1.5		1.5		ns	4
t_W	LEAB or LEBA Pulse Width HIGH		3.0		2.5		ns	5
t_W	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW		3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew[16]			0.5		0.5	ns	

Ordering Information CY74FCT16500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16500ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT162500ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	

Notes:
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.
16. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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