CY7C1041D

4-Mbit (256 K × 16) Static RAM

Features

- Pin-and function-compatible with CY7C1041B
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 90 mA at 10 ns (Industrial)
- Low CMOS standby power
  - I_{SB2} = 10 mA
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 44-Pin (400-Mil) Molded SOJ and 44-Pin TSOP II packages

Functional Description[1]

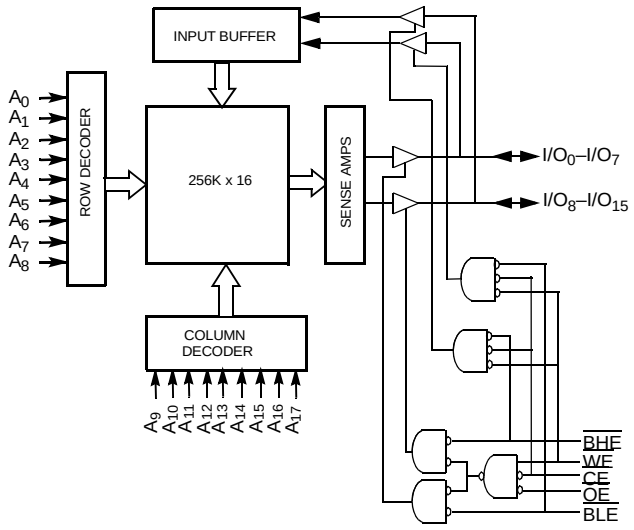
The CY7C1041D is a high-performance CMOS static RAM organized as 256K words by 16 bits. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1041D is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Selection Guide

	–10 (Industrial)	–12 (Automotive)[2]	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	90	95	mA
Maximum CMOS Standby Current	10	15	mA

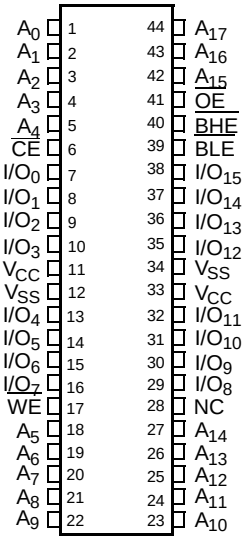
Note

1. For guidelines on SRAM system design, please refer to the “System Design Guidelines” Cypress application note, available on the internet at www.cypress.com.

Contents

Pin Configuration

Figure 1. SOJ / TSOP II – Top View



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] ...–0.5 V to +6.0 V

DC Voltage Applied to Outputs in High Z State[3] ..... –0.5 V to V_{CC} +0.5 V

DC Input Voltage[3] ..... –0.5 V to V_{CC} +0.5 V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... .....>2001 V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40°C to +85°C	5 V ± 0.5	10 ns
Automotive	–40°C to +125°C	5 V ± 0.5	12 ns

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial)		-12 (Automotive)		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA V_{CC} = Min, I_{OL} = 8.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage				0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[3]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	100 MHz		90		-	mA
			83 MHz		80		95	mA
			66 MHz		70		85	mA
			40 MHz		60		75	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			20		25	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0			10		15	mA

Capacitance[4]

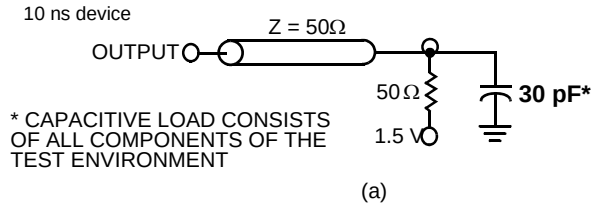
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[4]

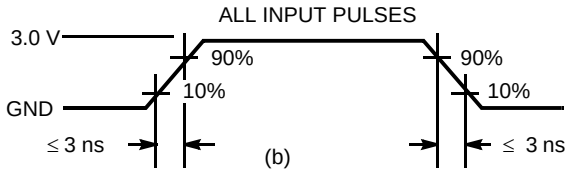
Parameter	Description	Test Conditions	SOJ Package	TSOP II Package	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)[4]	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.91	50.66	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)[4]		36.73	17.17	°C/W

Notes
2. Automotive product information is Preliminary.
3. V_{IL} (Min) = –2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[5]

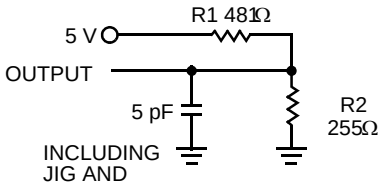


(a)



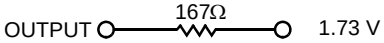
(b)

High-Z Characteristics:



(c)

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics[6] Over the Operating Range

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}	V_{CC}(typical) to the First Access[7]	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		6	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		5		6	ns

Notes

5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.

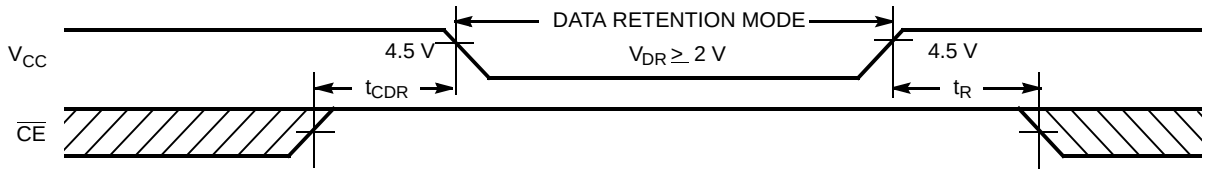
Switching Characteristics[6] Over the Operating Range(continued)

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min	Max	Min	Max	
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		10		ns
t_{AW}	Address Set-Up to Write End	7		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		10		ns
t_{SD}	Data Set-Up to Write End	6		7		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		10		ns

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[13]		Min	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	Ind'l		10	mA
I_{CCDR}	Data Retention Current		Auto		15	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[12]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Notes
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(Min)} \geq 50$ µs or stable at $V_{CC(Min)} \geq 50$ µs
13. No input may exceed V_{CC} + 0.5 V
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BHE}$ = V_{IL}.

Switching Waveforms

Figure 2. Read Cycle No. 1[13, 14]

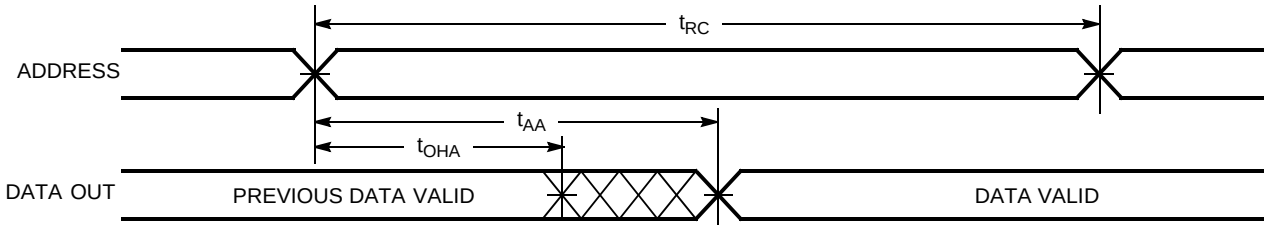
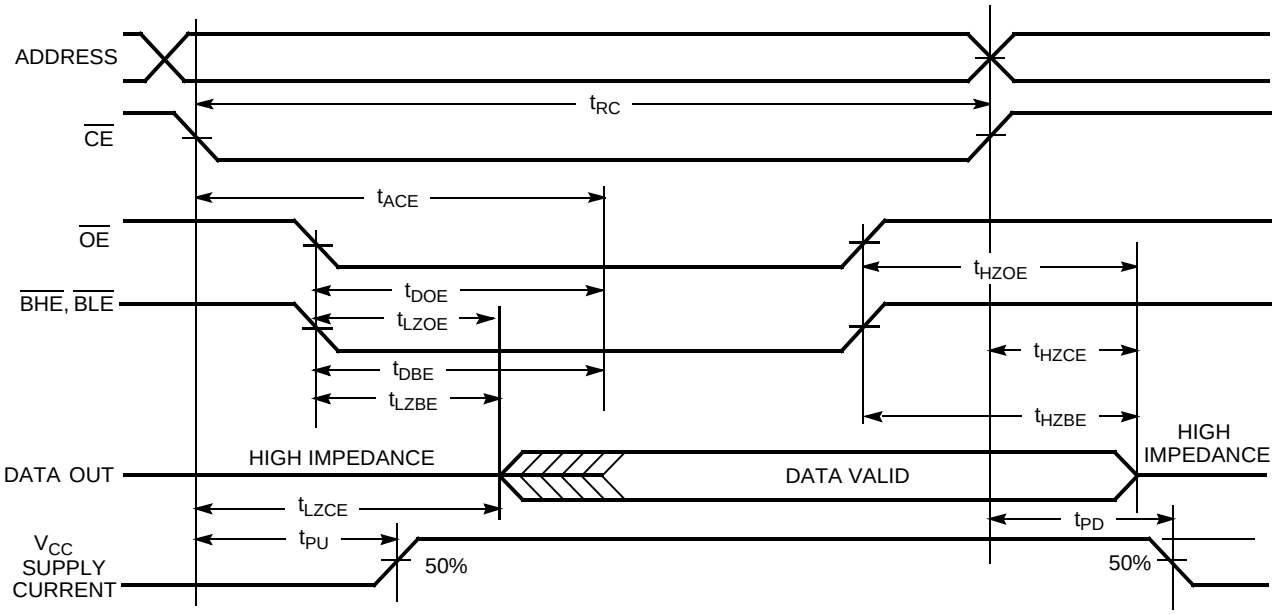


Figure 3. Read Cycle No. 2 (OE Controlled) [15,16]



Switching Waveforms (continued)

Figure 4. Write Cycle No. 1 ($\overline{CE}$ Controlled)[17, 18]

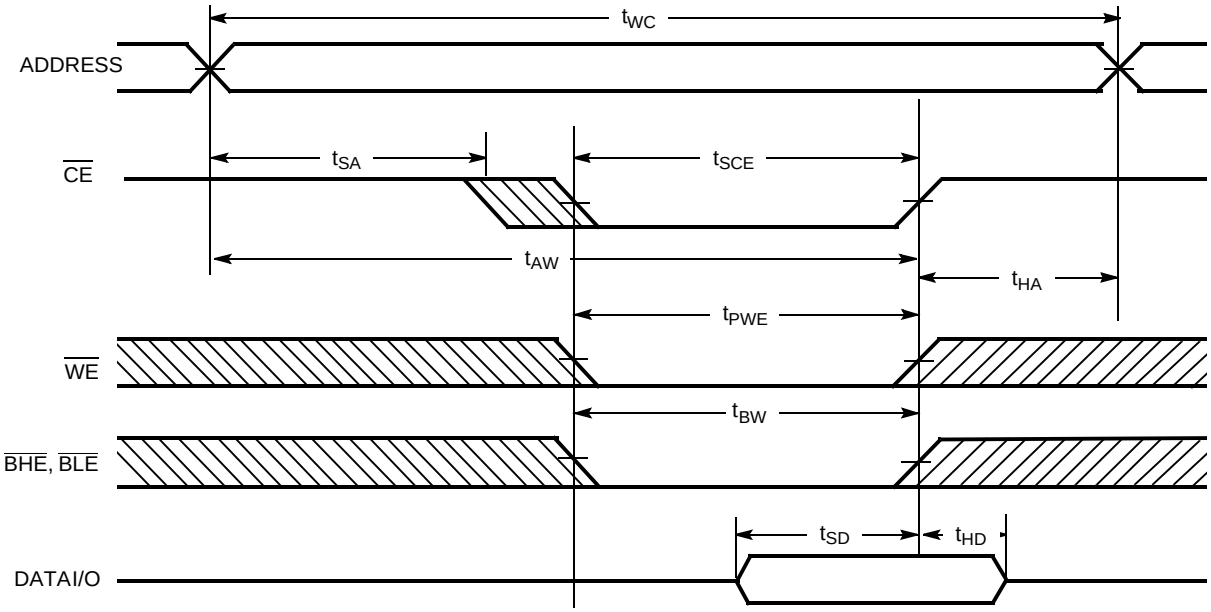
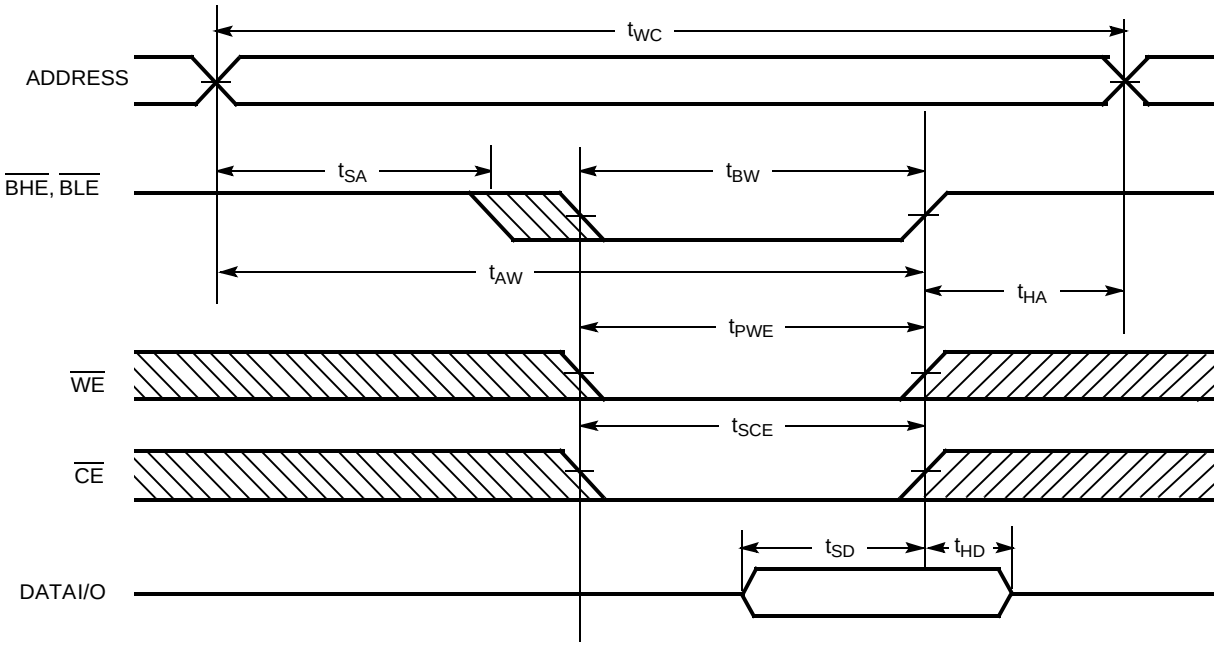


Figure 5. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW
17. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 3 (WE Controlled, OE HIGH During Write)[16, 17]

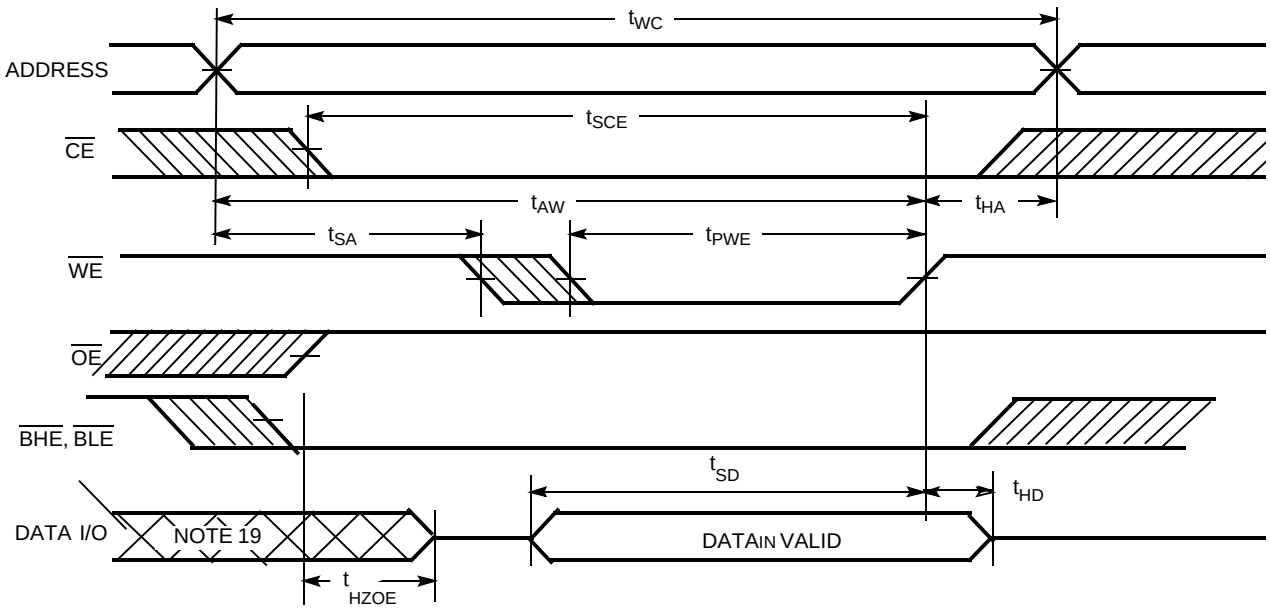
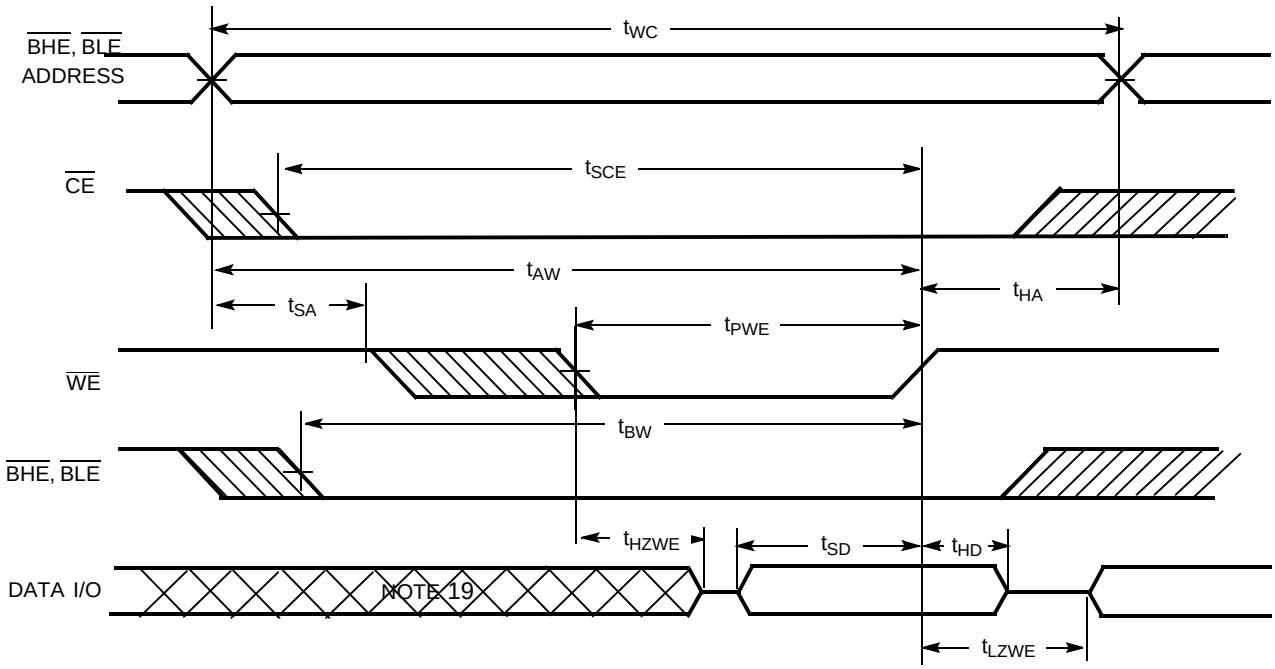


Figure 7. Write Cycle No. 4 (WE Controlled, OE LOW)



Note

19. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

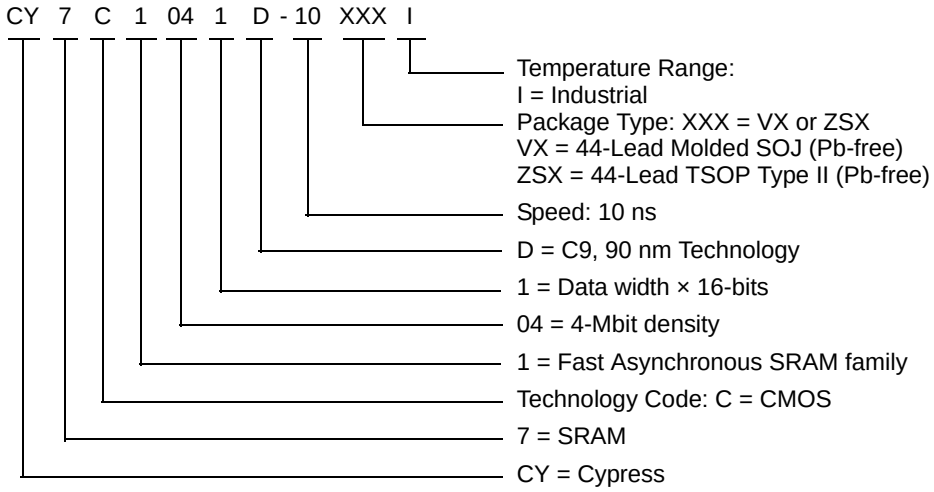
Ordering Information

Table 1 lists the CY7C1041D key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key Features and Ordering Information

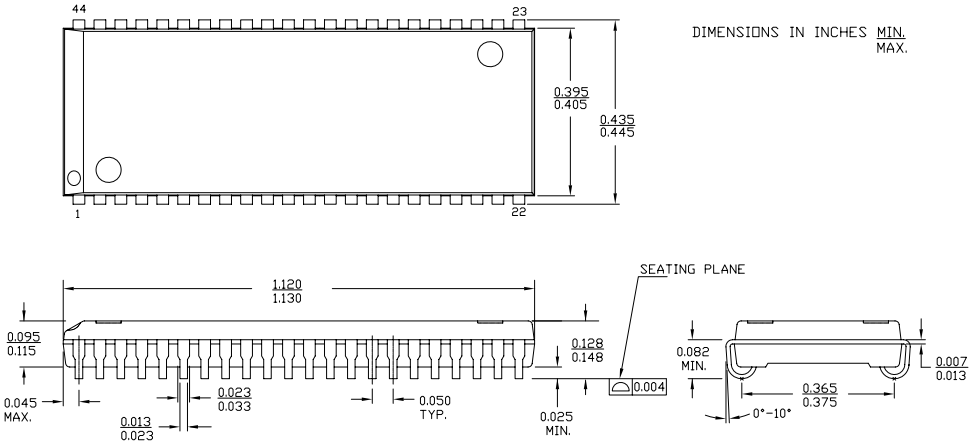
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041D-10VXI	51-85082	44-Pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1041D-10ZSXI	51-85087	44-Pin TSOP Type II (Pb-free)	

Ordering Code Definitions



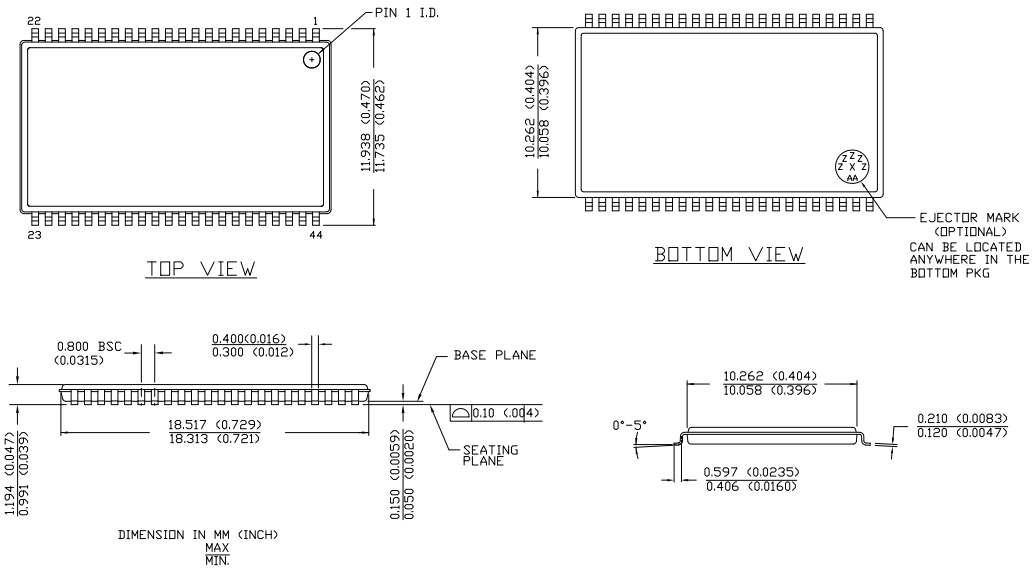
Package Diagrams

Figure 8. 44-Pin (400-Mil) Molded SOJ (51-85082)



51-85082 *C

Figure 9. 44-pin TSOP II (51-85087)



51-85087 *C

Acronyms

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title: CY7C1041D 4-Mbit (256K x 16) Static RAM Document Number: 38-05472				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201560	SWI	See ECN	Advance Datasheet for C9 IPP
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS (Spec #01-2165) 2.Pb-free offering in the 'ordering information'
*B	351117	PCI	See ECN	Changed from Advance to Preliminary Removed 17 and 20 ns Speed bin Added footnote # 4 Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I_{CC} (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Changed footnote # 10 on t_R Changed t_{SCE} from 8 to 7 ns for 10 ns speed bin Added Static Discharge Voltage and latch-up current spec Added $V_{IH(max)}$ spec in footnote # 2 Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Write Cycle ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) Timing Diagram Changed part names from Z to ZS in the Ordering Information Table Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Ordering Information Shaded Ordering Information Table
*C	446328	NXR	See ECN	Converted Preliminary to Final Removed -15 speed bin Removed Commercial Operating Range product information Added Automotive Operating Range product information Changed Maximum Rating for supply voltage from 7 V to 6 V Updated Thermal Resistance table Changed t_{HZWE} from 6 ns to 5 ns Updated footnote #8 on High-Z parameter measurement Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table
*D	2897049	VKN	03/22/10	Removed inactive parts from the ordering information table.
*E	3109184	AJU	12/13/2010	Added Ordering Code Definitions.
*F	3236731	PRAS	04/21/2011	Template updates. Added acronyms and units tables.

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