CY7C130

1 K × 8 Dual-Port Static RAM

Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1 K × 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 55 ns
- Low operating power: I_{CC} = 110 mA (maximum)
- Fully asynchronous operation
- Automatic power-down
- $\overline{BUSY}$ output flag on CY7C130
- $\overline{INT}$ flag for port-to-port communication
- Available in 48-pin DIP (CY7C130)

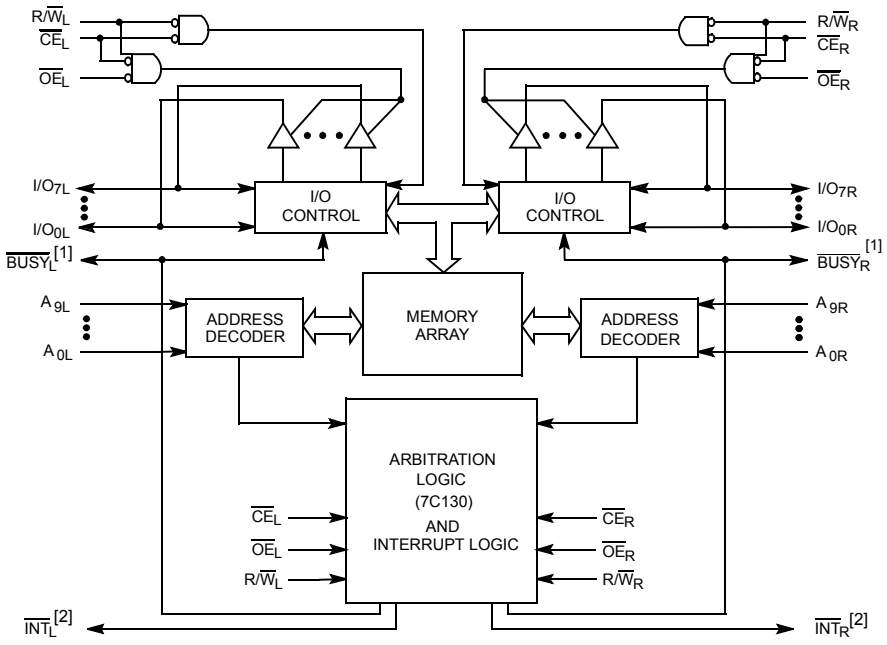
Functional Description

The CY7C130 is a high speed CMOS 1 K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130 can be used as a standalone 8-bit dual-port static RAM. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data is placed in a unique location (3FE for the left port and 3FF for the right port). An automatic power down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 is available in 48-pin DIP.

Logic Block Diagram

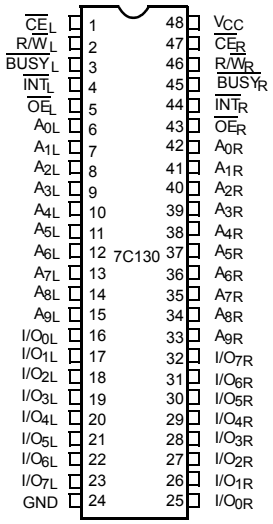


Notes
1. CY7C130 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
2. Open drain outputs: pull-up resistor required.

Contents

Pin Configurations

Figure 1. 48-pin DIP pinout (Top View)



Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
A_{0L}–A_{9L}	A_{0R}–A_{9R}	Address
I/O_{0L}–I/O_{7L}	I/O_{0R}–I/O_{7R}	Data bus input/output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
V_{CC}		Power
GND		Ground

Selection Guide

Parameter		7C130-55	Unit
Maximum access time		55	ns
Maximum operating current	Commercial	110	mA
Maximum standby current	Commercial	35	mA

Maximum Ratings

Exceeding maximum ratings [3] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential (pin 48 to pin 24) .....–0.5 V to +7.0 V

DC voltage applied to outputs in high Z State .....–0.5 V to +7.0 V

DC input voltage .....–3.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter [4]	Description	Test Conditions		7C130-55		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	I_{OL} = 4.0 mA		–	0.4	V
		I_{OL} = 16.0 mA [5]		–	0.5	V
V_{IH}	Input HIGH voltage			2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–5	+5	µA
I_{OS}	Output short circuit current [6, 7]	V_{CC} = Max, V_{OUT} = GND		–	–350	mA
I_{CC}	V_{CC} operating supply current	CE = V_{IL}, outputs open, f = f_{MAX} [8]	Commercial	–	110	mA
I_{SB1}	Standby current both ports, TTL inputs	CE_L and CE_R ≥ V_{IH}, f = f_{MAX} [8]	Commercial	–	35	mA
I_{SB2}	Standby current one port, TTL inputs	CE_L or CE_R ≥ V_{IH}, active port outputs open, f = f_{MAX} [8]	Commercial	–	75	mA
I_{SB3}	Standby current both ports, CMOS inputs	Both ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0	Commercial	–	15	mA
I_{SB4}	Standby current one port, CMOS inputs	One port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, active port outputs open, f = f_{MAX} [8]	Commercial	–	70	mA

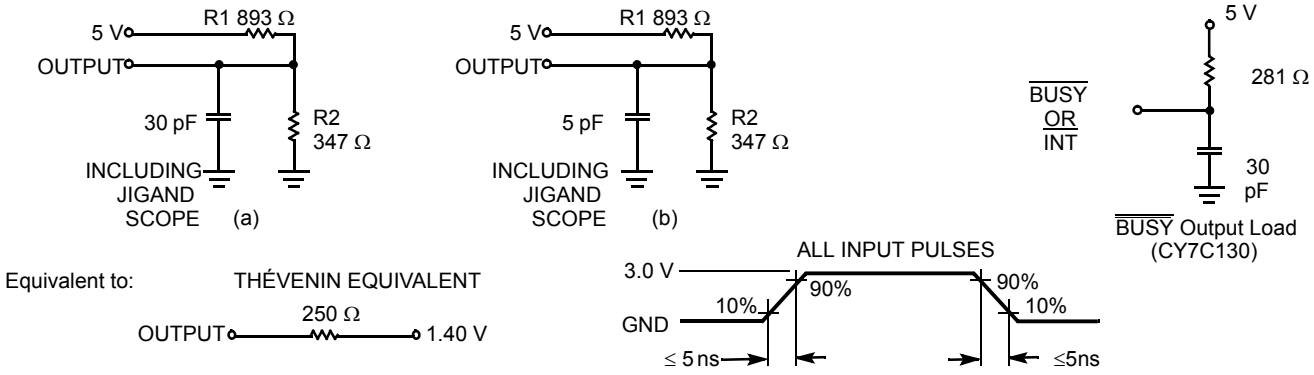
Notes
3. The voltage on any input or I/O pin cannot exceed the power pin during power up.
4. See the last page of this specification for Group A subgroup testing information.
5. BUSY and INT pins only.
6. Duration of the short circuit should not exceed 30 seconds.
7. This parameter is guaranteed but not tested.
8. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3 V.

Capacitance

Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	15	pF
C_{OUT}	Output capacitance		10	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range

Parameter [9, 10]	Description	7C130-55		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid [11]	–	55	ns
t_{OHA}	Data hold from address change	0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid [11]	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid [11]	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [12, 13, 14]	3	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [12, 13, 14]	–	25	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [12, 13, 14]	5	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [12, 13, 14]	–	25	ns
t_{PU}	$\overline{CE}$ LOW to power-up [12]	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [12]	–	35	ns
Write Cycle [15]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t_{AW}	Address set-up to write end	40	–	ns
t_{HA}	Address hold from write end	2	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	R/$\overline{W}$ pulse width	30	–	ns
t_{SD}	Data set-up to write end	20	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	R/$\overline{W}$ LOW to high Z [14]	–	25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to low Z [14]	0	–	ns

Notes

9. See the last page of this specification for Group A subgroup testing information.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH}, and 30 pF load capacitance.
11. AC Test Conditions use V_{OH} = 1.6 V and V_{OL} = 1.4 V.
12. This parameter is guaranteed but not tested.
13. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
14. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of Figure 2 on page 5. Transition is measured ±500 mV from steady state voltage.
15. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics *(continued)*

Over the Operating Range

Parameter [9, 10]	Description	7C130-55		Unit
		Min	Max	
Busy/Interrupt Timing				
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch [16]	–	30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[16]	–	30	ns
t_{PS}	Port set-up for priority	5	–	ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	35	–	ns
t_{BDD}	$\overline{BUSY}$ HIGH to valid data	–	45	ns
t_{DDD}	Write data valid to read data valid	–	Note 17	ns
t_{WDD}	Write pulse to data delay	–	Note 17	ns
Interrupt Timing				
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ set time	–	45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ set time	–	45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ set time	–	45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ reset time [18]	–	45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ reset time [18]	–	45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ reset time [18]	–	45	ns

Notes

16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    BUSY on Port B goes HIGH.
    Port B's address is toggled.
    $\overline{CE}$ for Port B is toggled.
    R/$\overline{W}$ for Port B is toggled during valid read.
18. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of Figure 2 on page 5. Transition is measured ±500 mV from steady state voltage.

Switching Waveforms

Figure 3. Read Cycle No. 1 [19, 20]

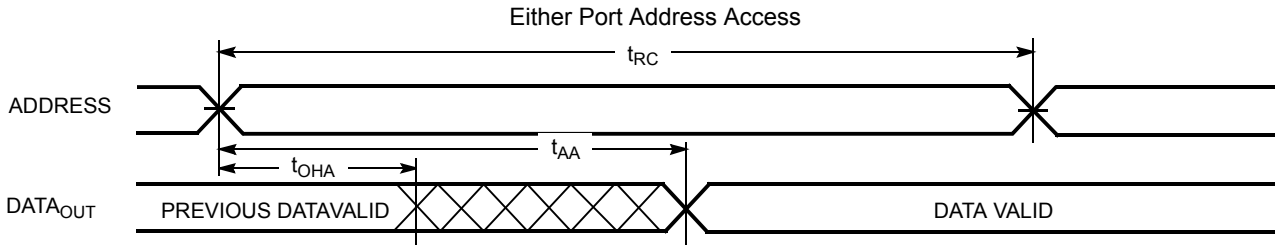


Figure 4. Read Cycle No. 2 [19, 21]

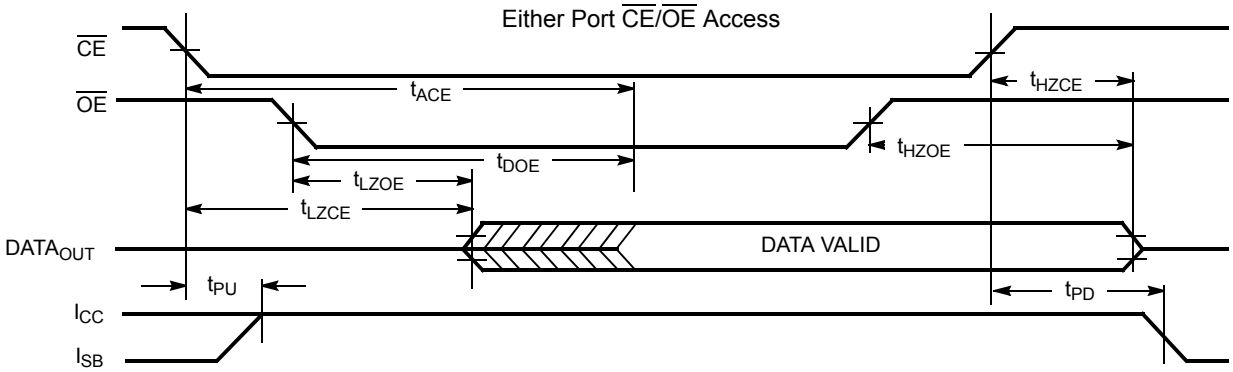
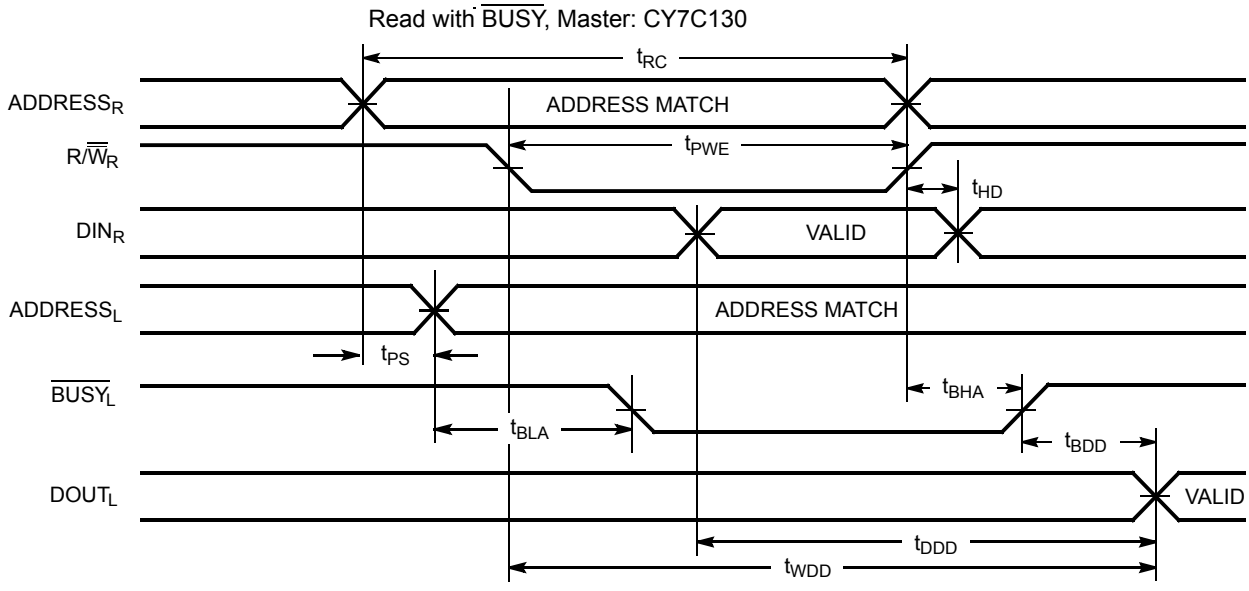


Figure 5. Read Cycle No. 3 [20]



Notes
19. R/W is HIGH for read cycle.
20. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
21. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{OE}$ Three-States Data I/Os – Either Port [22, 23]

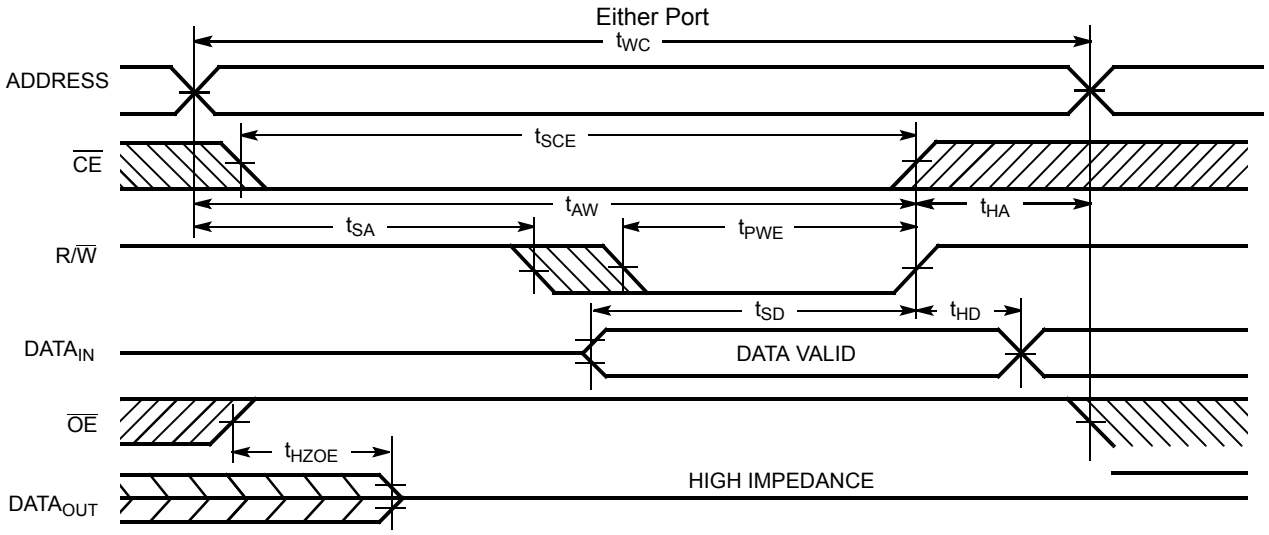
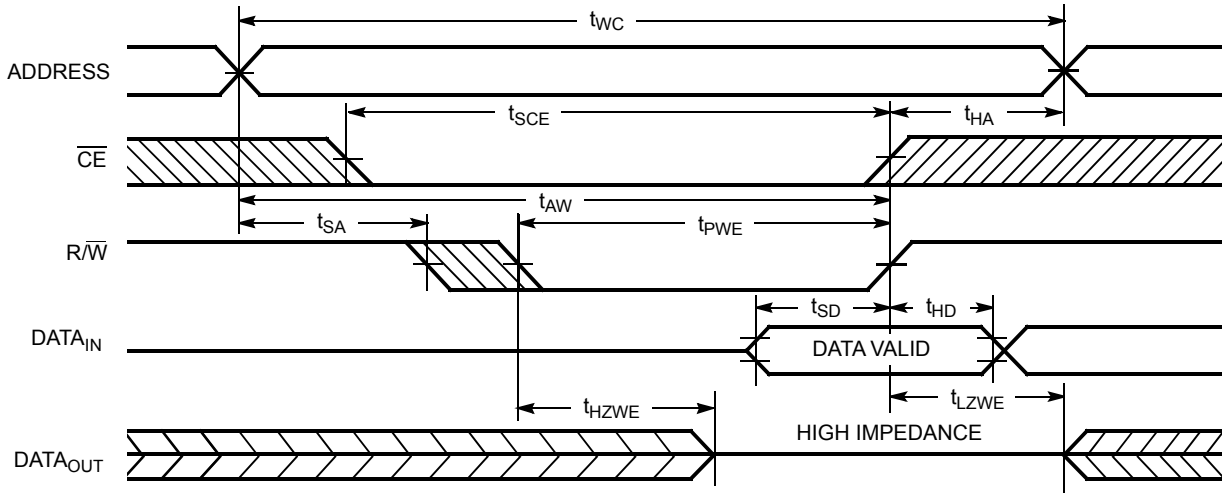


Figure 7. Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port) [24, 25]



Notes

22. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
24. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
25. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.

Switching Waveforms *(continued)*

Figure 8. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

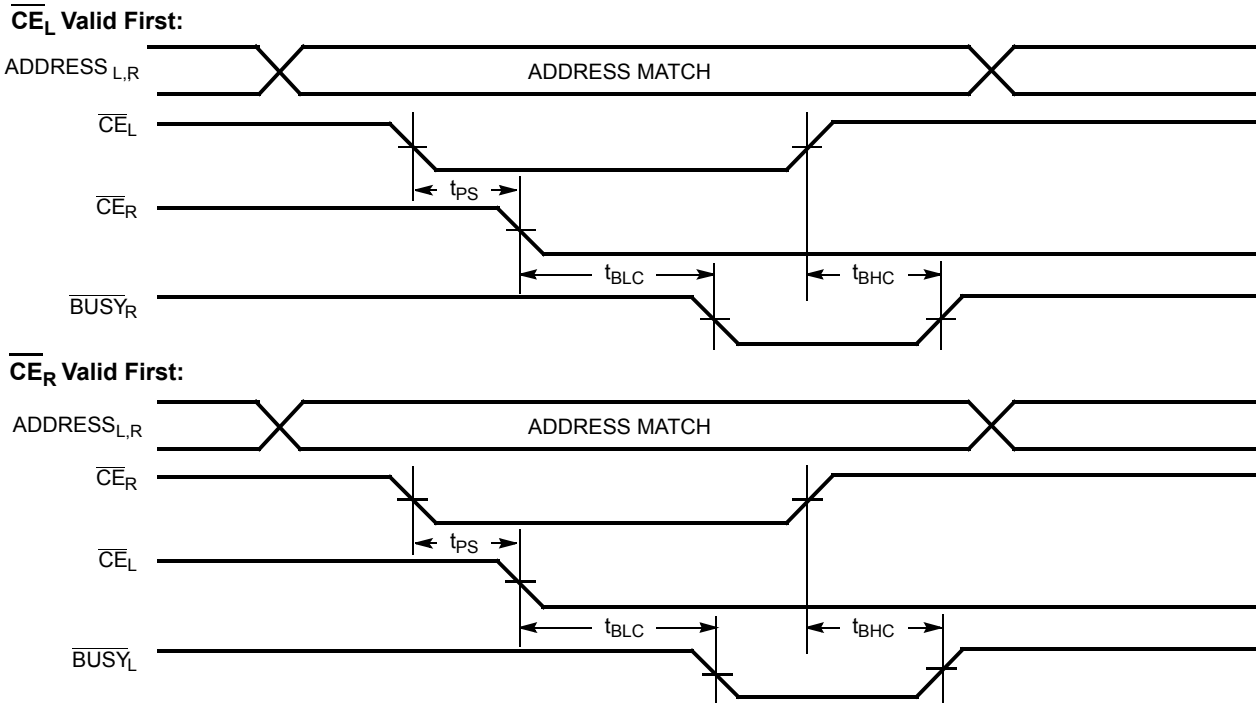
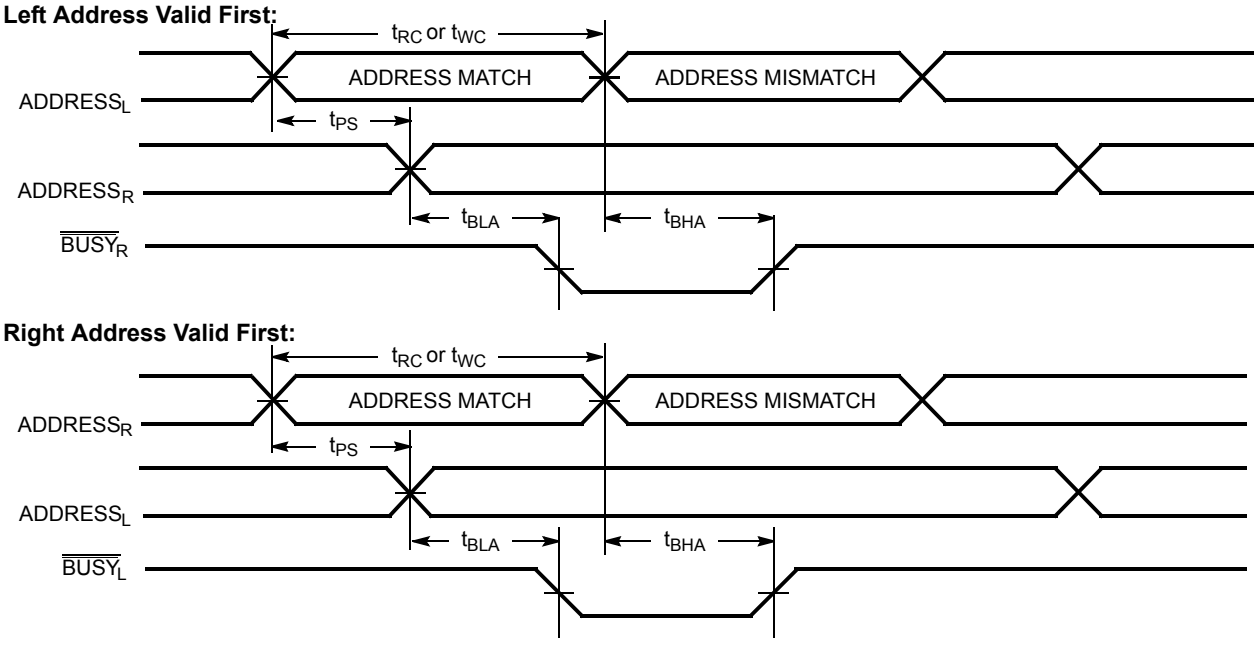
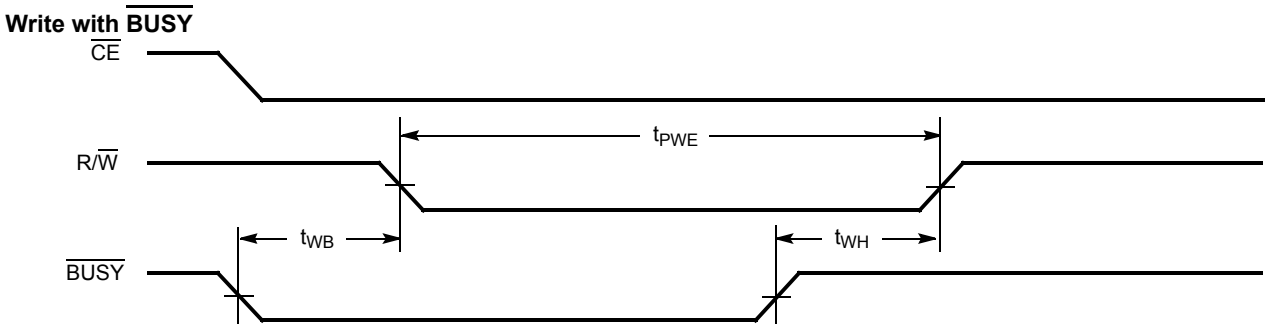


Figure 9. Busy Timing Diagram No. 2 (Address Arbitration)



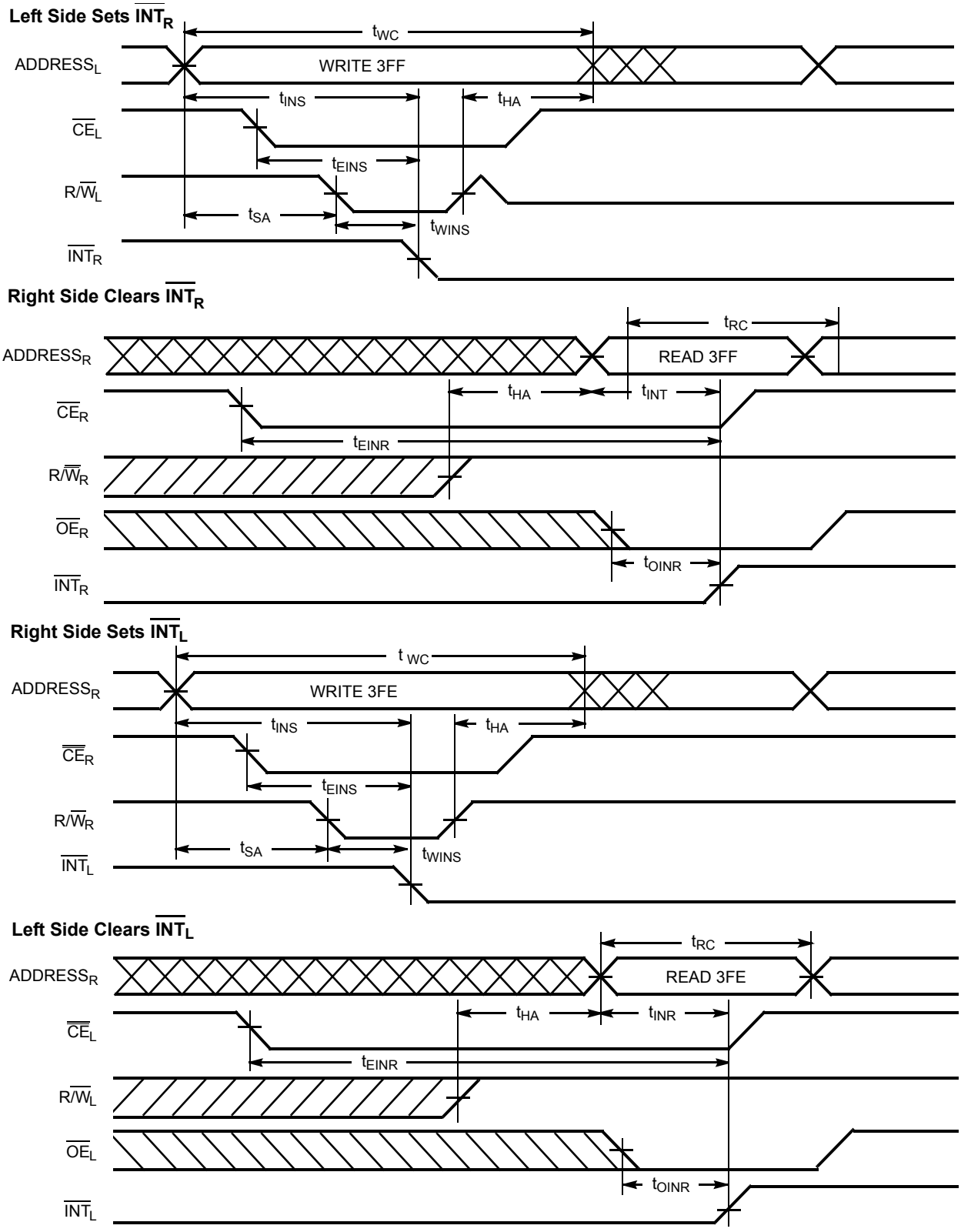
Switching Waveforms *(continued)*

Figure 10. Busy Timing Diagram No. 3



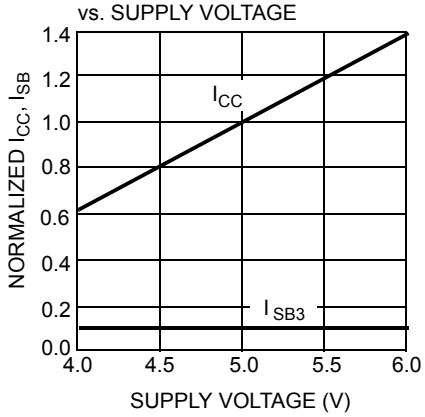
Switching Waveforms *(continued)*

Figure 11. Interrupt Timing Diagrams

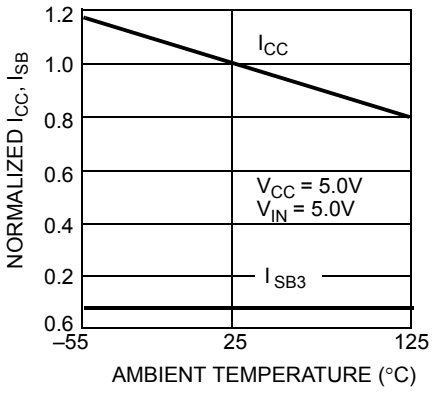


Typical DC and AC Characteristics

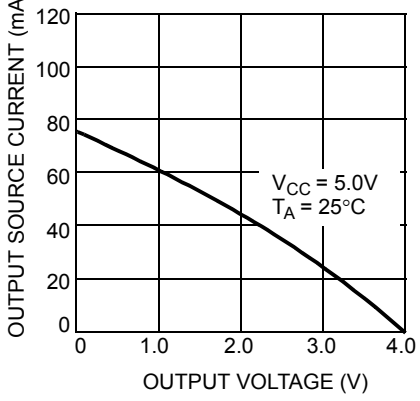
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



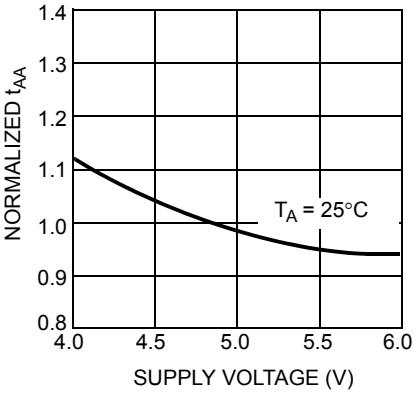
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



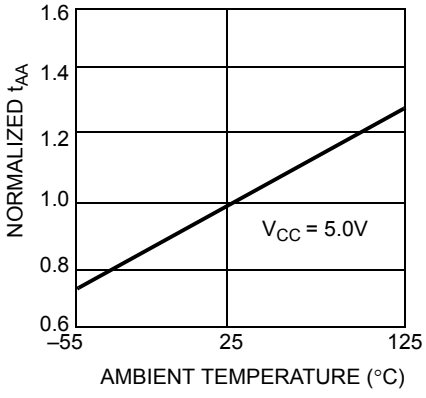
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



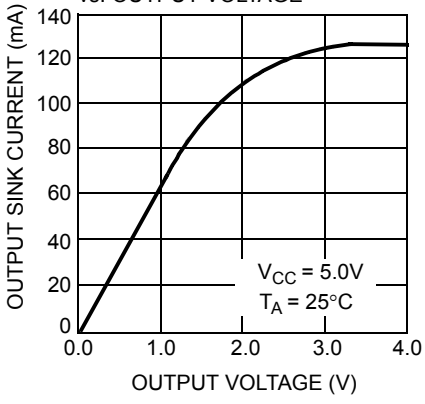
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



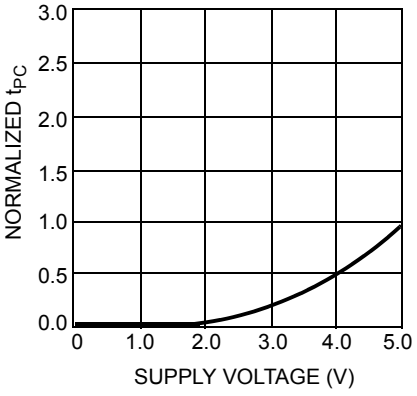
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



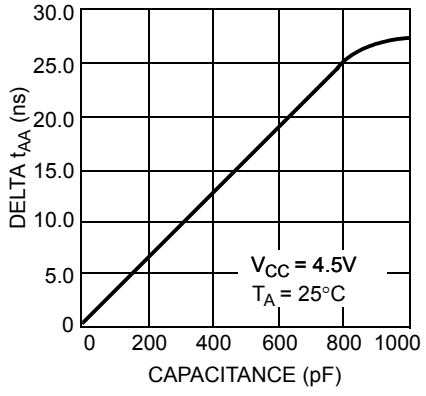
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



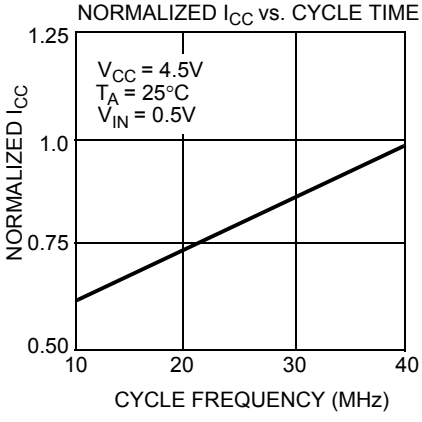
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



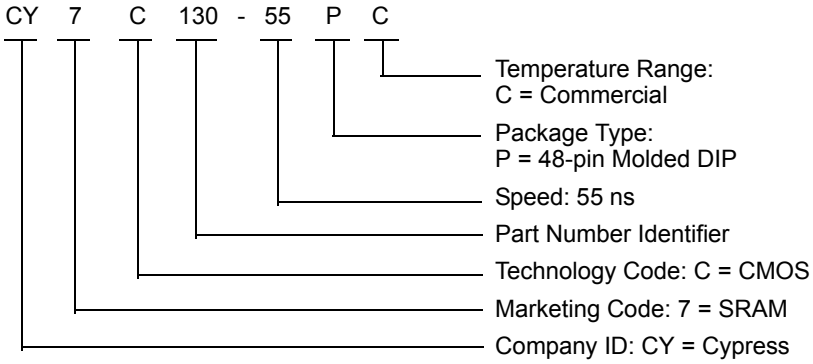
NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

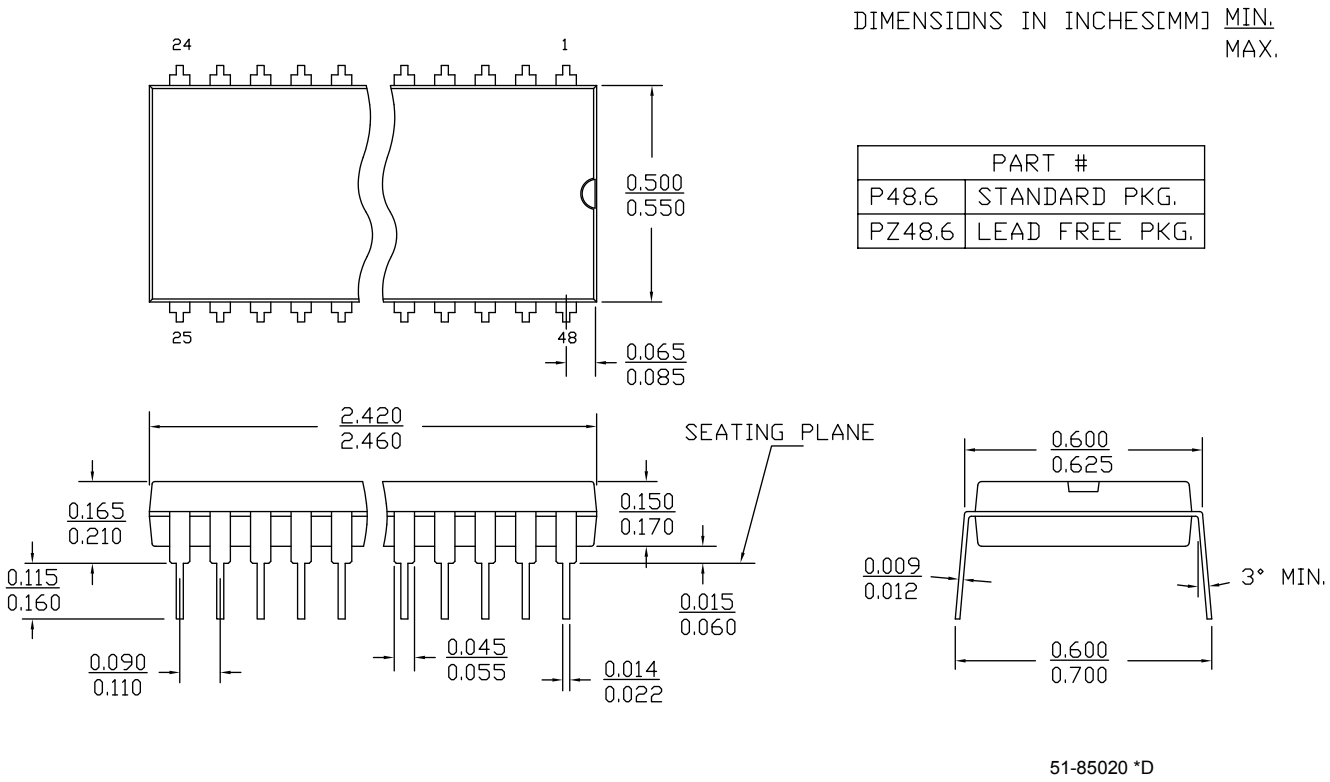
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY7C130-55PC	P25	48-pin (600 Mil) Molded DIP	Commercial

Ordering Code Definitions



Package Diagrams

Figure 12. 48-pin PDIP (2.460 × 0.550 × 0.170 inches) P48.6 Package Outline, 51-85020



Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
DIP	dual in-line package
I/O	input/output
$\overline{OE}$	output enable
PDIP	plastic dual in-line package
SRAM	static random access memory
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C130, 1 K × 8 Dual-Port Static RAM Document Number: 38-06002				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110169	SZV	09/29/01	Change from Spec number: 38-00027 to 38-06002
*A	122255	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	236751	YDT	See ECN	Removed cross information from features section
*C	325936	RUY	See ECN	Added pin definitions table, 52-pin PQFP package diagram and Pb-free information
*D	393153	YIM	See ECN	Added CY7C131-15JI to ordering information Added Pb-Free parts to ordering information: CY7C131-15JXI
*E	2623540	VKN/PYRS	12/17/08	Added CY7C130A and CY7C131A parts Removed military information Updated ordering information.
*F	2897217	RAME	03/22/2010	Updated Ordering Information. Updated Package Diagrams.
*G	3054633	ADMU	10/11/2010	Updated Ordering Information and added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*H	3402163	ADMU	10/12/2011	Removed pruned part CY7C131-25NC from Ordering Information Updated Package Diagrams.
*I	3796621	SMCH	10/29/2012	Updated Features (Removed CY7C130A, CY7C131, CY7C131A related information; removed 52-pin PLCC, 52-pin TQFP package related information). Updated Functional Description (Removed CY7C130A, CY7C131, CY7C131A related information; removed 52-pin PLCC, 52-pin TQFP package related information). Updated Pin Configurations (Removed 52-pin PLCC, 52-pin TQFP package related information). Updated Selection Guide (Removed CY7C130A, CY7C131, CY7C131A related information; removed 15 ns, 25 ns, 30 ns, 35 ns, 45 ns speed bins information, removed Industrial temperature range information). Updated Operating Range (Removed Industrial temperature range and Military temperature range information). Updated Electrical Characteristics (Removed CY7C130A, CY7C131, CY7C131A related information; removed 15 ns, 25 ns, 30 ns, 35 ns, 45 ns speed bins information). Updated Switching Characteristics (Removed CY7C130A, CY7C131, CY7C131A related information; removed 15 ns, 25 ns, 30 ns speed bins information). Updated Switching Characteristics (Removed CY7C130A, CY7C131, CY7C131A related information; removed 35 ns, 45 ns speed bins information). Updated Ordering Information (Updated part numbers). Updated Package Diagrams (Removed 52-pin PLCC, 52-pin TQFP package related information).

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