

256Kx1 Static RAM

Features

- **High speed**
— 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
— 880 mW
- **Low standby power**
— 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is pro-

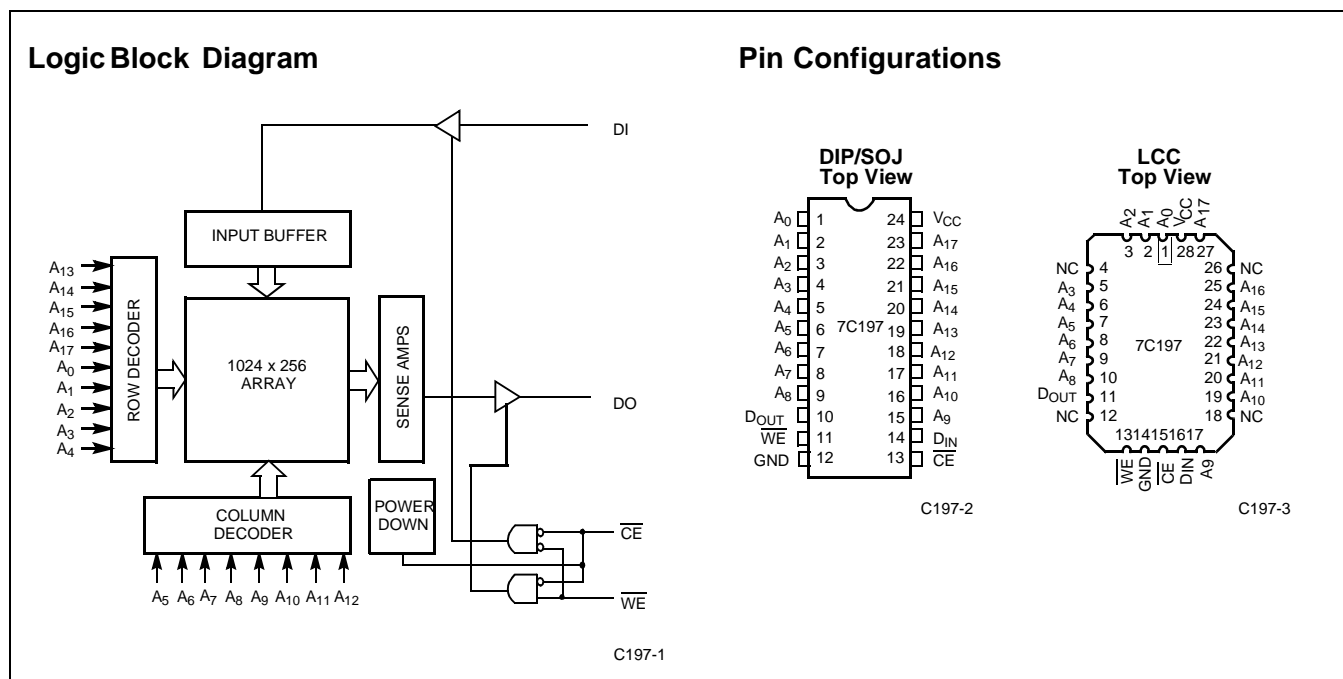
vided by an active LOW Chip Enable (\overline{CE}) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable (\overline{CE}) LOW while Write Enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when Chip Enable (\overline{CE}) is HIGH or Write Enable (\overline{WE}) is LOW.

The CY7C197 utilizes a die coat to insure alpha immunity.



Selection Guide

| | 7C197-12 | 7C197-15 | 7C197-20 | 7C197-25 | 7C197-35 | 7C197-45 |
|--------------------------------|----------|----------|----------|----------|----------|----------|
| Maximum Access Time (ns) | 12 | 15 | 20 | 25 | 35 | 45 |
| Maximum Operating Current (mA) | 150 | 140 | 135 | 95 | 95 | |
| Maximum Standby Current (mA) | 30 | 30 | 30 | 30 | 30 | 30 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1]..... -0.5V to $V_{CC} + 0.5V$
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|----------|
| Commercial | 0°C to +70°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C197-12 | | 7C197-15 | | Unit |
|-----------|---|--|----------|-----------------|----------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 12.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3V$ | 2.2 | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -5 | +5 | -5 | +5 | µA |
| I_{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -5 | +5 | -5 | +5 | µA |
| I_{OS} | Output Short Circuit Current ^[2] | $V_{CC} = \text{Max.}, V_{OUT} = GND$ | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$ | | 150 | | 140 | mA |
| I_{SB1} | Automatic \overline{CE} Power-Down Current—TTL Inputs ^[3] | Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 30 | | 30 | mA |
| I_{SB2} | Automatic \overline{CE} Power-Down Current—CMOS Inputs ^[3] | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} < 0.3V$ | | 10 | | 10 | mA |

Notes:

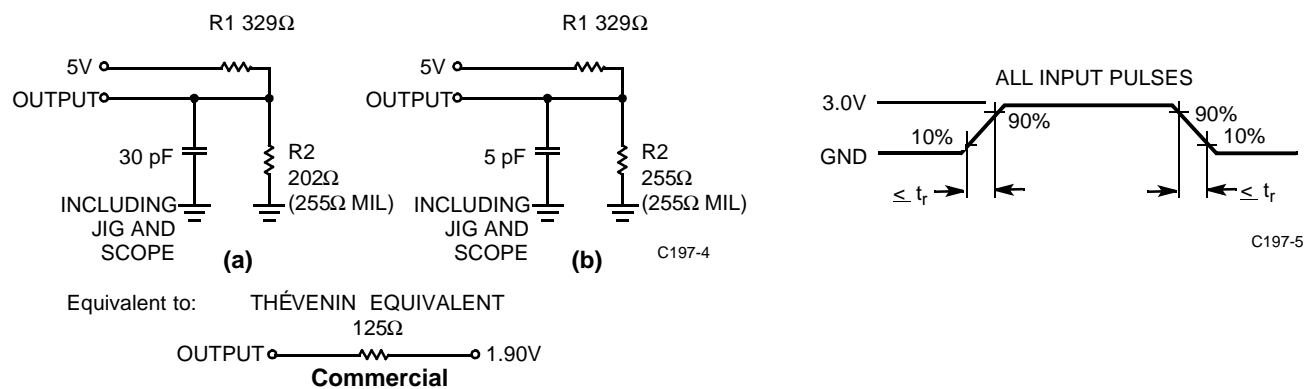
- $V_{(min.)} = -2.0V$ for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | Test Conditions | 7C197-20 | | 7C197-25, 35, 45 | | Unit |
|------------------|---|--|----------|------------------------|------------------|------------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 12.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3V | 2.2 | V _{CC} + 0.3V | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | -5 | +5 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output Short Circuit Current ^[2] | V _{CC} = Max., V _{OUT} = GND | | -300 | | -300 | mA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 135 | | 95 | mA |
| I _{SB1} | Automatic \overline{CE} Power Down Current—TTL Inputs ^[3] | Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 30 | | 30 | mA |
| I _{SB2} | Automatic \overline{CE} Power-Down Current—CMOS Inputs ^[3] | Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} < 0.3V | | 15 | | 15 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 8 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

AC Test Loads and Waveforms^[5]

Notes:

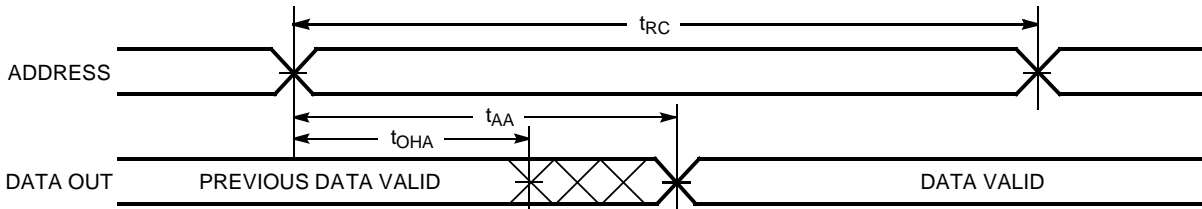
4. Tested initially and after any design or process changes that may affect these parameters.
5. t_r = ≤ 3 ns for the -12 and -15 speeds. t_r = ≤ 5 ns for the -20 and slower speeds.

Switching Characteristics Over the Operating Range^[6]

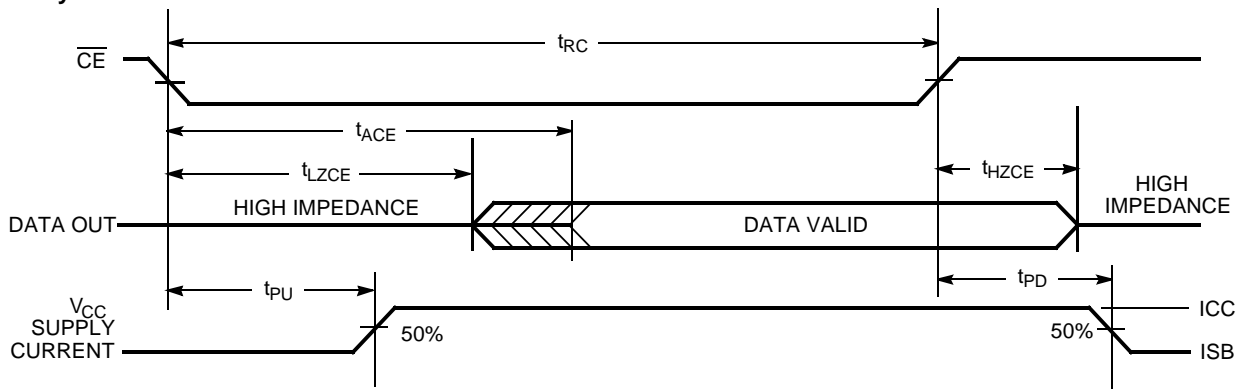
| Parameter | Description | 7C197-12 | | 7C197-15 | | 7C197-20 | | 7C197-25 | | 7C197-35 | | 7C197-45 | | Unit |
|----------------------------------|--|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| t _{OHA} | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[7] | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[7, 8] | | 5 | | 7 | 0 | 9 | 0 | 11 | 0 | 15 | 0 | 15 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 12 | | 15 | | 20 | | 20 | | 25 | | 30 | ns |
| WRITE CYCLE^[9] | | | | | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 9 | | 10 | | 15 | | 20 | | 30 | | 40 | | ns |
| t _{AW} | Address Set-Up to Write End | 9 | | 10 | | 15 | | 20 | | 30 | | 40 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 8 | | 9 | | 15 | | 20 | | 25 | | 30 | | ns |
| t _{SD} | Data Set-Up to Write End | 8 | | 9 | | 10 | | 15 | | 17 | | 20 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 2 | | 2 | | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[7, 8] | | 7 | | 7 | 0 | 10 | 0 | 11 | 0 | 15 | 0 | 15 | ns |

Notes:

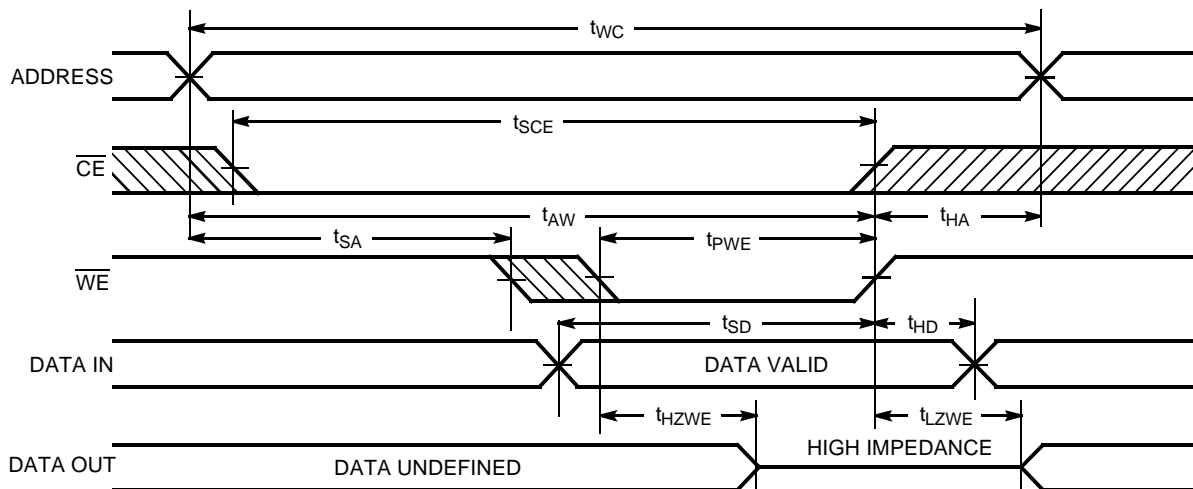
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1 ^[10, 11]


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Read Cycle No. 2 ^[10]


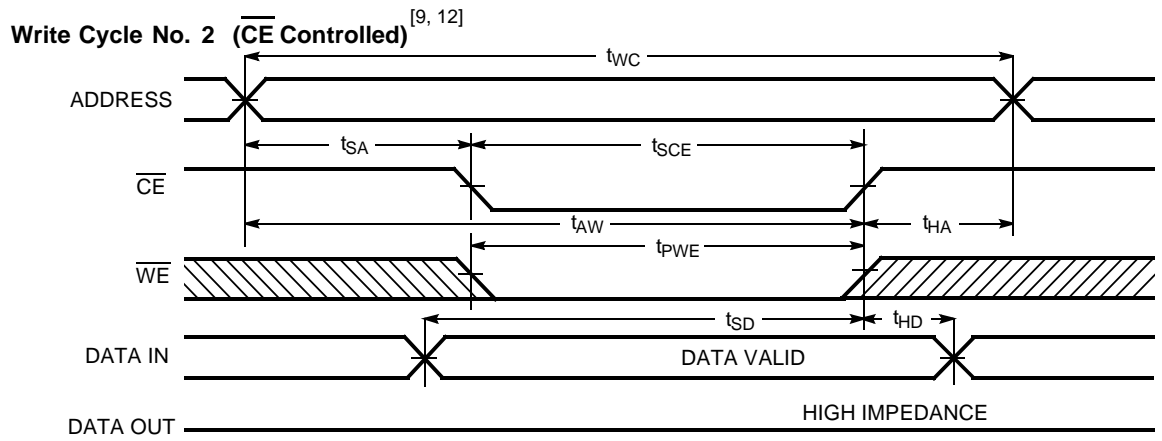
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Write Cycle No. 1 (WE Controlled) ^[9]


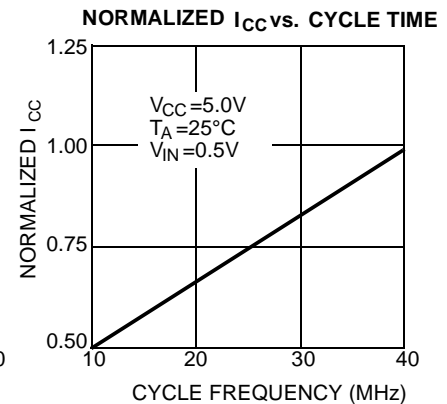
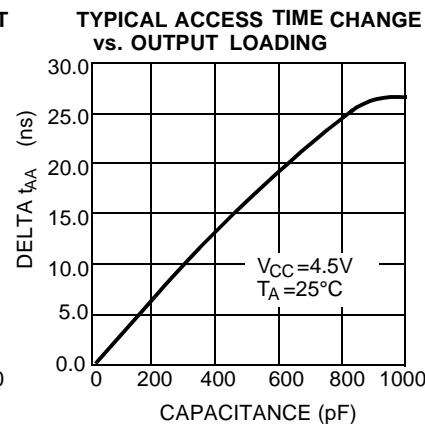
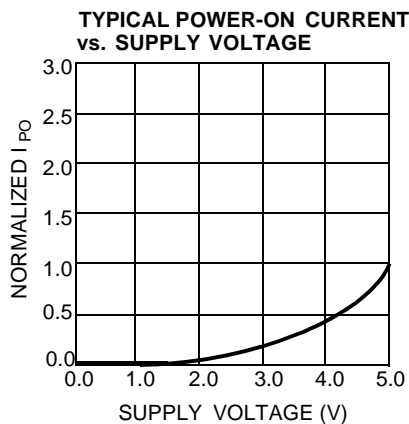
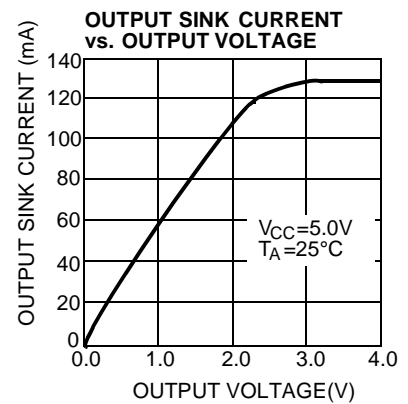
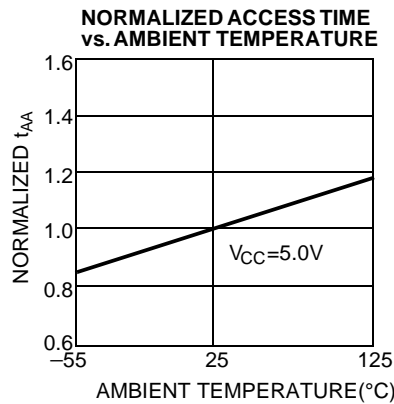
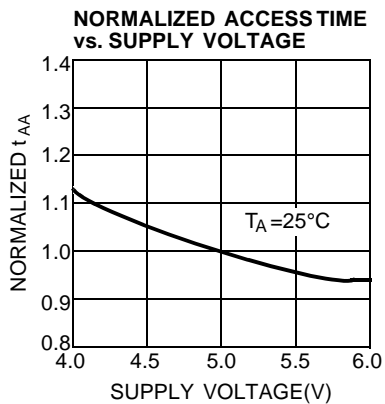
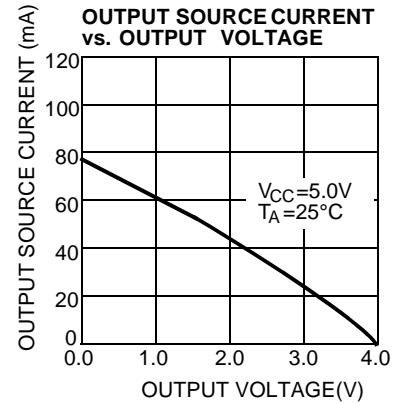
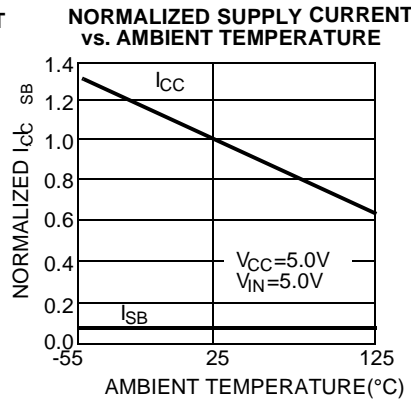
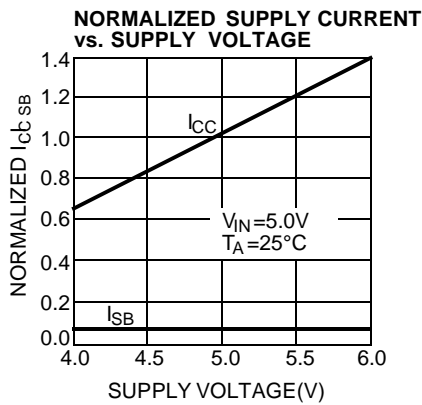
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Notes:

10. WE is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms (continued)

Note:

12. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics


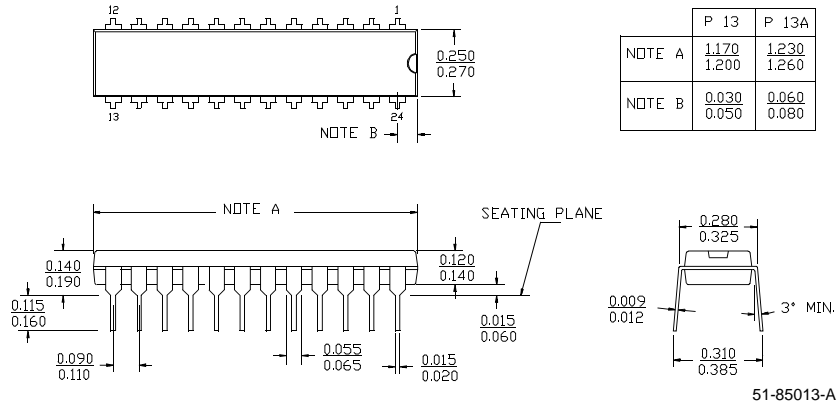
CY7C197 Truth Table

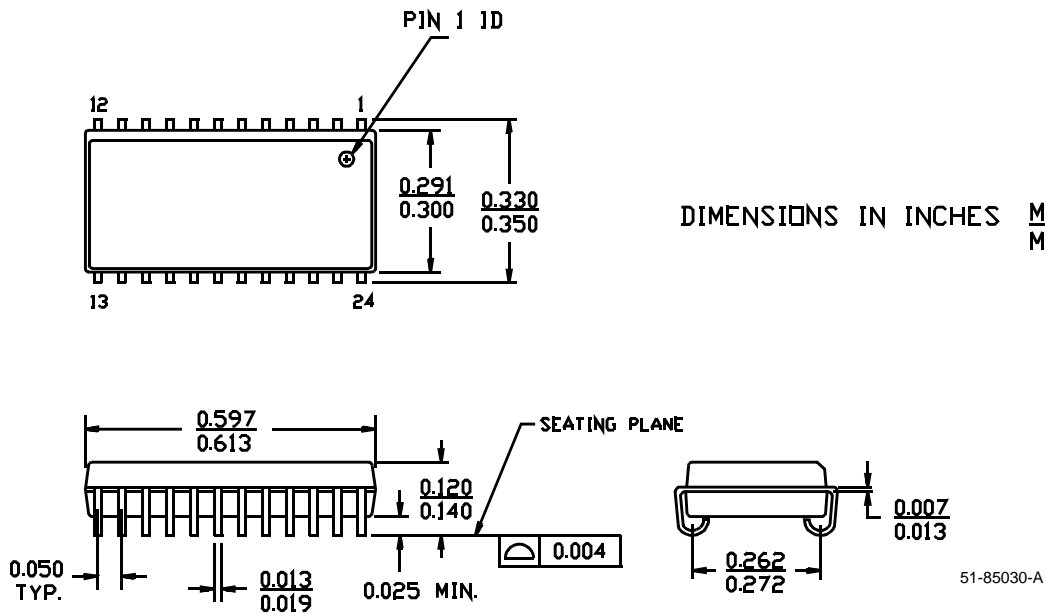
| CE | WE | Input/Output | Mode |
|-----------|-----------|---------------------|---------------------|
| H | X | High Z | Deselect/Power-Down |
| L | H | Data Out | Read |
| L | L | Data In | Write |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------------|----------------------|---------------------|------------------------------|------------------------|
| 12 | CY7C197-12PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-12VC | V13 | 24-Lead Molded SOJ | |
| 15 | CY7C197-15PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-15VC | V13 | 24-Lead Molded SOJ | |
| 20 | CY7C197-20PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-20VC | V13 | 24-Lead Molded SOJ | |
| 25 | CY7C197-25PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-25VC | V13 | 24-Lead Molded SOJ | |
| 35 | CY7C197-35PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-35VC | V13 | 24-Lead Molded SOJ | |
| 45 | CY7C197-45PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C197-45VC | V13 | 24-Lead Molded SOJ | |

Package Diagrams
24-Lead (300-Mil) Molded DIP P13/P13A

 DIMENSIONS IN INCHES MIN.
MAX.

24-Lead (300-Mil) Molded SOJ V13

 DIMENSIONS IN INCHES MIN.
MAX.


| Document Title: CY7C197 256K x 1 Static RAM Document Number: 38-05049 | | | | |
|--|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 107151 | 09/10/01 | SZV | Change from Spec number: 38-00078 to 38-05049 |