ISD-300LP™
Low-Power USB 2.0 to ATA/ATAPI Bridge IC

Cypress Semiconductor Corporation • 3901 North First Street • San Jose, CA 95134 • 408-943-2600
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1.0 Introduction

The CY7C68310 implements a bridge between one USB port and one ATA/ATAPI-based mass storage device port. This bridge adheres to the *Mass Storage Class Bulk-Only Transport* specification, version 1.0.

The USB port of the CY7C68310 is connected to a host computer directly or via the downstream port of a USB hub. Host software issues commands and data to the CY7C68310 and receives status and data from the CY7C68310 using standard USB protocol.

The ATA/ATAPI port of the CY7C68310 is connected to a mass storage device. A 2-Kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0–4, and Ultra Mode DMA modes 0–4.

The device initialization process is configurable, enabling the CY7C68310 to initialize most ATA/ATAPI devices without software intervention. The CY7C68310 can also be configured to allow software initialization of a device if initialization requirements are not supported by CY7C68310 algorithms.

1.1 Features

- Fixed-function mass storage device–requires no firmware code
- USB *Mass Storage Class Bulk-Only* specification-compliant (version 1.0)
- USB 2.0-compliant
  - Integrated USB transceiver
  - High-speed (480-Mbit) and full-speed (12-Mbit) support
  - USB Suspend/Resume, remote wakeup support
- Two power modes of operation–self-powered and USB bus-powered
  - Low power allows for bus-powered operation
  - VBUS-powered CF support
- Compact 80-pin TQFP package
- *ATA/ATAPI-6* specification-compliant–provides support for mass storage devices larger than 137GB
- 5V tolerant inputs, 3.3V output drive
- Flexible USB descriptor and configuration retrieval sources
  - I^2C-compatible serial ROM interface
  - ATA interface using vendor-specific ATA command (FBh) implemented on ATAPI or ATA device
  - Default on-chip ROM contents for manufacturing/development
- 2-Kbyte SRAM data buffer for ATA/ATAPI data transfers
- ATA interface supports ATA PIO modes 0–4, UDMA modes 0–4 (multi-word DMA not supported). ATA interface operation mode is automatically selected during device initialization or manually programmed with I^2C-compatible configuration data
- Automatic detection of either Master or Slave ATA/ATAPI devices
- Mode Page 5 Support–increased support for formatting removable media devices
- ATA Interrupt support for ATAPI devices–offers more robust ATA support across OS platforms
- System event notification via Vendor-specific ATA command
  - Input pin for media cartridge detection or ejection request
  - USB bus state indications (Reset, FS/HS mode of operation, Suspend/Resume, Bus/Self-powered)
- Three General Purpose I/O (GPIO) pins
- Multiple LUNs supported within a single ATAPI device
- ATA translation provides seamless ATA support with standard MSC drivers
- Additional ATA command support provided by vendor-specific ATACBs (ATA command blocks utilizing the MSC Command Block Wrapper)
- Provisions to share ATA bus with other hosts (e.g. USB/1394 dual device)
- Manufacturing interconnect test support provided with vendor-specific USB commands:
  - Read/Write access to relevant ASIC pins
  - Manufacturing Interconnect Test Tools
- Utilizes inexpensive 30-Mhz crystal for clock source.

1.2 Applications

The CY7C68310 implements a USB 2.0 bridge for all ATA/ATAPI-6 compliant mass storage devices, such as:

- Hard drives
- CDROM, CDR/W
- DVDROM, DVDRAM, DVDR/W
- MP3 Players
- Compact Flash
- Microdrives
- Tape drives
- Personal Video Recorders.

1.3 Additional Resources

- CY4617–CY7C68310 Mass Storage Reference Design Kit
- *USB Specification* version 2.0
- ATA Attachment-6 with Packet Interface revision 3b
- USB *Mass Storage Class Bulk-Only Transport* specification, Rev. 1.0

1.4 Functional Block Diagram

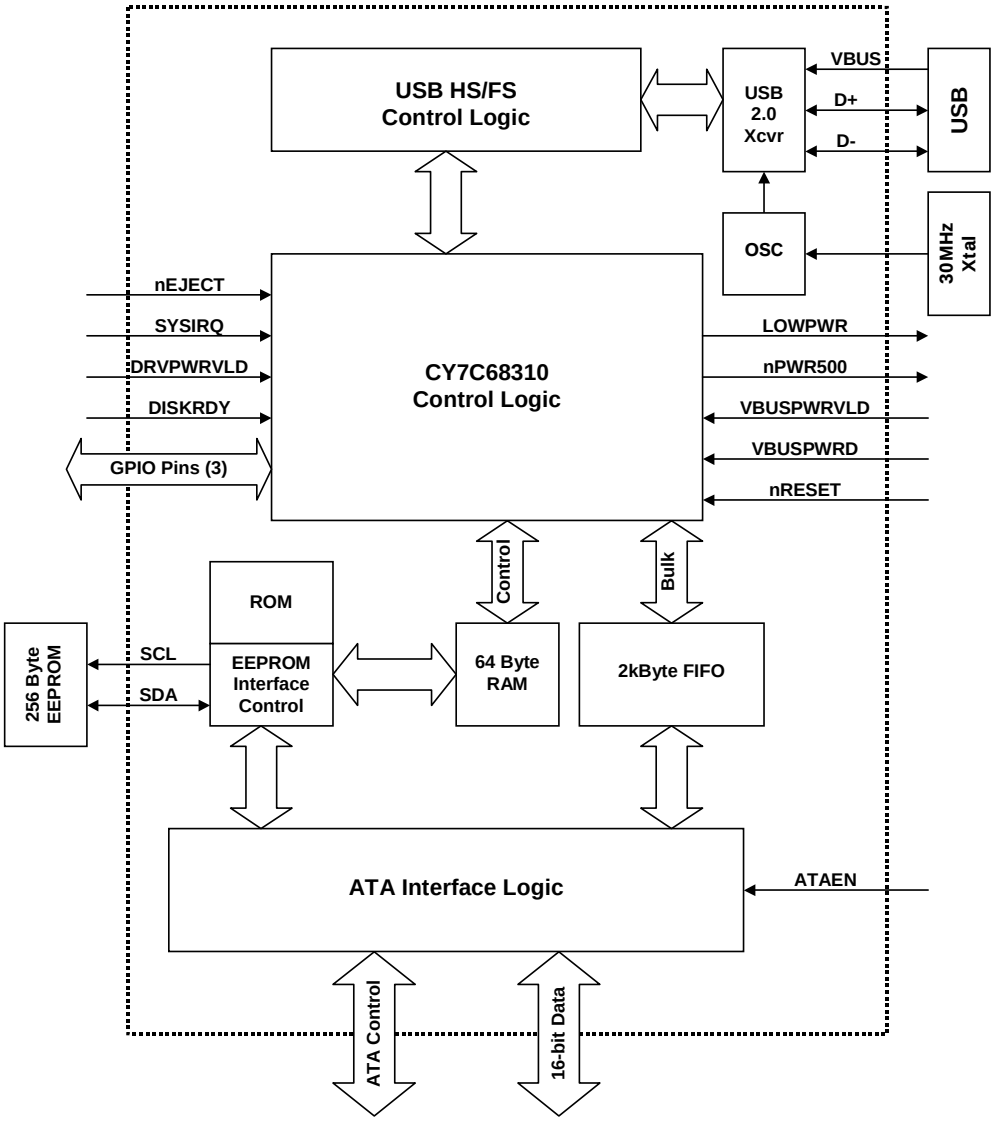


Figure 1-1. Block Diagram

2.0 Pin Assignments

2.1 Pin Diagram

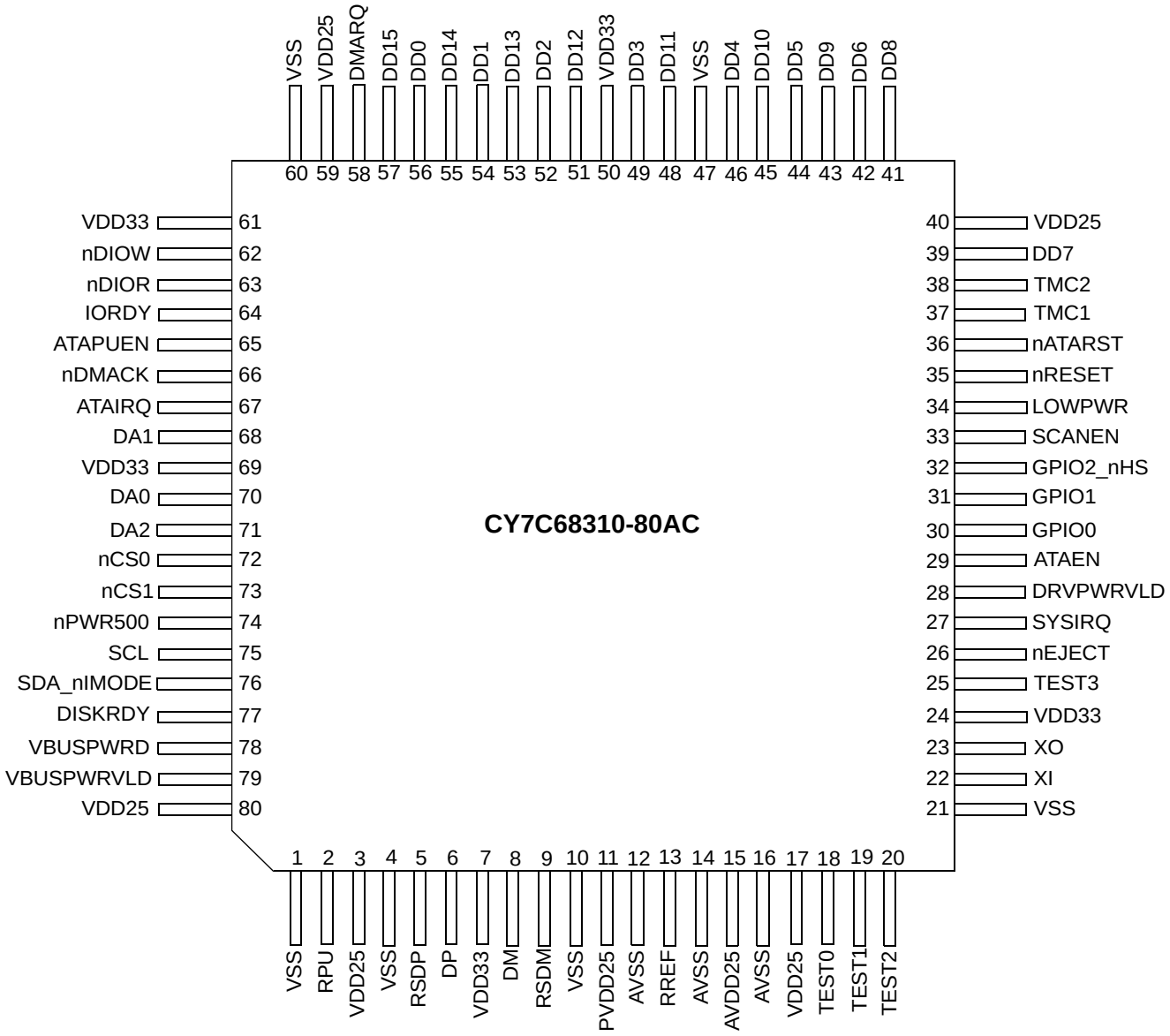


Figure 2-1. 80-pin TQFP

2.2 Pin Overview

Pin Number	Pin Name	Pin Direction	Pin Type	Pin Description
2	RPU	O	USB Output	**D+ pull-up source**. Power source for 1.5k pull-up resistor attached to D+ during full speed operation.
5	RSDP	O	USB I/O	**USB full speed output buffer (D+)**. RSDP also functions as a current sink for termination during high speed operation.
6	DP	I/O	USB I/O	**USB high speed I/O buffer (D+)**.
8	DM	I/O	USB I/O	**USB high speed I/O buffer (D-)**.
9	RSDM	O	USB I/O	**USB full speed output buffer (D-)**. RSDM also functions as a current sink for termination during high speed operation.
18-20, 25	TEST[0:3]	I	5V-tolerant input buffer	**Active HIGH**. ASIC fabrication and manufacturing test mode select. These pins must be tied to GND during normal operation.
22	XI	I	OSC input (2.5V-tolerant)	**30-MHz crystal input**.
23	XO	O	OSC output	**30-MHz crystal output**.
26	nEJECT	I	5V-tolerant Schmitt input	**Active LOW**. Media eject or remote wakeup requested. Tie to +3.3V if functionality is not used.
27	SYSIRQ	I	5V-tolerant Schmitt input	**Active HIGH**. USB interrupt request. Tie to GND if functionality is not used.
28	DRVPWRVLD	I	5V-tolerant Schmitt input	**Configurable polarity**. Device Presence Detect. This pin must not be allowed to float if functionality is not utilized.
29	ATAEN	I	5V-tolerant Schmitt input	**Active HIGH**. ATA interface enable. ‘1’ = normal ATA operation. ‘0’ = ATA interface pins three-stated and ATA interface logic halted.
30-32	GPIO[0:1], GPIO2_nHS	I/O	3.3V drive, 5V-tolerant, 6-mA I_{OL}, Schmitt input	**General purpose I/O pins**. The GPIO pins must be tied to GND if functionality is not utilized. If the hs_indicator config bit is set, the GPIO2_nHS pin will reflect the operating speed of the device: ‘1’ = full-speed operation. ‘0’ = high-speed operation.
33	SCANEN	I	5V tolerant input buffer	**Active HIGH**. ASIC test pin. This pin must be tied to GND during normal operation.
34	LOWPWR	O	three-state driver, 5V-tolerant, 6-mA I_{OL}	**Active HIGH**. USB suspend indicator. ‘0’ = Chip active. VBUS power up to 100 mA granted. ‘three-state’ = Chip suspend. VBUS system current limited to USB suspend mode value
35	nRESET	I	5V-tolerant Schmitt input	**Active LOW**. Asynchronous chip reset.
36	nATARST	O	3.3V drive, 5V-tolerant, 6-mA I_{OL}	**Active LOW**. ATA reset signal.
37, 38	TMC[1:2]	I	3.3V input	**Active HIGH**. ASIC test pins. These pins must be tied to GND during normal operation.
56, 54, 52, 49,46, 44, 42, 39, 41, 43, 45, 48, 51, 53, 55, 57	DD[0:15]	I/O	3.3V drive, 5V-tolerant, 6-mA I_{OL}, Schmitt input	**ATA data signals**.
58	DMARQ	I	5V tolerant Schmitt input	**ATA control signal**.
62	nDIOW	O	3.3V drive, 5V-tolerant, 6-mA I_{OL}	**ATA control signal**.

2.2 Pin Overview (continued)

Pin Number	Pin Name	Pin Direction	Pin Type	Pin Description
63	nDIOR	O	3.3V drive, 5V-tolerant, 6 mA I_{OL}	**ATA control signal**.
64	IORDY	I	5V-tolerant Schmitt input	**ATA control signal**.
65	ATAPUEN	O	3.3V drive, 5V-tolerant, 6 mA I_{OL}	**ATA IORDY pull-up connection**. For VBUS-powered systems.
66	nDMACK	O	3.3V drive, 5V-tolerant, 6 mA I_{OL}	**ATA control signal**.
67	ATAIRQ	I	5V-tolerant Schmitt input	**ATA interrupt request**.
70, 68, 71	DA[0:2]	O	3.3V drive, 5V-tolerant, 6 mA I_{OL}	**ATA address signals**.
72, 73	nCS[0:1]	O	3.3V drive, 5V-tolerant, 6 mA I_{OL}	**ATA chip select signals**.
74	nPWR500	O	three-state driver, 5V-tolerant, 6 mA I_{OL}	**Active LOW**. VBUS power granted indicator. '0' = VBUS power up to bMaxPower value 'three-state' = bMaxPower value not granted (if more than 100 mA)
75	SCL	O	three-state driver, 5V-tolerant, 6 mA I_{OL}	**I^2C-compatible clock**. This pin may be left as a no-connect pin if the I^2C-compatible interface is not utilized.
76	SDA_nIMODE	I/O	three-state driver, 5V-tolerant, 6 mA I_{OL}, Schmitt input	**I^2C-compatible address/data or nIMODE select**.
77	DISKRDY	I	5V-tolerant Schmitt input	**Configurable polarity**. Device ready.
78	VBUSPWRD	I	5V-tolerant Schmitt input	**Active HIGH**. Bus-powered operation select pin. '1' = Bus powered '0' = Self powered
79	VBUSPWRVLD	I	5V-tolerant Schmitt input	**Active HIGH**. Indicates that VBUS power is present.
1, 4, 10, 21, 47, 60	VSS		Power	**Digital ground**.
3, 17, 40, 59, 80	VDD25		Power	**2.5V digital supply**.
7, 24, 50, 61, 69	VDD33		Power	**3.3V digital supply**.
11	PVDD25		Power	**Analog 2.5V supply (PLL)**.
12,14,16	AVSS		Power	**Analog ground**.
13	RREF		Power	**PLL voltage reference**. Current source for 2.4k (1%) resistor connected to AVSS.
15	AVDD25		Power	**Analog 2.5V supply**.

2.3 Detailed Pin Descriptions

2.3.1 DP, DM

DP and DM are the high-speed USB signaling pins, and they should be tied to the D+ and D– pins of the USB connector. Because they operate at high frequencies, the USB signals require special consideration when designing the layout of the PCB. See section 12.0 for PCB layout guidelines.

2.3.2 RSDP, RSDM

RSDP and RSDM are the full-speed USB signaling pins, and they should be tied to the DP and DM pins through 39Ω resistors. RSDP and RSDM also function as current sinks for termination during high-speed operation.

2.3.3 TEST[0:3]

The test pins control the various test modes of the CY7C68310. Most test modes are reserved for ASIC fabrication, but the following table outlines the test modes available for device manufacturing environments. The test pins must be tied to GND for normal operation.

Table 2-1. CY7C68310 Test Modes

Test Mode	Description
0000	**Normal Mode**. This is the default mode of operation.
0001	**Reserved**.
0010	**Limbo Mode**. The CY7C68310 three-states all output pins during Limbo mode operation with the exception of the XO pin. The XO pin output cell does not have three-state control (always enabled), and must be disabled or disconnected by other means. To enter Limbo Mode, nRESET must be toggled after the Test pins are set to '0010'.
0011	**Input xnorTree Mode**. This mode tests the connectivity of all dedicated inputs and outputs. While in the Input xnorTree Mode of operation, all bi-directional pins are wired as chain outputs. The results of the connectivity procedure will be seen on all bidirectional pins. Chain Inputs (in order): VBUSPWRVLD, VBUSPWRD, DISKRDY, ATAIRQ, IORDY, DMARQ, nRESET, ATAEN, DRVPWRVLD, SYSIRQ, nEJECT Chain Outputs (in order): GPIO[2:0], DD[15:0], SDA_nIMODE.
0100	**Bi-di xnorTree Mode**. This mode test the connectivity of all bi-directional inputs. While in the Bi-di xnor Tree Mode of operation, all bi-directional pins are wired as inputs and become part of the xnor Tree chain. The results of the connectivity procedure will be seen on all output only pins. Chain Inputs: GPIO[0], GPIO[1], GPIO[2], DD[7], DD[8], DD[6], DD[0], DD[5], DD[10], DD[4], DD[11], DD[3], DD[12], DD[2], DD[13], DD[1], DD[14], DD[0], DD[15], SDA_nIMODE. Chain Outputs: nPWR500, nATARST, nDIOW, nDIOR, nDMACK, ATAPUEN, nCS[1:0], DA[2:0], LOWPWR, SCL
0101–1111	**Reserved**.

2.3.4 XI, XO

The CY7C68310 requires a 30-MHz signal to derive internal timing. Typically a 30-MHz (2.5V tolerant, parallel-resonant fundamental mode) crystal is used, but a 30-MHz (2.5V, 50% duty cycle) square wave from another source can also be used. If a crystal is used, connect the pins to XI and XO, and also through 20pF capacitors to GND. If an alternate clock source is used, apply it to XI and leave XO open.

2.3.5 nEJECT

The nEJECT input pin provides a means to communicate an Eject button push to the ATA/ATAPI device via event notification as well as a way to cause a USB Remote-wakeup. During normal operation, asserting nEJECT low for 10ms indicates that a media eject has been requested. If the CY7C68310 is in a suspend state, and if remote wakeup is enabled by the USB host, a state change on this pin will immediately cause the CY7C68310 to perform a USB remote wakeup event.

2.3.6 SYSIRQ

The SYS_IRQ pin provides a way for systems to request service from host software by use of the USB Interrupt pipe. If the CY7C68310 has no pending interrupt data to return, USB interrupt pipe data requests are NAKed. If pending data is available, CY7C68310 returns 16 bits of data indicating the state of the DISK_READY pin, the HS_MODE signal that indicates whether CY7C68310 is operating in high-speed or full-speed, the VBUSPWRD pin, the User-Defined values from bits [7:3] of address 0xE of the configuration space, and the GPIO Pins. The table below gives the bitmap for the data returned on the interrupt pipe, and the figure beneath it depicts the latching algorithm incorporated by CY7C68310.The table below gives the bitmap for the data returned on the interrupt pipe, and the and the figure beneath it depicts the latching algorithm incorporated by the CY7C68310.

Table 2-2. USB Interrupt Pipe Data Bitmap

USB Interrupt Data Byte 1								USB Interrupt Data Byte 0							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	DISKRDY	USB High Speed	VBUSPWRD	USER_DEF[4]	USER_DEF[3]	USER_DEF[2]	USER_DEF[1]	USER_DEF[0]	GPIO[2]	GPIO[1]	GPIO[0]

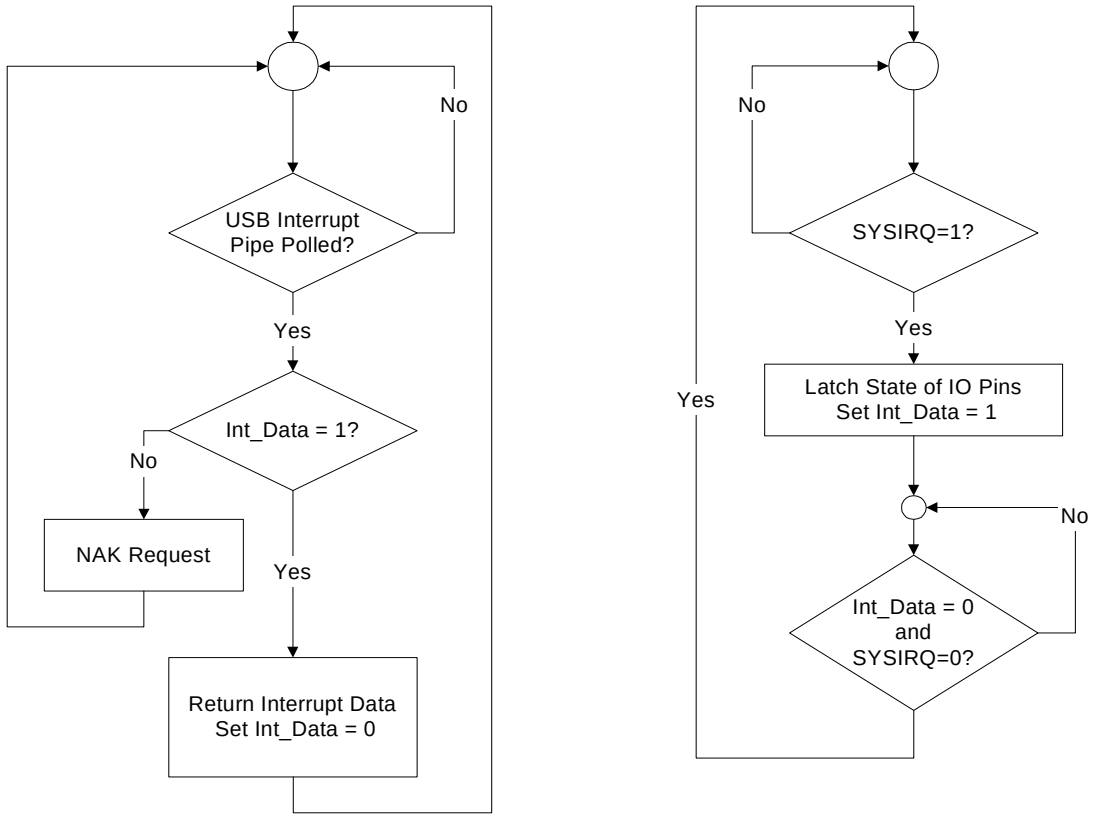


Figure 2-2. SYSIRQ Latching Algorithm

2.3.7 DRVPWRVLD

DRVPWRVLD can be used with removable devices (such as compact flash) to indicate that the media device is present. Pin polarity and function enable are controlled by bits 4 and 2, respectively, of EEPROM address 0x0B.

2.3.8 ATAEN

The ATAEN pin allows ATA bus sharing with other host devices. Asserting ATAEN low causes the CY7C68310 to three-state all ATA bus interface pins and suspend ATA state machine activity, otherwise leaving the CY7C68310 operational (USB operation continues). Asserting ATAEN high causes the CY7C68310 to reset the drive to state 0 and resume normal operation. To disable USB operation and the ATA interface, the DRVPWRVLD signal can be used in conjunction with ATAEN to force the CY7C68310 into a low power state until normal operation is resumed. Note that disabling the ATA bus with the ATAEN pin during the middle of a data transfer will result in data loss and may cause the operating system on the host computer to crash.

2.3.9 GPIO Pins

The GPIO pins allow for a general purpose Input/Output interface. Configuration bytes 0x0E and 0x0F contain the settings for the GPIO pins. See section 4.3 for details of how to use the vendor-specific commands to utilize the GPIO functionality. The status of the GPIO pins is also returned by a USB interrupt event. See section 2.3.6 for SYSIRQ details. Alternatively, If the hs_indicator config bit is set (bit 4 of EEPROM address 0x0F), the GPIO2_nHS pin will reflect the operating speed of the device.

2.3.10 LOWPWR

LOWPWR is an output pin that, when three-stated, indicates that the CY7C68310 is in a suspend state. When LOWPWR output is driven ‘0’, the CY7C68310 is active.

2.3.11 nRESET

Asserting nRESET for a minimum of 1ms after power rails are stable will reset the entire chip. An RC reset circuit should be used that ensures that no spurious resets occur.

2.3.12 ATAPUEN

This output provides control for the required host pull-up resistors on the ATA interface. ATAPUEN is driven ‘0’ when the ATA bus is inactive. ATAPUEN is driven ‘1’ when ATA bus is active. ATAPUEN is three-stated along with all other ATA interface pins when ATAEN is deasserted.

2.3.13 nPWR500

nPWR500 is an external pin that, when asserted low, indicates VBUS current may be drawn up to the limit specified by the appropriate bMaxPower field of the USB configuration descriptors. If the CY7C68310 enters a low-power state, nPWR500 is deasserted. When normal operation is resumed, nPWR500 is restored accordingly. The nPWR500 pin should never be used to control power sources for the CY7C68310.

2.3.14 SCL, SDA_nIMODE

If an external EEPROM device is used to store configuration information, the clock and data pins for the I^2C-compatible port should be connected to the configuration EEPROM and to VCC through 2.2kΩ resistors. If configuration information is to be obtained from the attached ATA/ATAPI device (IMODE), SCL should be left as a no-connect and SDA_nIMODE should be tied to GND.

2.3.15 DISKRDY

This input pin indicates the attached device is powered and ready to begin communication with the CY7C68310. DISKRDY qualifies the start of the CY7C68310 initialization sequence. A state change from ‘0’ to ‘1’ on DISKRDY will cause the CY7C68310 to wait for 25 ms before asserting nATARESET and re-initializing the device. The ATA interface state machines remain inactive and all of the ATA interface signals are driven logic '0' if DISKRDY is not asserted (assuming ATAEN = '1'). DISKRDY is filtered for 25 ms on the rising edge and cleared asynchronously on the falling edge.

2.3.16 VBUSPWRD

The VBUSPWRD input pin indicates whether the device will report itself as bus-powered or self-powered. Based upon the state of this pin at start-up, the CY7C68310 will request the current specified in the bMaxPower field of the appropriate USB Configuration Descriptor. If VBUSPWRD is asserted high, the CY&C68310 will report that the device is bus-powered. If VBUSPWRD is deasserted low, the CY7C68310 will report that the device is self-powered.

2.3.17 VBUSPWRVLD

VBUSPWRVLD (USB VBUS Power Valid) indicates that VBUS power is present at the USB connector. VBUSPWRVLD is asserted high and qualifies driving the system’s 1.5KΩ pull-up resistor on D+ (the USB specification only allows the device to source power to D+ when the host is powered). VBUSPWRVLD is conditioned so that it is only asserted after valid chip configuration bits have been loaded.

3.0 Functional Overview

3.1 USB Signaling Speeds

The CY7C68310 operates at two of the three signal rates that are defined in the Universal Serial Bus Specification Revision 2.0:

- Full speed, with a signaling bit rate of 12 Mbits/sec.
- High speed, with a signaling bit rate of 480 Mbits/sec.

3.2 ATA Interface

The ATA/ATAPI port on the CY7C68310 is compliant with the Information Technology–AT Attachment with Packet Interface–6 (ATA/ATAPI-6) Specification, T13/1410D Rev 2a. The CY7C68310 supports both ATAPI packet commands as well as ATA commands (by use of ATA Command Blocks). Refer to the USB Mass Storage Class (MSC) Bulk Only Transport Specification for information on Command Block formatting. Additionally, the CY7C68310 translates ATAPI SFF-8070i commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers. The CY7C68310 also provides a vendor-specific “event notify” ATA command to automatically communicate certain USB and system events to the attached device.

3.2.1 Vendor-specific EVENT_NOTIFY Command

The vendor-specific EVENT_NOTIFY command enables the CY7C68310 to communicate the occurrence of certain USB and system events to the attached device if the device's firmware supports the EVENT_NOTIFY command. The command code is specified by configuration address 0x02. Setting this byte to 0x00 disables the EVENT_NOTIFY feature.

Table 3-1. Notification Register Reads

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
LBA Low (Sector Number)	N/A							
LBA Mid (Cylinder Low)	nSTATE0							
LBA High (Cylinder High)	nSTATE1							
Device/Head	N/A							
Status	BUSY	N/A	N/A	N/A	DRQ	N/A	N/A	N/A

nSTATE0 and nSTATE1 are read from the device and stored for use as STATE0 and STATE1 during the next execution of the event notification command. nSTATE0 and nSTATE1 provide temporary non-volatile storage for devices whose power is controlled by NPWR500 (typically bus-powered systems). This allows the device to store information prior to entering a USB Suspend state for retrieval after resuming from the USB Suspend state. Note that a USB Reset from the host may interrupt the collection of data. The device must accommodate the potential for this occurrence. The BSY and DRQ bits must be cleared by the device upon the completion of an event notification command.

Table 3-2. Notification Register Write Values

Register	7	6	5	4	3	2	1	0
Features	USB Reset	Class Specific Reset	USB Suspend	USB Resume	Reserved	Reserved	Eject Button Pressed	Eject Button Released
Sector Count	Reserved	Reserved	Reserved	Reserved	Self-Powered	Bus-Powered	USB High-Speed	USB Full-Speed
LBA Low (Sector Number)	N/A							
LBA Mid (Cylinder Low)	STATE0							
LBA High (Cylinder High)	STATE1							
Device/Head	N/A							
Command	Specified in Configuration byte 0x02							

STATE0 and STATE1 are written with the value of NSTATE0 and NSTATE1 obtained from the previously completed event notification command. Assertion of NRESET resets STATE0 and STATE1to 0x00.

4.0 Configuration

Certain timing parameters and operational modes for the CY7C68310 are configurable. Some USB configuration and descriptor values are also configurable. CY7C68310 configuration data should not be confused with the USB Configuration Descriptor data.

4.1 CY7C68310 Configuration and USB Descriptor Sources

CY7C68310 configuration and USB descriptor data can be retrieved from three sources. *Table 4-1* indicates the method of determining which data source is used.

Table 4-1. CY7C68310 Configuration and USB Descriptor Sources

SDA_nIMODE = 0	I^2C-Compatible Device Present	I^2C Signature Check Passes	CY7C68310 Configuration and USB Descriptor Retrieval Method
No	No	N/A	In this mode, the CY7C68310 uses internal ROM contents for USB descriptor information and configuration register values. This mode is for debug/manufacturing operation only. Not for shipping products.
Yes	N/A	No	In this mode, the CY7C68310 uses internal ROM contents for USB descriptor information. Configuration register values are loaded from internal ROM. This is not a valid mode of operation.
Yes	N/A	Yes	The CY7C68310 retrieves all Descriptor and Configuration values from the vendor-specific Identify (FBh) data. The CY7C68310 is configured using internal ROM values until FBh data becomes available.
No	Yes	No	The CY7C68310 uses internal ROM contents for USB descriptor information. Configuration register values are loaded from internal ROM. In this mode of operation, any CY7C68310 vendor-specific configuration access causes the CY7C68310 to recheck the signature field. Once the signature check passes, SROM data is returned for USB descriptors requests. This is not a valid mode of operation.
No	Yes	Yes	The CY7C68310 retrieves all Descriptor and Configuration values from the I^2C-compatible memory device. The CY7C68310 is configured using these values.

4.1.1 I^2C-compatible Device

The CY7C68310 provides support for the 24LCXXB family of EEPROMs. Following the release of nRESET, the CY7C68310 waits 50 ms and then checks for I^2C-compatible device presence. If an I^2C-compatible device is present but does not pass signature check, the CY7C68310 re-tests the signature with each vendor-specific USB load or read access of configuration bytes 0 and 1. Once the signature check passes, I^2C-compatible data is returned for USB descriptor requests. If an I^2C-compatible device is detected initially, it is always assumed present until the next reset cycle (nRESET). If an I^2C-compatible device is present, a lack of an ACK response when required causes the CY7C68310 to stall that USB request. The CY7C68310 will attempt the access again with the next USB request.

4.1.2 IMode

Configuration and descriptor data can also be supplied by an attached mass storage device (IMODE) through a vendor-specific Identify (FBh) ATA command. The CY7C68310 provides 256 bytes of internal RAM for FBh data storage. Unlike operation with an external I2C-compatible memory device, IMODE operation requires the attached device first be initialized and FBh data retrieved before the CY7C68310 can allow USB enumeration. To meet USB specification requirements, IMODE operation must be limited to systems that draw 100 mA or less from VBUS prior to USB enumeration.

4.1.3 Internal ROM Contents

The CY7C68310 also contains an internal set of CY7C68310 configuration and USB descriptors. The internal descriptors may only be used during manufacturing, as the internal ROM values disable some features required for normal operation to aid use in a manufacturing environment. See *Table 4-2* for the organization of the internal ROM contents. The internal ROM descriptors do not provide a unique serial number (required for USB Mass Storage Class compliance), and therefore cannot be used for shipping products. An external I^2C-compatible memory device or utilization of the vendor-specific FBh identify command is required to correctly configure the CY7C68310 for operation and provide a unique serial number for MSC compliance.

4.2 EEPROM Organization

CY7C68310 configuration and USB descriptor data can be supplied from an I^2C-compatible serial memory device. The CY7C68310 can address 2 Kbytes of I^2C-compatible data, but CY7C68310 configuration and USB descriptor information are limited to 512 bytes maximum. Unused register space in the I^2C-compatible serial memory device may be used for product specific data storage. Note that no descriptor is allowed to span multiple pages within the I^2C-compatible serial memory device.

Table 4-2. EEPROM Organization

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
CY7C68310 Configuration Data				
0x00	I^2C memory device Signature (LSB)	LSB I^2C memory device Signature byte. Register does not exist in HW.	0x4B	
0x01	I^2C memory device Signature (MSB)	MSB I^2C memory device Signature byte. Register does not exist in HW.	0x50	
0x02	Event Notification	Bits (7:0) ATAPI event notification command. Setting this field to 0x00 disables this feature.		0x00
0x03	APM Value	Bits (7:0) ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the Initialization state machines will issue a SET FEATURES command to Enable APM with the register value during the drive initialization.		0x00
0x04	ATA Initialization Timeout	Time in 128-millisecond granularity before the CY7C68310 stops polling the ALT STAT register for reset complete and restarts the reset process (0x80 = 16.4 seconds).		0x80
0x05	USB Bus Mode	Bit (7) – read-only.		0x00
		USB bus mode of operation		
		'0' = USB bus is operating in full-speed mode (12 Mbit/sec).		
		'1' = USB bus is operating in high-speed mode (480 Mbit/sec).		
	ATAPI Command Block Size	Bit (6)		
		CBW Command Block Size.		
		'0' = 12 byte ATAPI CB		
		'1' = 16 byte ATAPI CB		
0x05	Master/Slave Selection	Bit (5)		
		Device number selection. This bit is valid only when "Skip ATA/ATAPI Device Initialization" is active. Under CY7C68310 control ("Skip ATA/ATAPI Device Initialization = '0'), the value is ignored.		
		'0' = Drive 0 (master)		
		'1' = Drive 1 (slave)		
	ATAPI Reset	Bit (4)		
		ATAPI reset during drive initialization.		
		Setting this bit enables the ATAPI reset algorithm in the drive initialization state machines.		
	ATA_NATAPI	Bit (3) – read only.		
		Indicates if an ATA or ATAPI device is detected.		
		'0' = ATAPI device		
		'1' = ATA device or possible device initialization failure.		
	Force USB FS	Bit(2)		
		Force USB full speed only operation.		
		Setting this bit prevents the CY7C68310 from negotiating HS operation during USB reset events		
		'0' = Normal operation – allow HS negotiation during USB reset		
		'1' = USB FS only – do not allow HS negotiation during USB reset		

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
	VS/MSC SOFT_RESET	Bit(1)		
		Vendor-specific/MSC SOFT_RESET control.		
		'0' = Vendor-specific USB command utilized for SOFT_RESET		
		'1' = Mass Storage Class USB command utilized for SOFT_RESET		
	DISKRDY Polarity	Bit (0)		
		DISKRDY active polarity. DISKRDY Polarity is ignored if IMODE is set to '1'. During IMODE operation DISKRDY polarity is active high.		
		'0' = Active high polarity		
		'1' = Active low polarity		
0x06	ATA Command Designator	Value in CBW CB field that designates if the CB is decoded as vendor-specific ATA/CFG commands instead of the ATAPI command block.		0x24
0x07	Reserved	Bits (7:1) – must be set to '0'		0x01
	Retry ATAPI	Bit (0)		
		This bit enables the CY7C68310 to accommodate ATAPI devices that take longer to initialize than what is allowed in the ATA/ATAPI-6 specification.		
		'1' = Retry ATAPI '0' = Normal ATAPI timing		
0x08	Initialization Status	Bit (7) – read only		0x00
		Drive Initialization Status		
		If set, indicates the drive initialization sequence state machine is active.		
	Force ATA Device	Bit (6)		
		Allows software to manually enable ATA Translation with devices that do not support CY7C68310 device initialization algorithms. Force ATA Device must be set to '1' in conjunction with Skip ATA/ATAPI Device Initialization and ATA Translation Enable.		
	Skip ATA/ATAPI Device Initialization	Bit (5)		
		Skip_Init – This bit should be cleared for IMODE operation. The host driver must initialize the attached device (if required) when this bit is set. For ATAPI devices, the host driver must issue an IDENTIFY command utilizing ATA.		
		'0' = normal operation		
		'1' = only reset the device and write the device control register prior to processing commands.		
	Reserved	Bit (4:3) – Must be set to '0'		
	Last LUN Identifier	Bits (2:0)		
		Maximum number of LUNs device supports.		
0x09	ATAEN	Bit (7) – read only.		0x01
		Current logic state of the ATAEN pin		
	Reserved	Bits (6:1) – Must be set to '0'		

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
	SRST Enable	Bit (0)		
		SRST reset during drive initialization. Setting this bit enables the SRST reset algorithm in the drive initialization state machines.		
0x0A	ATA Data Assert	Bits (7:4)		0x20
		Standard values for ATA-compliant devices and a 30.0-MHz system clock (in binary).[1]		
		mode 0 0101 (5+1)*33.33 = 200 ns		
		mode 1 0011 (3+1)*33.33 = 133 ns		
		mode 2 0011 (3+1)*33.33 = 133 ns		
		mode 3 0010 (2+1)*33.33 = 100 ns		
		mode 4 0010 (2+1)*33.33 = 100 ns		
	ATA Data Recover	Bits (3:0)		
		ATA cycle times are calculated using Data Assert and Data Recover values. Standard recover values and cycle times for ATA-compliant devices and a 30.0 MHz system clock (in binary).[1]		
		mode 0 1100 (4+1)+(12+1)*33.33 = 600 ns		
		mode 1 0111 (3+1)+(7+1)*33.33 = 400 ns		
		mode 2 0011 (2+1)+(3+1)*33.33 = 233 ns		
		mode 3 0010 (2+1)+(2+1)*33.33 = 200 ns		
		mode 4 0000 (2+1)+(0+1)*33.33 = 133 ns		
0x0B	ATA Data Set-up	Bits (7:5)		0x00
		Set-up time is only incurred on the first data cycle of a burst. Standard values for ATA-compliant devices and a 30.0 MHz system clock are (in binary).		
		mode 0 010 (2+1)*33.33 = 133 ns		
		mode 1 001 (1+1)*33.33 = 66 ns		
		mode 2 001 (1+1)*33.33 = 66 ns		
		mode 3 001 (1+1)*33.33 = 66 ns		
		mode 4 000 (0+1)*33.33 = 33 ns		
	Drive Power Valid Polarity	Bit (4)		
		Controls the polarity of DRVPWRVLD pin		
		‘0’ = Active low (“connector ground” indication)		
		‘1’ = Active high (power indication from device)		
	Override PIO Timing	Bit (3)		
		This field is used in conjunction with ATA Data Set-up, ATA Data Assertion, ATA Data Recover, and PIO Mode Selection fields.		
		‘0’ = Use timing information acquired from the Drive		
		‘1’ = Override device timing information with configuration values		

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
	Drive Power Valid Enable	Bit (2)		
		Enable for the DRVPWRVLD pin. Drive Power Valid should only be enabled in cable applications where the CY7C68310 is VBUS powered.		
		'0' = pin disabled (most systems)		
		'1' = pin enabled		
	ATA Read Kludge	Bit(1)		
		PIO data read three-state control. Enabling this will three-state the ATA data bus during PIO read operations while addressing the data register. In most applications this bit is set to '0.'		
		'0' = Normal operation as per ATA/ATAPI interface specification.		
		'1' = three-state DD[15:0] during PIO data register reads.		
	IMODE	Bit (0) – read only		
		This bit reflects the state of the IMODE input pin at start-up.		
0x0C	SYSIRQ	Bits(7) – read only		0x3C
		This bit reflects the current logic state of the SYSIRQ input.		
	DISKRDY	Bit(6) – read only		
		This bit reflects the current logic state of the DISKRDY input.		
	ATA Translation Enable	Bit(5)		
		Enable ATAPI to ATA protocol translation enable. If enabled, AND if an ATA device is detected, ATA translation is enabled. If Skip ATA/ATAPI Device Initialization is set '1,' Force ATA Device must also be set '1' in order to utilize ATA translation.		
		'0' = ATA Translation Disabled		
		'1' = ATA Translation Enable		
	ATA UDMA Enable	Bit(4)		
		Enable Ultra Mode data transfer support for ATA devices. If enabled, AND the ATA device reports UDMA support, the CY7C68310 will utilize UDMA data transfers.		
		'0' = Disable ATA device UDMA support		
		'1' = Enable ATA device UDMA support		
	ATAPI UDMA Enable	Bit(3)		
		Enable Ultra Mode data transfer support for ATAPI devices. If enabled, AND the ATAPI device reports UDMA support, the CY7C68310 will utilize UDMA data transfers.		
		'0' = Disable ATAPI device UDMA support		
		'1' = Enable ATAPI device UDMA support		

Table 4-2. EEPROM Organization (continued)

I²C Address	Field Name	Field Description	Required I²C Data	Example I²C Data
	ROM UDMA Mode	Bits(2:0)		
		ROM UDMA Mode indicates the highest UDMA mode supported by the product. The CY7C68310 will utilize the lesser of ROM UDMA Mode or the highest mode supported by the device. UDMA read operation mode timing is controlled by the device.		
		mode 0 000 133.3 ns per 16-bit word write		
		mode 1 001 100 ns per 16-bit word write		
		mode 2 010 66.7 ns per 16-bit word write		
		mode 3 011 66.7 ns per 16-bit word write		
		mode 4 100 33.3 ns per 16-bit word write		
0x0D	PIO Mode Selection	Bits (7:5)		0x90
		PIO Mode Selection. The PIO mode reported back to the device if the Override PIO Timing configuration bit is set. This field represents the PIO mode of operation configured by the ATA Data Set-up, ATA Data Assertion, ATA Data Recover, and Override PIO Ti		
		mode 0 000		
		mode 1 001		
		mode 2 010		
		mode 3 011		
		mode 4 100		
	Skip Pin Reset	Bit (4)		
		Skip nATARST assertion. Setting this bit prevents the CY7C68310 from asserting nATARST during initialization of the ATA/ATAPI device. If this bit is set to ‘1’, SRST Enable (address 0x09, bit 0) must also be set to ‘1’.		
		‘0’ = Allow nATARST assertion		
		‘1’ = Disable nATARST assertion		
	Reserved	Bits (3:0) – must be set to ‘0’		
0x0E	Reserved	Bits (7:3)		0x00
	General Purpose IO	Bits(2:0)		
		GPIO[2:0] pin values		
		When the GPIO pins are configured as outputs, writing to these bits will set the logic value of the GPIO pins to ‘0’ or ‘1’.		
		Reading this address, regardless of whether the GPIO pins are set to input or output, returns the logic value from the GPIO pins.		
0x0F	ATAPI IRQ Disable	Bit (7)		0x07
		Disables the use of the ATAIRQ signal with ATAPI devices. ‘1’ = disabled		
	Reserved	Bit (6) – must be set to ‘0’.		
	Int Reason Disable	Bit (5) Setting to a ‘1’ causes CY7C68310 to ignore the contents of the interrupt reason register when talking to an ATAPI device.		

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
	HS Indicator Enable	Bit (4)		
		Enables GPIO2_nHS pin to indicate the current operating speed of the device.		
		'0' = normal GPIO operation.		
		'1' = high-speed indicator enable.		
	Reserved	Bit (3)		
		This bit must be set to '1'.		
	General Purpose IO three-state Control	Bits (2:0)		
		GPIO[2:0] three-state control.		
		'0' = Output enabled (GPIO pin is an output).		
		'1' = three-state (GPIO pin is an input).		
USB Device Descriptor				
0x10	bLength	Length of device descriptor in bytes.	0x12	
0x11	bDescriptor Type	Descriptor type for device descriptor.	0x01	
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00	
0x13	bcdUSB (MSB)		0x02	
0x14	bDeviceClass	Device class		0x00
0x15	bDeviceSubClass	Device subclass		0x00
0x16	bDeviceProtocol	Device protocol		0x00
0x17	bMaxPacketSize0	Maximum USB packet size supported.	0x40	
0x18	idVendor (LSB)	Vendor ID		0xB4
0x19	idVendor (MSB)			0x04
0x1A	idProduct (LSB)	Product ID		0x31
0x1B	idProduct (MSB)			0x68
0x1C	bcdDevice (LSB)	Device release number in BCD lsb (product release number)		0x00
0x1D	bcdDevice (MSB)	Device release number in BCD msb (silicon release number). This field entry is always returned from internal ROM contents, regardless of the descriptor source.		0x01
0x1E	iManufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.		0x49
0x1F	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.		0x5F
0x20	iSerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0 if the string does not exist. The USB Mass Storage Class Bulk Only Transport Specification requires a unique serial number.		0x73
0x21	bNumConfigurations	Number of configurations supported.	0x01	
USB Device Qualifier Descriptor				
0x22	bLength	Length of device descriptor in bytes.	0x0A	
0x23	bDescriptorType	Descriptor type.	0x06	
0x24	bcdUSB (LSB)	USB specification release number in BCD.		0x00
0x25	bcdUSB (MSB)			0x02
0x26	bDeviceClass	Device class.		0x00
0x27	bDeviceSubClass	Device subclass.		0x00

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
0x28	bDeviceProtocol	Device protocol.		0x00
0x29	bMaxPacketSize0	Maximum USB packet size supported	0x40	
0x2A	bNumConfigurations	Number of configurations supported.	0x01	
0x2B	bReserved	Reserved. Must be set to 0.	0x00	
USB Standard Configuration Descriptor (VBUSPWRD active)				
0x2C	bLength	Length of Configuration descriptor in bytes.	0x09	
0x2D	bDescriptorType	Descriptor type.	0x02	
0x2E	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27	
0x2F	bTotalLength (MSB)		0x00	
0x30	bNumInterfaces	Number of interfaces supported. The CY7C68310 only supports one interface.	0x01	
0x31	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02.	0x02	
0x32	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
0x33	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On board default 7 Reserved. Set to '1' '1' 6 Self powered '0' = Bus powered device 5 Remoter wake-up '0' 4:0 Reserved. Set to '0' '0'	0x80	
0x34	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e., 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9	
USB Other Speed Configuration Descriptor (VBUSPWRD active)				
0x35	bLength	Length of Configuration descriptor in bytes.	0x09	
0x36	bDescriptorType	Descriptor type.	0x07	
0x37	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27	
0x38	bTotalLength (MSB)		0x00	
0x39	bNumInterfaces	Number of interfaces supported. The CY7C68310 only supports one interface.	0x01	
0x3A	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02	
0x3B	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
0x3C	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On board default 7 Reserved. Set to '1' '1' 6 Self powered '0' = Bus powered device 5 Remoter wake-up '0' 4:0 Reserved. Set to '0' '0'	0x80	
0x3D	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e., 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9	
USB Interface Descriptor (High-speed)				
0x3E	bLength	Length of interface descriptor in bytes.	0x09	

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
0x3F	bDescriptorType	Descriptor type.	0x04	
0x40	bInterfaceNumber	Interface number.	0x00	
0x41	bAlternateSettings	Alternate settings	0x00	
0x42	bNumEndpoints	Number of endpoints	0x03	
0x43	bInterfaceClass	Interface class.		0x08
0x44	bInterfaceSubClass	Interface subclass.		0x06
0x45	bInterfaceProtocol	Interface protocol.		0x50
0x46	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.		0x00
USB Bulk Out Endpoint (High-speed)				
0x47	bLength	Length of this descriptor in bytes.	0x07	
0x48	bDescriptorType	Endpoint descriptor type.	0x05	
0x49	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x82	
0x4A	bmAttributes	This is a bulk endpoint.	0x02	
0x4B	wMaxPacketSize (LSB)	Max data transfer size.	0x00	
0x4C	wMaxPacketSize (MSB)		0x02	
0x4D	bInterval	High-speed interval for polling (max NAK rate).	0x01	
USB Bulk In Endpoint (High-speed)				
0x4E	bLength	Length of this descriptor in bytes.	0x07	
0x4F	bDescriptorType	Endpoint descriptor type.	0x05	
0x50	bEndpointAddress	This is an Out endpoint, endpoint number 2.	0x01	
0x51	bmAttributes	This is a bulk endpoint.	0x02	
0x52	wMaxPacketSize (LSB)	Max data transfer size.	0x00	
0x53	wMaxPacketSize (MSB)		0x02	
0x54	bInterval	High-speed interval for polling (max NAK rate).	0x01	
USB Interrupt Endpoint (High-speed)				
0x55	bLength	Length of this descriptor in bytes.	0x07	
0x56	bDescriptorType	Endpoint descriptor type.	0x05	
0x57	bEndpointAddress	This is an Out endpoint, endpoint number 3.	0x83	
0x58	bmAttributes	This is a bulk endpoint.	0x03	
0x59	wMaxPacketSize (LSB)	Max data transfer size.	0x02	
0x5A	wMaxPacketSize (MSB)		0x00	
0x5B	bInterval	High-speed interval for polling (max NAK rate).	0x0C	
0x5C	Reserved	Reserved.	0x00	
USB Interface Descriptor (Full-speed)				
0x5D	bLength	Length of interface descriptor in bytes.	0x09	
0x5E	bDescriptorType	Descriptor type.	0x04	
0x5F	bInterfaceNumber	Interface number.	0x00	
0x60	bAlternateSettings	Alternate settings	0x00	
0x61	bNumEndpoints	Number of endpoints	0x03	
0x62	bInterfaceClass	Interface class.		0x08
0x63	bInterfaceSubClass	Interface subclass.		0x06
0x64	bInterfaceProtocol	Interface protocol.		0x50

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
0x65	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.		0x00
USB Bulk Out Endpoint (Full-speed)				
0x66	bLength	Length of this descriptor in bytes.	0x07	
0x67	bDescriptorType	Endpoint descriptor type.	0x05	
0x68	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x82	
0x69	bmAttributes	This is a bulk endpoint.	0x02	
0x6A	wMaxPacketSize (LSB)	Max data transfer size.	0x40	
0x6B	wMaxPacketSize (MSB)		0x00	
0x6C	bInterval	High-speed interval for polling (max NAK rate). Does not apply to FS bulk endpoints, set to zero.	0x00	
USB Bulk In Endpoint (Full-speed)				
0x6D	bLength	Length of this descriptor in bytes.	0x07	
0x6E	bDescriptorType	Endpoint descriptor type.	0x05	
0x6F	bEndpointAddress	This is an Out endpoint, endpoint number 2.	0x01	
0x70	bmAttributes	This is a bulk endpoint.	0x02	
0x71	wMaxPacketSize (LSB)	Max data transfer size.	0x40	
0x72	wMaxPacketSize (MSB)		0x00	
0x73	bInterval	High-speed interval for polling (max NAK rate). Does not apply to FS bulk endpoints, set to zero.	0x00	
USB Interrupt Endpoint (Full-speed)				
0x74	bLength	Length of this descriptor in bytes.	0x07	
0x75	bDescriptorType	Endpoint descriptor type.	0x05	
0x76	bEndpointAddress	This is an Out endpoint, endpoint number 3.	0x83	
0x77	bmAttributes	This is a bulk endpoint.	0x03	
0x78	wMaxPacketSize (LSB)	Max data transfer size.	0x02	
0x79	wMaxPacketSize (MSB)		0x00	
0x7A	bInterval	High-speed interval for polling (max NAK rate).	0xFF	
0x7B	Reserved	Reserved.	0x00	
USB String Descriptor – Index 0 (LANGID)				
0x7C	bLength	LANGID descriptor length	0x04	
0x7D	bDescriptorType	Descriptor type	0x03	
0x7E	LANGID (lsb)	Language supported (0x0409 = US English)		0x09
0x7F	LANGID (msb)			0x04
USB Standard Configuration Descriptor (VBUSPWRD Inactive)				
0x80	bLength	Length of Configuration descriptor in bytes.	0x09	
0x81	bDescriptorType	Descriptor type.	0x02	
0x82	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27	
0x83	bTotalLength (MSB)		0x00	
0x84	bNumInterfaces	Number of interfaces supported. The CY7C68310 only supports one interface.	0x01	
0x85	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02	

Table 4-2. EEPROM Organization (continued)

I²C Address	Field Name	Field Description	Required I²C Data	Example I²C Data
0x86	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
0x87	BmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On board default 7 Reserved. Set to '1' '1' 6 Self powered. '1' = Self powered device 5 Remoter wake-up. '0' 4:0 Reserved. Set to '0' '0'	0xC0	
0x88	BMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e., 0x31 = 98 mA, 0xF9 = 498 mA).	0x31	
USB Other Speed Configuration Descriptor (VBUSPWRD inactive)				
0x89	bLength	Length of Configuration descriptor in bytes.	0x09	
0x8A	bDescriptorType	Descriptor type.	0x07	
0x8B	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27	
0x8C	bTotalLength (MSB)		0x00	
0x8D	bNumInterfaces	Number of interfaces supported. The CY7C68310 only supports one interface.	0x01	
0x8E	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02	
0x8F	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
0x90	BmAttributes	Device attributes for this configuration. Configuration characteristics:	0xC0	
		Bit Description On board default 7 Reserved. Set to '1' '1' 6 Self powered '1' = Self powered device 5 Remoter wake-up '0' 4:0 Reserved. Set to '0' '0'		
0x91	BMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0x31	
USB String Descriptor – Manufacturer				
0x92	bLength	String descriptor length in bytes.		0x2C
0x93	bDescriptorType	Descriptor type.	0x03	
0x94	bString	ASCII character.		0x43 ("C")
0x95	bString	(NUL)		0x00
0x96	bString	ASCII character.		0x79 ("y")
0x97	bString	(NUL)		0x00
0x98	bString	ASCII character.		0x70 ("p")
0x99	bString	(NUL)		0x00
0x9A	bString	ASCII character.		0x72 ("r")
0x9B	bString	(NUL)		0x00
0x9C	bString	ASCII character.		0x65 ("e")
0x9D	bString	(NUL)		0x00
0x9E	bString	ASCII character.		0x73 ("s")

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
0x9F	bString	(NUL)		0x00
0xA0	bString	ASCII character.		0x73 (“s”)
0xA1	bString	(NUL)		0x00
0xA2	bString	ASCII character.		0x20 (“ ”)
0xA3	bString	(NUL)		0x00
0xA4	bString	ASCII character.		0x53 (“S”)
0xA5	bString	(NUL)		0x00
0xA6	bString	ASCII character.		0x65 (“e”)
0xA7	bString	(NUL)		0x00
0xA8	bString	ASCII character.		0x6D (“m”)
0xA9	bString	(NUL)		0x00
0xAA	bString	ASCII character.		0x69 (“i”)
0xAB	bString	(NUL)		0x00
0xAC	bString	ASCII character.		0x63 (“c”)
0xAD	bString	(NUL)		0x00
0xAE	bString	ASCII character.		0x6F (“o”)
0xAF	bString	(NUL)		0x00
0xB0	bString	ASCII character.		0x6E (“n”)
0xB1	bString	(NUL)		0x00
0xB2	bString	ASCII character.		0x64 (“d”)
0x1B	bString	(NUL)		0x00
0xB4	bString	ASCII character.		0x75 (“u”)
0xB5	bString	(NUL)		0x00
0xB6	bString	ASCII character.		0x63 (“c”)
0xB7	bString	(NUL)		0x00
0xB8	bString	ASCII character.		0x74 (“t”)
0x1B	bString	(NUL)		0x00
0xBA	bString	ASCII character.		0x6F (“o”)
0xBB	bString	(NUL)		0x00
0xBC	bString	ASCII character.		0x72 (“r”)
0xBD	bString	(NUL)		0x00
USB String Descriptor – Product				
0xBE	bLength	String descriptor length in bytes.		0x2A
0xBF	bDescriptorType	Descriptor Type.		0x03
0xC0	bString	ASCII character.		0x55 (“U”)
0xC1	bString	(NUL)		0x00
0x1C	bString	ASCII character.		0x53 (“S”)
0xC3	bString	(NUL)		0x00
0xC4	bString	ASCII character.		0x52 (“B”)
0xC5	bString	(NUL)		0x00
0xC6	bString	ASCII character.		0x20 (“ ”)
0xC7	bString	(NUL)		0x00
0xC8	bString	ASCII character.		0x53 (“S”)

Table 4-2. EEPROM Organization (continued)

I^2C Address	Field Name	Field Description	Required I^2C Data	Example I^2C Data
0xC9	bString	(NUL)		0x00
0xCA	bString	ASCII character.		0x74 (“t”)
0xCB	bString	(NUL)		0x00
0xCC	bString	ASCII character.		0x6F (“o”)
0xCD	bString	(NUL)		0x00
0xCE	bString	ASCII character.		0x72 (“r”)
0xCF	bString	(NUL)		0x00
0xD0	bString	ASCII character.		0x61 (“a”)
0xD1	bString	(NUL)		0x00
0xD2	bString	ASCII character.		0x67 (“g”)
0xD3	bString	(NUL)		0x00
0xD4	bString	ASCII character.		0x65 (“e”)
0xD5	bString	(NUL)		0x00
0xD6	bString	ASCII character.		0x20 (“ ”)
0xD7	bString	(NUL)		0x00
0xD8	bString	ASCII character.		0x41 (“A”)
0xD9	bString	(NUL)		0x00
0xDA	bString	ASCII character.		0x64 (“d”)
0xDB	bString	(NUL)		0x00
0xDC	bString	ASCII character.		0x61 (“a”)
0xDD	bString	(NUL)		0x00
0xDE	bString	ASCII character.		0x70 (“p”)
0xDF	bString	(NUL)		0x00
0xE0	bString	ASCII character.		0x74 (“t”)
0xE1	bString	(NUL)		0x00
0xE2	bString	ASCII character.		0x65 (“e”)
0xE3	bString	(NUL)		0x00
0xE4	bString	ASCII character.		0x72 (“r”)
0xE5	bString	(NUL)		0x00
USB String Descriptor – Serial Number				
0xE6	bLength	String descriptor length in bytes.		0x1A
0xE7	bDescriptorType	Descriptor type.		0x03
0xE8	bString	Serial number byte #1		0xXX (?)
0xE9	bString	Serial number byte #2		0xXX (?)
0xEA	bString	Serial number byte #3		0xXX (?)
0xEB	bString	Serial number byte #4		0xXX (?)
0xEC	bString	Serial number byte #5		0xXX (?)
0xED	bString	Serial number byte #6		0xXX (?)
0xEE	bString	Serial number byte #7		0xXX (?)
0xEF	bString	Serial number byte #8		0xXX (?)
0xF0	bString	Serial number byte #9		0xXX (?)
0xF1	bString	Serial number byte #10		0xXX (?)
0xF2	bString	Serial number byte #11		0xXX (?)

Table 4-2. EEPROM Organization (continued)

I²C Address	Field Name	Field Description	Required I²C Data	Example I²C Data
0xF3	bString	Serial number byte #12		0xXX (?)
0xF4	bString	Serial number byte #13		0xXX (?)
0xF5	bString	Serial number byte #14		0xXX (?)
0xF6	bString	Serial number byte #15		0xXX (?)
0xF7	bString	Serial number byte #16		0xXX (?)
0xF8	bString	Serial number byte #17		0xXX (?)
0xF9	bString	Serial number byte #18		0xXX (?)
0xFA	bString	Serial number byte #19		0xXX (?)
0xFB	bString	Serial number byte #20		0xXX (?)
0xFC	bString	Serial number byte #21		0xXX (?)
0xFD	bString	Serial number byte #22		0xXX (?)
0xFE	bString	Serial number byte #23		0xXX (?)
0xFF	bString	Serial number byte #24		0xXX (?)

4.3 Programming the EEPROM

Programming of the I²C memory device can be accomplished using an external device programmer, CY7C68310 supported vendor-specific USB commands, or an in-system programmer such as a bed of nails. *Table 4-3* shows the format of the vendor-specific commands used to program the EEPROM via USB. Any vendor-specific USB write request to the Serial ROM device configuration space will simultaneously update internal configuration register values as well. If the I²C device is programmed without vendor specific USB commands, CY7C68310 must be synchronously reset (nRESET) before configuration data is reloaded.

Table 4-3. EEPROM-related Vendor-specific Question

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
LOAD_CONFIG_DATA	0x40	0x01	Data Destination	Starting Address	Data Length	Configuration Data
READ_CONFIG_DATA	0xC0	0x02	Data Source	Starting Address	Data Length	Configuration Data

The CY7C68310 supports a subset of the “slow mode” specification (100 KHz) required for 24LCXXB EEPROM family device support. Features such as “Multi-Master,” “Clock Synchronization” (the SCL pin is output only), “10-bit addressing,” and “CBUS device support” are not supported. Vendor-specific USB commands allow the CY7C68310 to address up to 2 Kbytes of data (although configuration/descriptor information is limited to 512 bytes of register space).

4.3.1 LOAD_CONFIG_DATA

This request enables configuration data writes to the data source specified by the wValue field. The wIndex field specifies the starting address and the wLength field denotes the data length in bytes.

Legal values for wValue are as follows:

- 0x0000 Configuration bytes, address range 0x2 – 0xF
- 0x0002 External I²C memory device.

Configuration byte writes must be constrained to addresses 0x2 through 0xF, as shown in *Table 4-2*. Attempts to write outside this address space will result in a STALL condition. Configuration byte writes only overwrite CY7C68310 Configuration Byte registers, the original data source remains unchanged (I²C-compatible memory device, FBh identify data, or internal ROM).

Single byte writes to the I²C-compatible memory devices can start at any address. Writes greater then a single byte must only start on eight-byte boundaries, meaning that the address value must be evenly divisible by eight. Writes to I²C-compatible memory devices must not cross 256-byte page boundaries, i.e., start and finish write addresses must have equal modulo 256 values. Write operations with beginning and end addresses that do not fall in the same 256-byte page will result in a STALL condition. Illegal values for wValue as well as attempts to write to an I²C-compatible memory device when none is connected will result in a STALL condition.

4.3.2 READ_CONFIG_DATA

This USB request allows data retrieval from the data source specified by the wValue field. Data is retrieved beginning at the address specified by the wIndex field. The wLength field denotes the length in bytes of data requested from the data source.

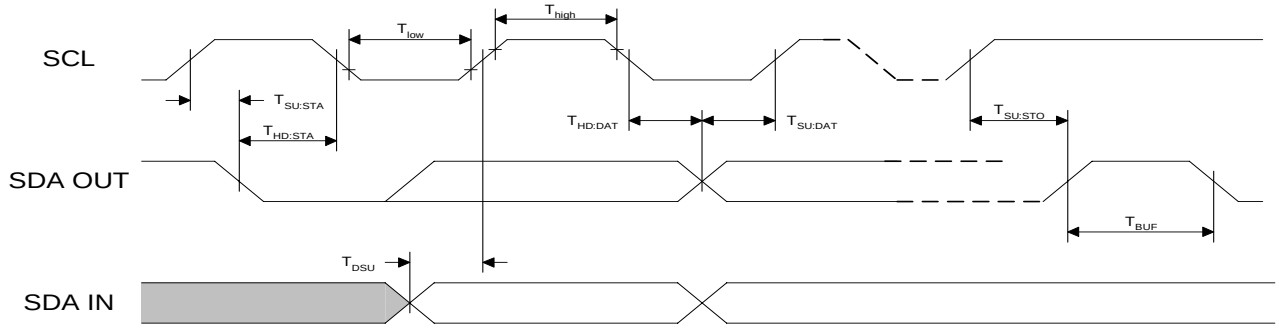
Legal values for wValue are as follows:

- 0x0000 Configuration bytes, addresses 0x0 – 0xF only
- 0x0001 Internal ROM
- 0x0002 External I^2C-compatible memory device
- 0x0003 Vendor-specific identify (FBh) data.

Illegal values for wValue will result in a STALL condition on the USB port. Attempted reads from an I^2C-compatible memory device when none is connected or attempted reads from FBh data when not in IMODE will result in a STALL condition. Attempts to read configuration bytes with starting addresses greater than 0xF will also result in a STALL condition.

5.0 Timing Characteristics

5.1 I^2C-compatible Memory Device Interface Timing



I^2C-compatible Device Parameter	Symbol	Value
Clock high time	T_{high}	5066 ns
Clock low time	T_{low}	5066 ns
Start condition hold time	$T_{HD:STA}$	5066 ns
Start condition set-up time	$T_{SU:STA}$	5066 ns
Data output hold time	$T_{HD:DAT}$	5066 ns
Data output set-up time	$T_{SU:DAT}$	5066 ns
Stop condition set-up time	$T_{SU:STO}$	5066 ns
Required data valid before clock	T_{DSU}	500 ns
Min time bus must be free before next transmission	T_{BUF}	5066 ns

Figure 5-1. I^2C Interface Timing

5.2 USB Interface Timing

The CY7C68310 transceiver complies to the timing characteristics as stated in the USB Specification version 2.0. The CY7C68310 can operate at either the high-speed or full-speed signalling rate.

5.3 ATA/ATAPI Interface Timing

The ATA interface supports ATA PIO modes 0 to 4, and Ultra DMA modes 0 to 4, per the ATA Attachment – 6 with Packet Interface revision 3b. All input signals on the ATA/ATAPI port are considered asynchronous and are synchronized to the chip's internal system clock. All output signals are clocked using the chip's internal system clock, for which there is no external reference. Thus, the output signals should also be considered asynchronous. The PIO mode used for data register accesses is retrieved from the device or specified in the CY7C68310 configuration bytes.

5.4 External Clock Source Timing

The CY7C68310 derives its internal system clock from an external clock source. The external clock input signal frequency is measured at ½ of the 2.5V power source (VDD25). The CY7C68310 internal PLL can be clocked using either a 30-MHz (±0.005%) fundamental-mode crystal or a 2.5V, 50% duty-cycle square wave. The recommended external clock source for the CY7C68310 is the PRE XH30PRF10BL crystal (10-pF load capacitance).

5.5 Reset Timing

The CY7C68310 requires an off-chip power-on reset circuit. nRESET must be held asserted for a minimum of 1 ms after power is stable to cause a chip reset.

6.0 External Circuitry Requirements

Certain external components are required for proper CY7C68310 operation. The following figure details the minimum required circuitry for normal operation. Additional components may be required to support configurable CY7C68310 features, if utilized.

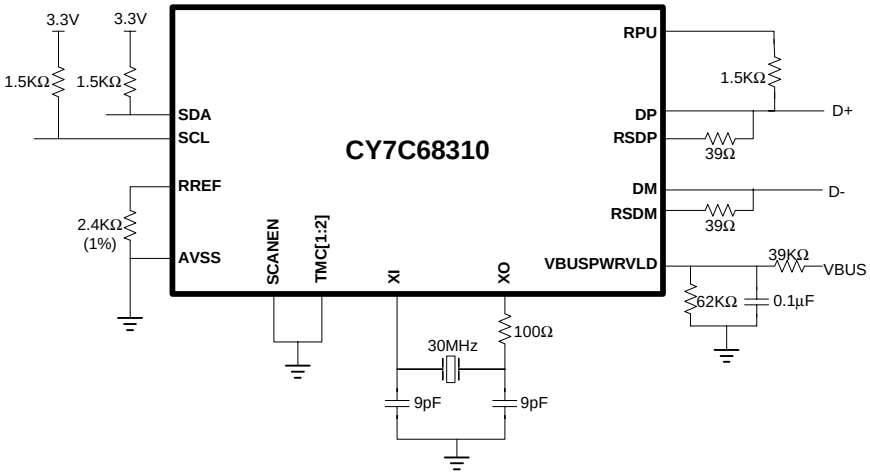


Figure 6-1. External Circuitry Requirements

6.1 ATA Interface Termination

Design practices as outlined in the ATA/ATAPI-6 specification for signal integrity should be followed with systems that utilize a ribbon cable interconnect between the CY7C68310's ATA interface and the attached ATA/ATAPI device, especially if Ultra DMA Mode is utilized.

6.2 Power Supply Regulation

At no time should the 3.3V power rail drop below the 2.5V rail for proper device operation. Care should be taken to ensure that the power rails rise and fall without allowing the 3.3V supply to drop below the 2.5V supply. The recommended method is to cascade voltage regulating circuits such that the 2.5V supply is powered from the 3.3V supply.

6.3 Pull-ups/Pull-downs on Three-stated Pins

Certain output pins act as open-drain and remain three-stated unless asserting a '0.' These pins include SCL, SDA, LOWPWR, and nPWR500. If their functionality is utilized, these pins must be tied to pull-up resistors to avoid floating while three-stated. These pins can be left as no-connects if the functionality is not utilized.

7.0 Manufacturing Interconnect Test Support

Manufacturing Test Mode is provided as a means to implement board- and system-level interconnect tests. During Manufacturing Test Mode operation, all outputs not associated directly with USB operation are controllable. Normal state machine and register control of output pins are disabled. Two vendor-specific USB requests (LOAD_MFG_DATA and READ_MFG_DATA) are used in Manufacturing Test Mode operation.

7.1 LOAD_MFG_DATA

This USB request is used to enable and control Manufacturing Test Mode operation. While in Manufacturing Test Mode, individual pins may be asserted or deasserted depending upon the contents of the data field. The DD and GPIO pins may also be three-stated in preparation for READ_MFG_DATA command operations. Control of the select CY7C68310 I/O pins and their three-state controls are mapped to the USB data packet associated with this request.

Table 7-1. LOAD_MFG_DATA Command Format

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
LOAD_MFG_DATA	0x40	0x05	Disable/Enable	Starting Address	Data Length	Mfg. Test Data

Legal values for wValue are as follows:

- 0x0000 Normal operation mode – returns CY7C68310 to normal operation regardless of previous command data sets (power-on reset default).
- 0x0001 Manufacturing Test Mode – manufacturing test registers control specific CY7C68310 outputs cells to enable board level testing in the manufacturing environment.

Legal values for wLength are as follows:

- 0x0000 Valid only when wValue = 0x0000; when disabling Manufacturing Test Mode of operation.
- 0x0007 Valid only when wValue = 0x0001. For proper Manufacturing Test Mode operation, wLength must equal 0x0007. Any data packet lengths greater than 7 will result in a STALL condition.

Table 7-2. Bit-wise Mapping of LOAD_MFG_DATA Test Data

Byte	Bit(s)	Test/Three-state Control Register Name
0	0	LOWPWR
0	1	Reserved – Value will not affect output
0	2	nPWR500
0	3	nATARST
0	4	nDIOW
0	5	nDIOR
0	6	nDMACK
0	7	ATAPUEN
1	0	Reserved – Value will not affect output
1	2:1	nCS[1:0]
1	5:3	DA[2:0]
1	6	SCL
1	7	DD_EN – ‘1’ = Enable output (set for writes), ‘0’ = three-state DD[15:0] (set for reads)
2	7:0	DD[7:0]
3	7:0	DD[15:8]
4	2:0	GPIO[2:0]
4	3	Reserved - Value will not affect output
4	6:4	GPIO_EN[2:0] – ‘1’ = Enable output (set for writes), ‘1’ = three-state GPIO[2:0] (set for reads)
4	7	Reserved – Value will not affect output
5	7:0	Reserved – Value will not affect output

7.2 READ_MFG_DATA

This USB request returns a “snapshot in time” of selected input pins. The input pin states are bit-wise mapped to the USB data packed associated with this request. CY7C68310 input pins not associated directly with USB operation can be sampled at any time during normal or Manufacturing Test Mode operation. This request is independent of normal CY7C68310 state machine control or Manufacturing Test Mode write operations.

Table 7-3. READ_MFG_DATA Command Format

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
READ_MFG_DATA	0xC0	0x06	0x00	0x00	Data Length	Mfg. Test Data

Legal values for wValue are as follows:

- 0x0000 wValue must be set to 0x0000.

Legal values for wLength are as follows:

- 0x0001–0x0008 Any wLength value greater than 0x0008 will result in a STALL response.

Table 7-4. Bit-wise Mapping of READ_MFG_Data Test Data

Byte	Bit(s)	Pin Name
0	0	DRVPWRVLD
0	1	VBUSPWRVLD
0	2	VBUSPWRD
0	3	DISKRDY
0	4	SYSIRQ
0	5	IORDY
0	6	DMARQ
0	7	nEJECT
1	0	ATAIRQ
1	1	Will always return ‘1’
1	2	LOWPWR
1	3	Reserved – Disregard value
1	4	nPWR500
1	5	nATARST
1	6	nDIOW
1	7	nDIOR
2	0	nDMACK
2	1	ATAPUEN
2	2	Reserved – Disregard value
2	4:3	nCS[1:0]
2	7:5	DA[2:0]
3	7:0	DD[7:0]
4	7:0	DD[15:8]
5	2:0	GPIO[2:0]
5	3	Will always return ‘0’
5	4	DD_EN
5	7:5	GPIO_EN[2:0]
6	0	MFG_SEL (manufacturing test mode enable)
6	1	ATAEN
6	2:7	Will always return ‘1’
7	7:0	Will always return ‘1’

8.0 Absolute Maximum Ratings

Storage Temperature ..... –65 to 150 °C
Ambient Temperature with power supplied ..... 0 to 70 °C
Supply Voltage to Ground Potential ..... –0.5 to 5.5 V
DC Input Voltage to Any Input Pin ..... –0.5 to 5.5 V
DC Voltage Applied to Outputs in three-state ..... –0.5 to 5.5 V
Power Dissipation ..... 235 mW
Static Discharge Voltage
ESD “HBM Model” tested to MIL-STD-883 Method 3015.7 ..... 2000 V
ESD “CDM Model” tested to ESDA STM5.3.1 ..... 250 V
Max Output Current per I/O port ..... 20 mA
Latch-up Current ..... > 200 mA

9.0 Operating Conditions

Operating temperature ..... 0 to 70°C

10.0 DC Characteristics

Parameter	Description		Min.	Typ.	Max.	Unit
V_{DD}	Digital voltage supply		2.25	2.50	2.75	V
V_{DDA}	Analog voltage supply		2.25	2.50	2.75	V
V_{DDIO}	I/O cell voltage supply		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0		V_{DDIO} + 0.5	V
V_{IL}	Input low voltage		–0.5		0.8	V
V_{OH}	Output high voltage at I_{OH}		2.4			V
V_{OL}	Output low voltage at I_{OL}				0.4	V
I_{OH}	Source current at V_{OH}		6			mA
I_{OL}	Sink current at V_{OL}		6			mA
I_{nCFG}	Unconfigured current	Full-speed		40		mA
		High-speed		60		mA
I_{CC}	Current in normal operation	Full-speed		65		mA
		High-speed		85		mA
I_{SUP}	Current in USB suspend (inactive, connected)			250		µA
I_{SLP}	Current in Sleep mode (inactive, unconnected)			<10		µA

11.0 Ordering Information

Part Number	Package Type
CY7C68310-80AC	80-lead TQFP
CY4617	CY7C68310 Mass Storage Reference Design Kit

12.0 PCB Layout Recommendations

The CY7C68310 contains high-speed analog circuitry that is sensitive to system noise. In particular, noise on both analog and digital power supplies must be minimized to ensure reliable, high-performance operation. Special attention should also be given to the design of the frequency generation, voltage reference, and USB interface circuits. Cypress recommends using the following guidelines in designing any product that uses the CY7C68310.

- The 3.3V power rail must remain above the 2.5V rail at all times for proper device operation.
- DP and DM trace lengths should be kept to within 2 mm of each other and must not exceed 37 mm in total length, with a preferred length of 20–30 mm.
- Maintain a solid ground plane under the DP and DM traces. Do not allow the plane to be split under these traces.
- Do not place vias on the DP or DM traces.
- Isolate the DP and DM traces from all other signal traces by no less than 10 mm.

- The DP and DM common mode trace impedance should be controlled to 45Ω with total differential impedance controlled to 90Ω (±10%).
- The VDD power plane should be as solid as possible with direct paths from the voltage regulator to all discrete components. A four layer board is required with inner layers dedicated to power and ground planes. Digital ground should cover one entire layer of the design.
- Analog and digital power planes must be isolated using inductors.
- Ceramic or tantalum capacitors are required. Do not use electrolytic capacitors. Electrolytic capacitors have higher lead inductance and series resistance values that have been observed to contribute to increased power supply noise.
- Adequate bypass capacitance must be implemented very near to the CY7C68310 power pins. One ceramic bypass capacitor per power/ground pair is recommended.
- All termination and pull-up resistors (including DP and DM) should be placed within 5 mm of the CY7C68310 pins.
- The crystal and RREF external resistor components should be placed as near the CY7C68310 pins as possible.

13.0 Package Diagram

80-lead Thin Plastic Quad Flat Pack (12 x 12 x 1.0 mm) A8012x12

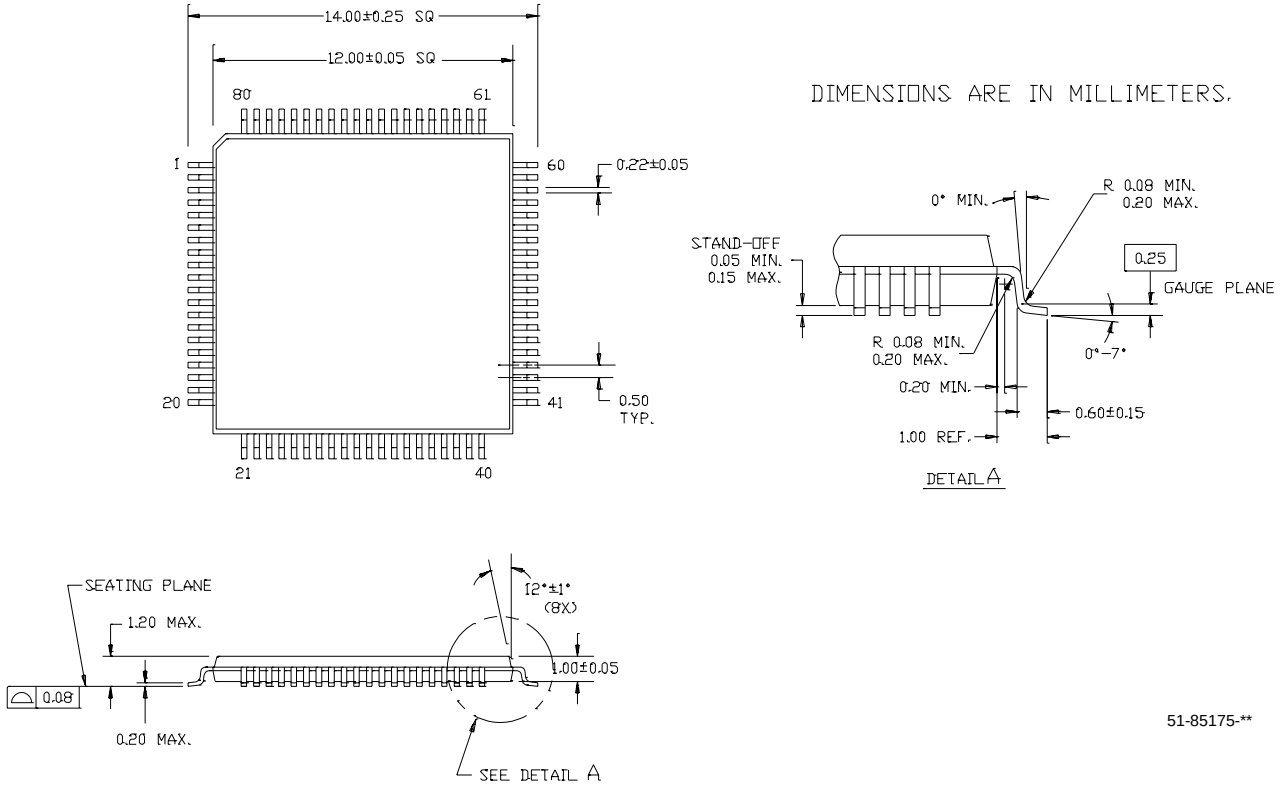


Figure 13-1. 80-pin TQFP Package Diagram

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Document History Page

Description Title: CY7C68310 ISD-300LP™ Low-Power USB 2.0 to ATA/ATAPI Bridge IC Document Number: 38-08030				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118297	09/18/02	BHA	New Data Sheet
*A	120307	12/12/02	GIR	Revised for Preliminary Status
*B	123509	04/04/03	GIR	Revised to include first silicon information
*C	126049	04/07/03	CVR	Post to External Website CY7C68310-80AC
*D	126323	05/21/03	GIR	Updated Suspend Current and included Sleep Mode in Section 10.0 Added ESD Testing Methodology and Power Dissipation values to Section 8.0 Revised for Final Status