WirelessUSB™ Radio

1.0 Features

The Cypress CYWUSB6941 WirelessUSB™ radio transceiver is designed to work with the Cypress CYWUSB6942 WirelessUSB baseband controller to provide a complete WirelessUSB solution. The CYWUSB6941 contains a 2.4-GHz radio transceiver, a GFSK modem, and a radio control interface that communicates with the CYWUSB6942.

- **Typically requires only ten external components for ease of implementation and manufacturing**
- **-10-dBm to 0-dBm transmit power for a transmission range of up to 10 meters**
- **-74-dBm receive sensitivity for dual antenna configurations, -70 dBm for single antenna**
- **AGC for enhanced interference immunity in high-density environments**
- **Provides low-power operating modes to conserve battery life**
- **2.7V to 3.6V operation**
- **7 x 5 x 1.2 mm 42-pin FBGA package**

1.1 Applications

The CYWUSB6941 is targeted for the following Human Input Device (HID) applications:

- Mice
- Keyboards
- Joysticks/Gamepads.

Block Diagram

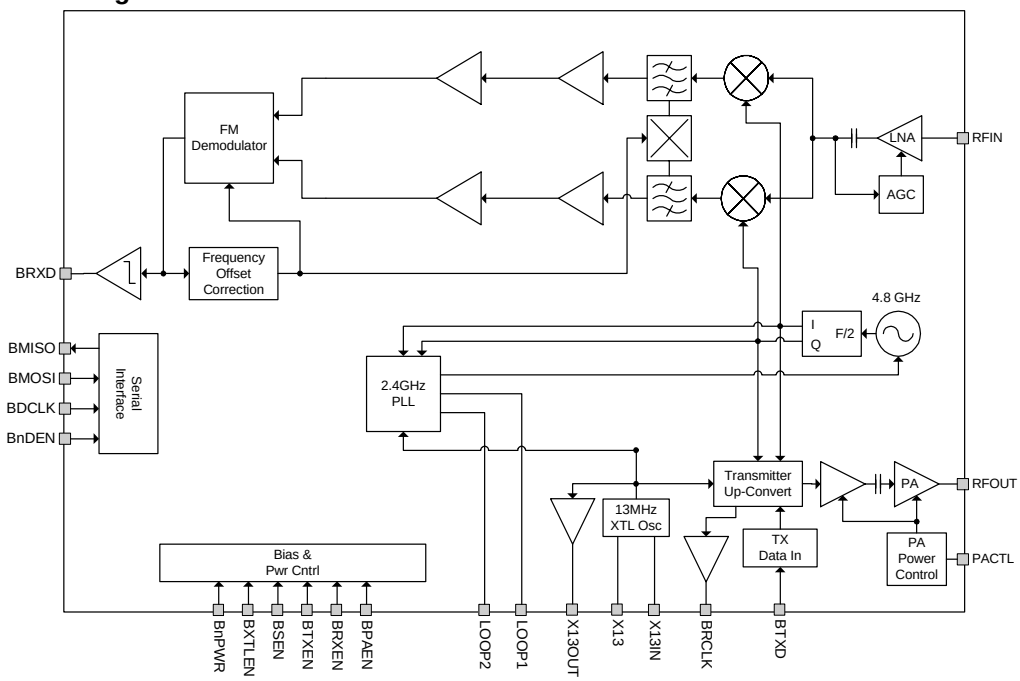

Figure 1-1. CYWUSB6941 Block Diagram

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2.0 Functional Overview

The Cypress CYWUSB6941 WirelessUSB transceiver is designed to work with the Cypress CYWUSB6942 WirelessUSB baseband controller to provide a complete WirelessUSB solution. The CYWUSB6941 contains a 2.4-GHz radio transceiver, a GFSK modem, and a radio control interface that communicates with the CYWUSB6942 WirelessUSB baseband. The CYWUSB6941 also facilitates the development of a complete WirelessUSB system with a minimum number of additional components, typically requiring only ten external components (including crystal and bandpass filter) for ease of implementation and manufacturing (refer to *Figure 2-1*), and only nine external components (no crystal is needed) if an external 13-MHz clock is available. Specific features include:

- **2.4-GHz frequency-hopping spread spectrum (FHSS) transceiver**
- **GFSK modulator/demodulator**
- **No external transmit/receive switch required**
  - Minimizes the need for external components
- **Closed-loop phase-locked loop (PLL)**
  - VCO is integrated in the CYWUSB6941
- **AGC circuitry**
  - Advanced AGC circuitry allows the CYWUSB6941's radio to operate more efficiently in high-node-density environments
- **Radio control interface**

2.1 2.4-GHz Radio Transceiver and GFSK Modem

The receiver is a low-IF architecture that uses RF and baseband AGC with fully integrated IF filters to achieve high performance in the presence of interference. The FM demodulator and fast data slicer are fully integrated.

The hop frequency synthesizer provides the frequency-hopping local oscillator for the transmitter and receiver. The only external components required are reference crystal, several capacitors, and a resistor. The RF VCO is fully integrated, requiring no external tank circuits.

The transmitter uses a DSP-based vector modulator to convert the transmit data to an accurate GFSK-modulated carrier. The maximum output power supports 0-dBm operation. There are a variety of DC power control features for transmitter, synthesizer, and receiver functions to optimize the average current drain.

2.2 Clocking

The CYWUSB6941 requires an external 13-MHz crystal with the following characteristics:

a. Maximum crystal series resistance: 100 Ohms

b. Crystal temperature stability: ± 15 ppm max.

c. Crystal load capacitance: 10 – 15 pF

The crystal has to be placed across the X13IN and X13 pins. No extra capacitors are needed.

To achieve the accuracy of 13 MHz ± 20 ppm, the crystal frequency has to be adjusted. There are two ways to adjust the crystal frequency:

1. through a trim capacitor placed in parallel to the crystal.
2. modifying the EPROM (.HEX image) location dedicated to the crystal adjustment. This is loaded in the external EPROM connected to the CYWUSB6942 baseband IC.

If an external 13-MHz clock is available, it can be provided to the CYWUSB6941 via the X13IN pin (refer to Section 3.0), eliminating the need for an external crystal. This will reduce the typical number of external components from ten to nine.

The external 13-MHz clock at X13IN must have a maximum rise/fall edge times of 2 ns, and the V_{IL}/V_{IH} needs to center at 2.0V in order to achieve a 50% duty cycle at X13OUT. The input capacitance for X13IN is 15 pF.

2.3 Application Examples

2.3.1 Application Example with the CYWUSB6942

Figure 2-1 shows an application example with external components.[1]

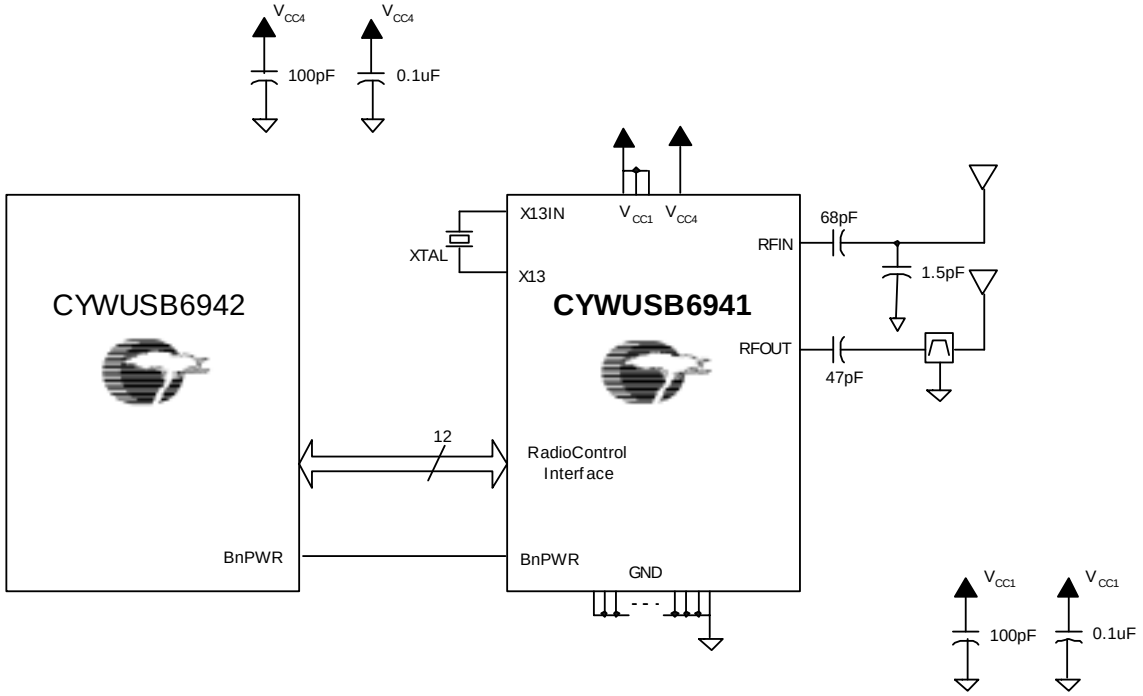

Figure 2-1. CYWUSB6941 Application Example with External Components

Note:

1. The matching network components between the RFIN, RFOUT, and bandpass filter are chosen based on the usage of a four-layer FR4 PCB with the following specifications:
   - Width between layer 1 (top component layer) and layer 2 (power plane) is 5.64 mils
   - Width between layer 2 (power plane) and layer 3 (power plane) is 47 mils
   - Width between layer 3 (power plane) and layer 4 (bottom trace layer) is 5.64 mils
   - Layers 1 and 4 (the top and bottom) are 1/2 oz. copper
   - Layers 2 and 3 (the inner power planes) are 1 oz. copper.

3.0 Pin Description

Table 3-1. Pin Description Table for the CYWUSB6941

Ball	Name	Type	Default	Description
RF Pins				
E1	RFIN	Input	N/A	**Antenna Input**. Modulated RF signal received.
F5	RFOUT	Output	N/A	**Antenna Output**. Modulated RF signal to be transmitted.
Filter/Crystal/Power Control Pins				
D7	X13	Input	N/A	**Crystal Differential Input**. Input for a differential crystal oscillator (refer to Section 2.2).
E7	X13IN	Input	N/A	**Crystal Differential Input/Clock Input**. Input for a differential crystal oscillator. This pin can also be connected to a 13-MHz CMOS output clock if available (refer to Section 2.2).
B7	X13OUT	Output		**System Clock**. Buffered 13-MHz system clock.
Radio Control Interface (Data Pins)				
A5	BTXD	Input		**Transmit Data**. Transmit data input port.
A6	BRXD	Output		**Receive Data**. Demodulated and sliced digital receive data.
Radio Control Interface (Control Pins)				
B5	BRCLK	Output		**Transmit Clock**. 1-MHz clock associated with the transmit data.
C5	BPAEN	Input		**Power Amplifier Enable**. Enables the PA in transmit mode. Active HIGH.
C6	BRXEN	Input		**Receive Circuitry Enable**. This signal enables the receive circuitry. Active HIGH.
B6	BTXEN	Input		**Transmit Circuitry Enable**. This signal enables the transmit circuitry. Active HIGH.
C4	BSEN	Input		**Synthesizer Enable**. This signal enables the hop synthesizer. Active HIGH.
A2	BnPWR	Input		**Power-on Reset**. This signal is active LOW.
D6	BXTLEN	Input		**Crystal Oscillator Enable**. This signal enables the crystal oscillator or the external 13-MHz clock, if provided. Active HIGH.
Serial Interface Pins				
A3	BMOSI	Input		**Input Data**. This is the serial data input pin.
B3	BMISO	Output		**Output Data**. This is the serial data output pin.
A4	BDCLK	Input		**Input Clock**. This is the serial register clock.
B4	BnDEN	Input		**Enable**. This signal enables the serial communication.
Power and Ground Pins				
B2	VCC1	V_{CC}	H	**V_{CC} pins for RF and analog baseband signals**.
D1	VCC2			
F6	VCC3			
E6	VCC4	V_{CC}	H	**V_{CC} pin for digital signals**.
A1	GND	GND	L	**Ground pins**.
A7				
C2				
C3				
C7				
D2				
D3				
D4				
E2				
E3				
E4				
E5				
F1				

Table 3-1. Pin Description Table for the CYWUSB6941 (continued)

Ball	Name	Type	Default	Description
F2	GND	GND	L	**Ground pins**.
F3				
F4				
F7	Reserved	GND	N/A	**Reserved pin.** Must be tied to GND.
B1	Reserved	GND	N/A	**Reserved pin.** Must be tied to GND.
C1	Reserved	GND	N/A	**Reserved pin.** Must be tied to GND.

	1	2	3	4	5	6	7	
A	**GND**	**BnPWR**	**BMOSI**	**BDCLK**	**BTXD**	**BRXD**	**GND**	A
B	**GND**	**VCC1**	**BMISO**	**BnDEN**	**BRCLK**	**BTXEN**	**X13OUT**	B
C	**GND**	**GND**	**GND**	**BSEN**	**BPAEN**	**BRXEN**	**GND**	C
D	**RFVCC2**	**GND**	**GND**	**GND**	**PACTL**	**BXTLEN**	**X13**	D
E	**RFIN**	**GND**	**GND**	**GND**	**GND**	**RFVCC4**	**X13IN**	E
F	**GND**	**GND**	**GND**	**GND**	**RFOUT**	**VCC3**	**GND**	F
	1	2	3	4	5	6	7	

Figure 3-1. CYWUSB6941 42-Ball FBGA Top View

4.0 Radio Control Interface

The CYWUSB6941 radio control interface is the communication interface between the CYWUSB6941 transceiver and the CYWUSB6942 WirelessUSB baseband. It consists of a data interface and a control interface for transmitting and receiving data, and a serial interface for programming the internal registers of the CYWUSB6941.

There are two subsections of the interface:

- RF data and control path
- Register control interface (serial).

Nine signals are used in the RF data and control path, four in the serial register control interface, and one system clock. All of the signals are unidirectional. Direction is oriented to/from the CYWUSB6941 RF IC.

4.1 Radio Control Interface Pin Description

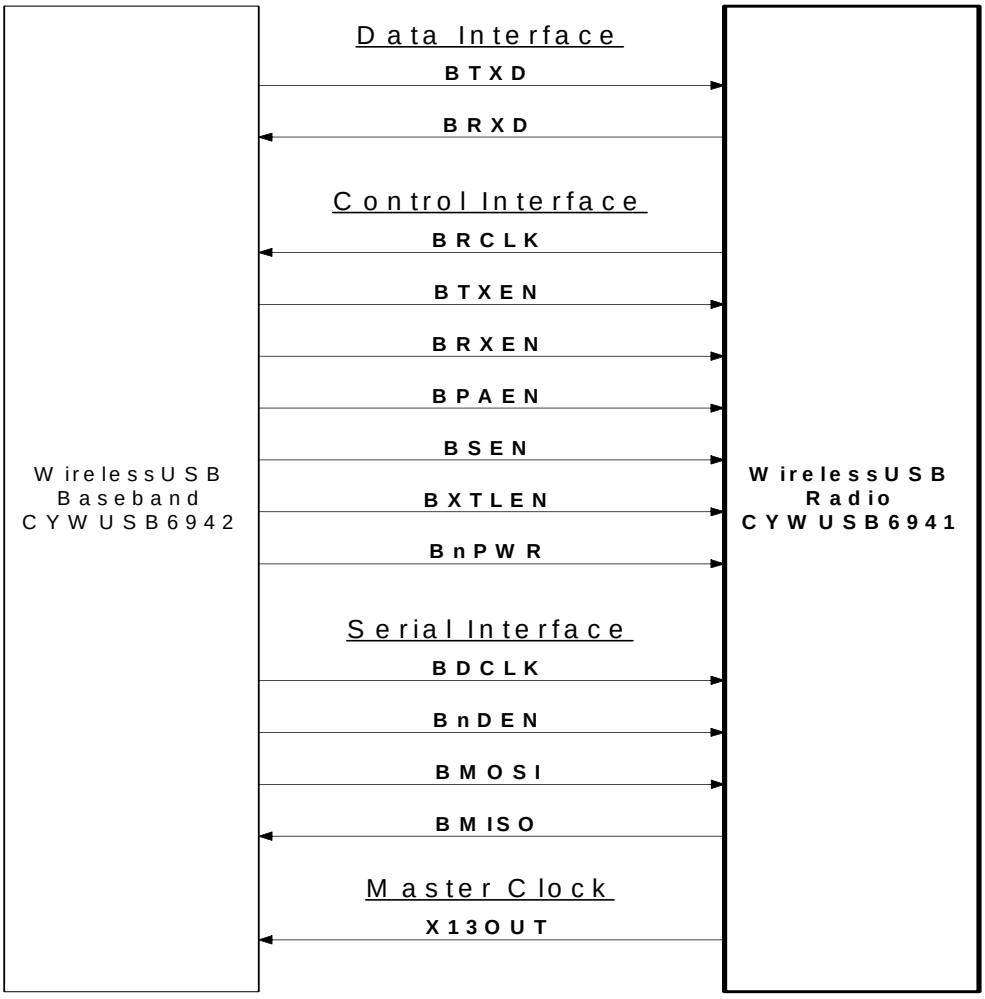

Figure 4-1. CYWUSB6941 Radio Control Interface Diagram

5.0 Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage on V_{CC} relative to V_{SS} ..... –0.3V to +3.9V

DC Input Voltage ..... –0.3V to V_{CC} +0.3V

DC Voltage applied to Outputs in High-Z State ..... –0.3V to V_{CC} +0.3V

Static Discharge Voltage (Digital)[2] ..... > 2001 V

Static Discharge Voltage (RF)[2] ..... > 501 V

Latch-up Current ..... +200 mA, –200 mA

6.0 Operating Conditions

V_{CC} (Supply Voltage) ..... 2.7V to 3.6V

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C

Ground Voltage 0V

F_{OSC} (Oscillator or Crystal Frequency) ..... 13 MHz ± 20 ppm

7.0 DC Characteristics (over the operating range)

Table 7-1. DC Parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	At I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	At I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$	–1		+1	µA
C_{IN}	Pin Input Capacitance (except X13, X13IN)				8	pF
C_{INX13}	Clock Pin Input Capacitance (X13, X13IN)				15	pF
I_{Sleep}	Current consumption during sleep mode	BXTLEN = 0		10		µA
I_{CC} (BXTLEN)	Current consumption when crystal oscillator is enabled and stable	BnPWR = 1		4	15	mA
I_{CC} (BSEN)	Current consumption when hop frequency synthesizer is enabled and stable	BXTLEN = 1		25	45	mA
I_{CC} (BRXEN)	Current consumption when receiver circuitry is enabled and stable	BXTLEN = 1 BSEN = 1		50	85	mA
I_{CC} (BTXEN)	Current consumption when transmit circuitry is enabled and stable	BXTLEN = 1 BSEN = 1		45	70	mA
I_{CC} (BPAEN)	Current consumption when transmit circuitry and PA are enabled and stable	BXTLEN = 1 BSEN = 1 BTXEN = 1		55	85	mA

Note:
2. Rating measured using the Human Body Model (HBM).

8.0 Radio Specification

Table 8-1. Radio Parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	RF Frequency Range		2.400			GHz
Radio Receiver (T = 25°C, V_{CC} = 3.3V)						
	Sensitivity (One antenna)	BER ≤ 10^{-3}		–72		dBm
	Sensitivity (Two antennas)	BER ≤ 10^{-3}		–78	–70	dBm
	Maximum Received Signal		–20	–12		dBm
	Interference Performance[3]	BER ≤ 10^{-3}				
	Co-channel Interference rejection Carrier-to-Interference (C/I)	C = –60 dBm		11		dB
	Adjacent (1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm		0		dB
	Adjacent (2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm		–30		dB
	Adjacent (≥ 3 MHz) channel selectivity C/I ≥ 3 MHz	C = –67 dBm		–40		dB
	Image Frequency Interference, C/I Image	C = –67 dBm		–20		dB
	Adjacent (1 MHz) interference to in-band image frequency, C/I image ±1 MHz	C = –67 dBm		–30		dB
	Out-of-Band Blocking Interference Signal Frequency[3]	BER ≤ 10^{-3}				
	30 MHz – 2000 MHz	C = –67 dBm		–30		dBm
	2000 MHz – 2399 MHz	C = –67 dBm		–30		dBm
	2498 MHz – 3000 MHz	C = –67 dBm		–27		dBm
	3000 MHz – 12.75 GHz	C = –67 dBm		–10		dBm
	Intermodulation	C = –64 dBm Δf = 5,10 MHz		–39		dBm
	Spurious Emission					
	30 MHz – 1 GHz				–57	dBm
	1 GHz – 12.75 GHz				–47	dBm
Radio Transmitter (T = 25°C, V_{CC} = 3.3V, PABias = 6)[4]						
	Maximum RF Transmit Power (One antenna)	Pwr setting = PA6	–10	–6	0	dBm
	RF Power Control Range			26		dB
	RF Power Range Control Step Size	6 steps, monotonic; 4.3 dB per step.		6		dB
	Frequency Deviation	101010 pattern		90		kHz
	Frequency Deviation	11110000 pattern		175		
	Zero Crossing Error			±125		ns
	Occupied Bandwidth	100-kHz resolution bandwidth, –20 dBc			±500	kHz
	Initial Frequency Offset			±75		kHz
	In-band Spurious					
	Second Channel Power (±2 MHz)				–20	dBm
	≥ Third Channel Power (≥3 MHz)				–40	dBm
	Non-harmonically Related Spurious					
	30 MHz – 12.75 GHz				–57	dBm
	Harmonic Spurious					
	2nd Harmonic				–26	dBm
	3rd Harmonic				–30	dBm
	4th Harmonic				–47	dBm

Notes:
3. Interference measurements are taken with the RFAGC disabled. Subharmonics of receive frequency excluded.
4. All radio-specific parameters are measured between the band-pass filter and the antenna on Cypress reference design.

9.0 AC Characteristics (over the operating range)

Table 9-1. AC Timing Parameters

Name	Description	Min.	Typ.	Max.	Unit
$t_{R/F}$	Rise and Fall Times			15	ns
t_{BPWR}	Pulse width for BnPWR for initiating a power-on-reset	100			ns
t_{BRCLK}	BRCLK period (duty cycle = 40/60)		1		µs
t_{BTXDSU}	Set-up time, data stable (on BTXD) before positive edge on BRCLK	164			ns
$t_{BTXDHLD}$	Hold time, data stable (on BTXD) after positive edge on BRCLK	0			ns
t_{BRXDPD}	Propagation delay of data from RFIN to serial data at BRXD		3		µs
t_{BXTLEN}[5]	Time from BXTLEN being driven HIGH to crystal oscillator becoming stable			10	ms
t_{BSEN}	Time from BSEN asserted to hop frequency synthesizer stable			250	µs
t_{TXRX}	Time from carrier on to first data transition	1.5		2.5	µs
t_{BPAEN}	Time from BTXD valid to PA off	0.5		2.5	µs
t_{BRXEN}	Time from BRXEN asserted to receiver circuitry stable for data reception	35			µs
t_{BPAOFF}	Time from last bit transmitted from the baseband to PA off	4			µs
t_{BTXOFF}	Time from BPAEN to BSEN and BTXEN off	1			µs
t_{BRXOFF}	Time from last bit received to BSEN, and BRXEN off			1	µs
t_{BXEN}	Time from BSEN	4			µs
Serial Interface Timing Parameters					
t_{BDCLK}	BDCLK period (max. 6.5 MHz)	154			ns
η	Duty cycle of BDCLK	40		60	%
t_{HLD}	Hold time, data stable after positive edge on BDCLK	20			ns
t_{SU}	Set-up time, data stable before positive edge on BDCLK	20			ns

Note:

5. This time depends on the crystal characteristics. Using a crystal with the specified parameters, the system will meet this timing specification when adjusted with an external capacitor (Xtal Cal set to zero), or when using the following procedure:
   - Start with Xtal cal set to zero
   - When the clock starts, immediately set the Xtal Cal bits to their correct final value
   - Before returning to “sleep” mode, reset Xtal Cal to zero.

9.1 Transmit and Receive Timing Diagrams

Transmit Timing Diagram

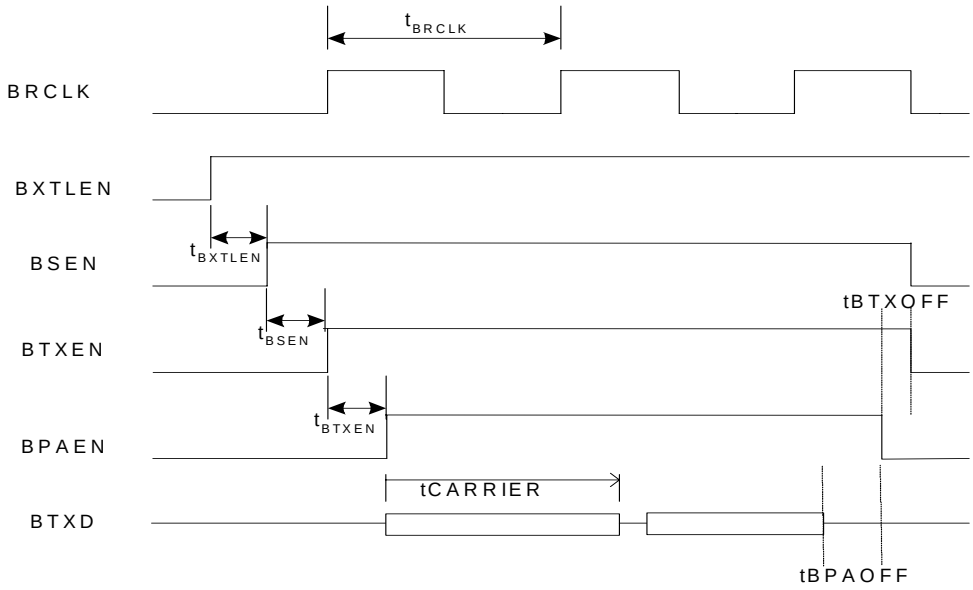

Figure 9-1. Transmit Timing Diagram

Receive Timing Diagram

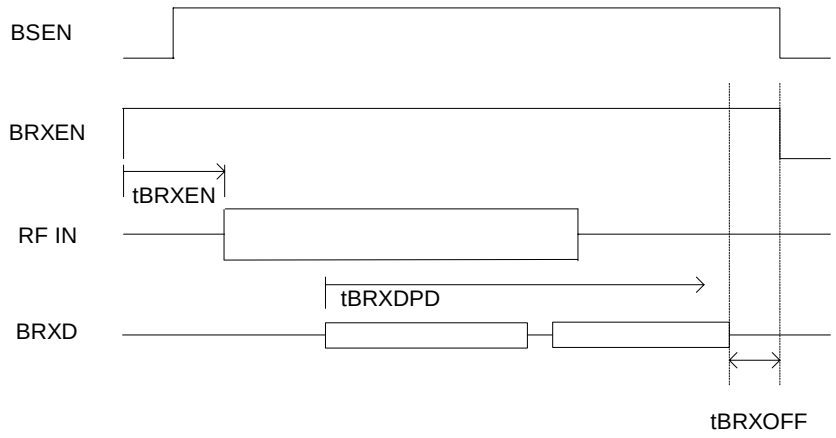

Figure 9-2. Receive Timing Diagram

9.2 Transmit Setup and Hold Times

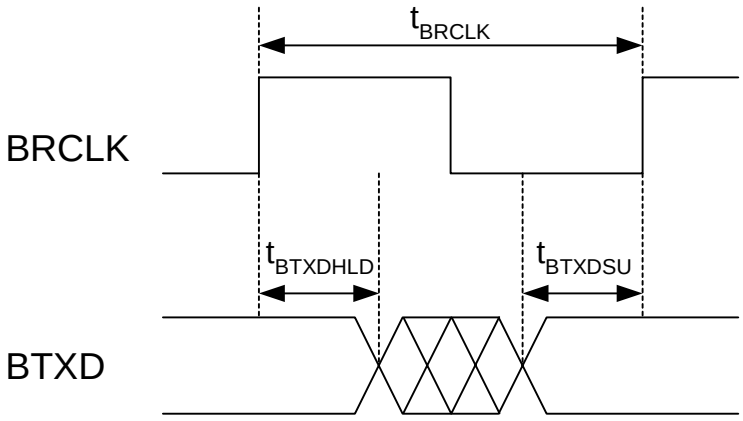

Figure 9-3. Transmit Set-up and Hold Times

9.3 Serial Interface Timing Diagram

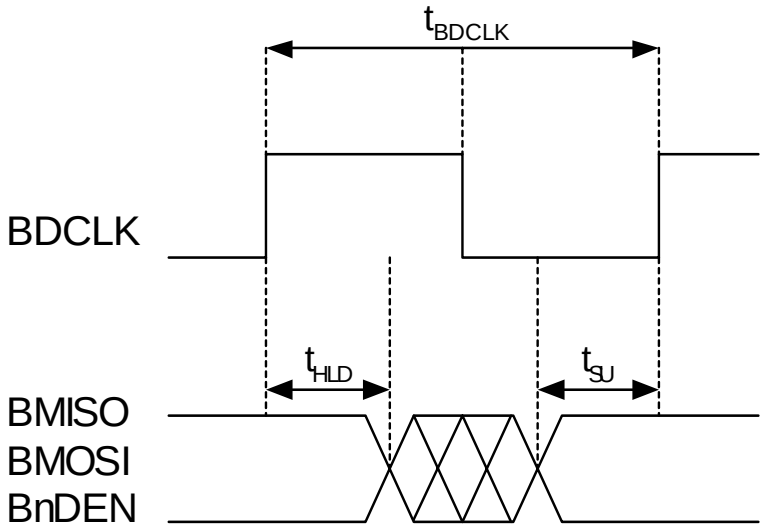

Figure 9-4. Timing Diagram

10.0 Ordering Information[6]

Table 10-1. Ordering Information

Part Number	Package Name	Package Type	Operating Range
CYWUSB6941-42BAC	42FBGA	42-ball Fine Ball Grid Array (7 x 5 x 1.2 mm)	Commercial

Note:
6. Companion part CYWUSB6942 is required for proper operation.

11.0 Package Description

The CYWUSB6941 comes in a 42-ball FBGA package with package size of 7 x 5 x 1.2 mm and a ball pitch of 0.75 mm. All dimensions are in millimeters (mm).

42-ball FBGA (7.0 x 5.0 x 1.2 mm) BA42

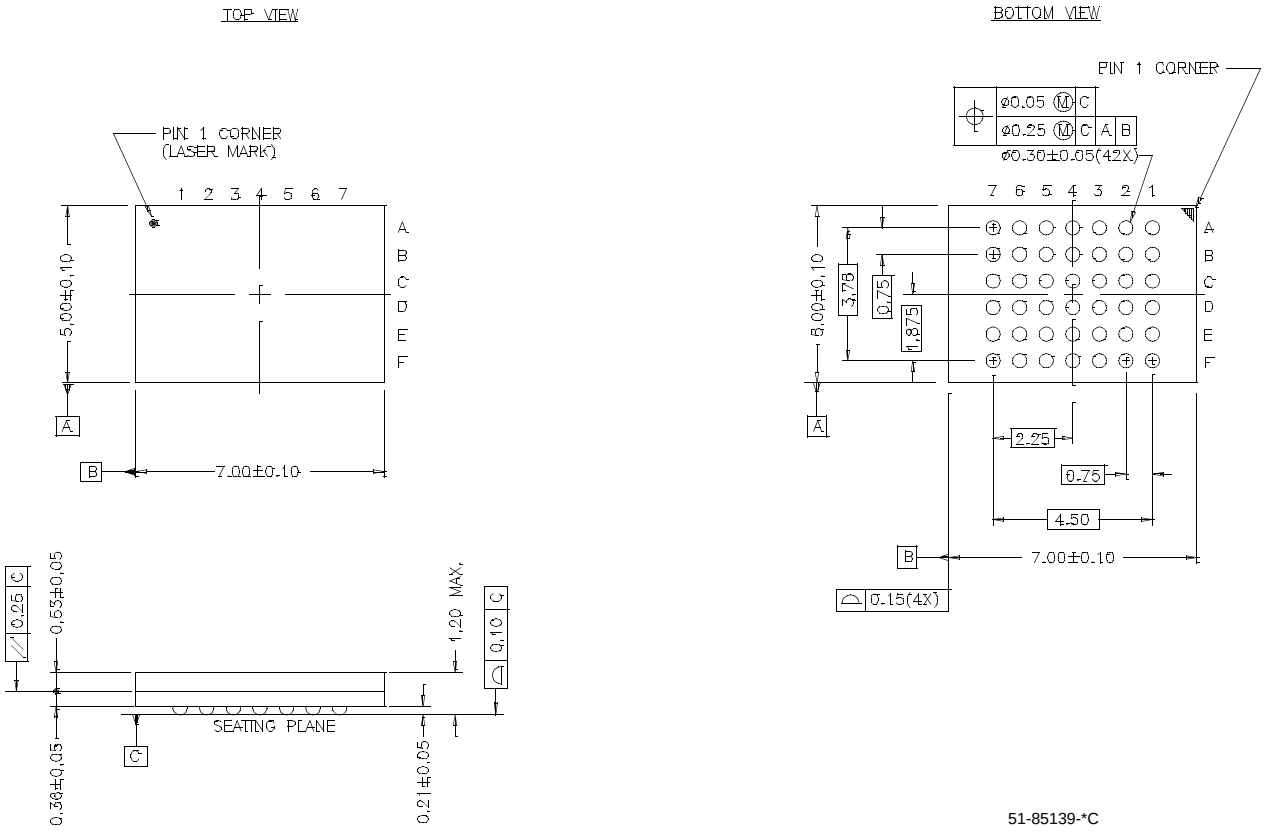

Figure 11-1. CYWUSB6941 Package Diagram

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