HA-5020/883

100MHz Current Feedback Video Amplifier with Disable

January 1996

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Wide Unity Gain Bandwidth . . . . 105MHz (Min)**
- **Slew Rate 800V/μs**
- **Output Current . . . . ±30mA (Min)**
- **Drives 3.5V into 75Ω**
- **Differential Gain 0.025%**
- **Differential Phase. . . . . 0.025 Deg**
- **Low Input Noise Voltage . . . . 4.5nV/√Hz**
- **Low Supply Current. . . . . 10mA (Max)**
- **Wide Supply Range . . . . ±5V to ±15V**
- **Output Enable/Disable**
- **High Performance Replacement for EL2020/883**

Applications

- **Unity Gain Video/Wideband Buffer**
- **Video Gain Block**
- **Video Distribution Amp/Coax Cable Driver**
- **Flash A/D Driver**
- **Waveform Generator Output Driver**
- **Current to Voltage Converter; D/A Output Buffer**
- **Radar Systems**
- **Imaging Systems**

Description

The HA-5020/883 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Intersil's Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020/883 offers better gain accuracy and lower distortion than open loop buffers.

The HA-5020/883 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020/883 are relatively independent of closed loop gain. The 105MHz unity gain bandwidth only decreases to 77MHz at a gain of 10. The HA-5020/883 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, the HA-5020/883 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

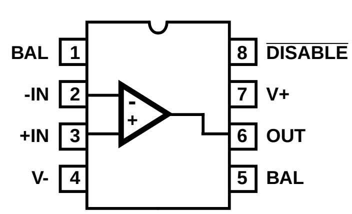
The HA-5020/883 offers significant enhancements over competing amplifiers, such as the EL2020. Improvements include unity gain bandwidth, slew rate, video performance, lower supply current, and superior DC specifications.

Ordering Information

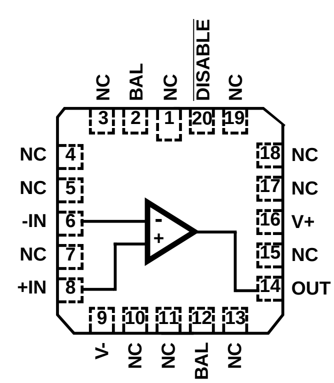
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA7-5020/883	-55^{o}C to +125^{o}C	8 Lead CerDIP
HA4-5020/883	-55^{o}C to +125^{o}C	20 Lead Ceramic LCC

Pinouts

HA-5020/883 (CERDIP)
TOP VIEW



HA-5020/883 (CLCC)
TOP VIEW



Spec Number **511080-883**
File Number **3541.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage. 8V
Voltage at Either Input Terminal . . . . V+ to V-
Peak Output Current. . . . . Full Short Circuit Protected
Junction Temperature (T_J) . . . . +175°C
Storage Temperature Range . . . . -65°C to +150°C
ESD Rating. . . . . < 2000V
Lead Temperature (Soldering 10s) . . . . +300°C

Thermal Information (Typical)

Thermal Package Characteristics — θ_{JA} / θ_{JC}
CerDIP Package . . . . 115°C/W 30°C/W
Ceramic LCC Package . . . . 75°C/W 23°C/W
Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
CerDIP Package 0.87W
Ceramic LCC Package 1.33W
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . 8.7mW/°C
Ceramic LCC Package . . . . 13.3mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . -55°C to +125°C
Operating Supply Voltage . . . . ±5V to ±15V
$V_{INCM} \leq$ 1/2(V+ - V-)
$R_L \geq$ 400Ω
R_F = 1kΩ
$V_{\overline{DISABLE}}$ = V+ or 0V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 0Ω, A_{VCL} = +1, R_F = 1kΩ, R_{LOAD} = 400Ω, V_{OUT} = 0V, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-8	8	mV
			2, 3	+125°C, -55°C	-10	10	mV
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V, V+ = 5V, V- = -25V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	50	-	dB
	-CMRR	ΔV_{CM} = -10V, V+ = 25V, V- = -5V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	50	-	dB
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 13.5V, V+ = 4.5V, V- = -15V; V+ = 18V, V- = -15V	1	+25°C	64	-	dB
			2, 3	+125°C, -55°C	60	-	dB
	-PSRR	ΔV_{SUP} = 13.5V, V+ = 15V, V- = -4.5V; V+ = 15V, V- = -18V	1	+25°C	64	-	dB
			2, 3	+125°C, -55°C	60	-	dB
Non-Inverting (+IN) Current	I_{BP}	V_{CM} = 0V	1	+25°C	-8	8	µA
			2, 3	+125°C, -55°C	-20	20	µA
+IN Common Mode Rejection	IBPCMP	ΔV_{CM} = +10V, V+ = 5V, V- = -25V	1	+25°C	-	0.1	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
	IBPCMN	ΔV_{CM} = -10V, V+ = 25V, V- = -5V	1	+25°C	-	0.1	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
Non-Inverting (+IN) Input Impedance	$+R_{IN}$	Calculated 1/IBPCMP	1	+25°C	10	-	MΩ
			2, 3	+125°C, -55°C	2	-	MΩ
+IN Power Supply Rejection	IBPPSP	ΔV_{SUP} = 13.5V, V+ = 4.5V, V- = -15V; V+ = 18V, V- = -15V	1	+25°C	-	0.06	µA/V
			2, 3	+125°C, -55°C	-	0.2	µA/V
	IBPPSN	ΔV_{SUP} = 13.5V, V+ = 15V, V- = -4.5V; V+ = 15V, V- = -18V	1	+25°C	-	0.06	µA/V
			2, 3	+125°C, -55°C	-	0.2	µA/V
Inverting Input (-IN) Current	I_{BN}	V_{CM} = 0V	1	+25°C	-20	20	µA
			2, 3	+125°C, -55°C	-50	50	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 0Ω, A_{VCL} = +1, R_F = 1kΩ, R_{LOAD} = 400Ω, V_{OUT} = 0V, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
-IN Common Mode Rejection	IBNCMP	ΔV_{CM} = +10V, V+ = 5V, V- = -25V	1	+25°C	-	0.4	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
	IBNCMN	ΔV_{CM} = -10V, V+ = 25V, V- = -5V	1	+25°C	-	0.4	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
-IN Power Supply Rejection	IBNPSP	ΔV_{SUP} = 13.5V, V+ = 4.5V, V- = -15V; V+ = 18V, V- = -15V	1	+25°C	-	0.2	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
	IBNPSN	ΔV_{SUP} = 13.5V, V+ = 15V, V- = -4.5V; V+ = 15V, V- = -18V	1	+25°C	-	0.2	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
Common Mode Range	+CMR	V+ = 5V, V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Transimpedance	$+A_{ZOL1}$	R_L = 400Ω, V_{OUT} = 0 to 10V	1	+25°C	1	-	MΩ
			2, 3	+125°C, -55°C	1	-	MΩ
	$-A_{ZOL1}$	R_L = 400Ω, V_{OUT} = 0 to -10V	1	+25°C	1	-	MΩ
			2, 3	+125°C, -55°C	1	-	MΩ
Output Voltage Swing	$+V_{OUT}$	V_{IN} = 12.8V	1, 2	+25°C, +125°C	12	-	V
			3	-55°C	11	-	V
	$-V_{OUT}$	V_{IN} = -12.8V	1, 2	+25°C, +125°C	-	-12	V
			3	-55°C	-	-11	V
	$+V_{OUT5}$	V+ = 5V, V- = -5V, V_{IN} = 3V	1	+25°C	2	-	V
			2, 3	+125°C, -55°C	2	-	V
	$-V_{OUT5}$	V+ = 5V, V- = -5V, V_{IN} = -3V	1	+25°C	-	-2	V
			2, 3	+125°C, -55°C	-	-2	V
Output Current	$+I_{OUT}$	Note 1	1, 2	+25°C, +125°C	30	-	mA
			3	-55°C	27.5	-	mA
	$-I_{OUT}$	Note 1	1, 2	+25°C, +125°C	-	-30	mA
			3	-55°C	-	-27.5	mA
Short Circuit Output Current	$+I_{SC}$	R_L = Open, V_{IN} = 10V	1	+25°C	50	-	mA
			2, 3	+125°C, -55°C	50	-	mA
	$-I_{SC}$	R_L = Open, V_{IN} = -10V	1	+25°C	-	-50	mA
			2, 3	+125°C, -55°C	-	-50	mA
Disabled Output Current	$+I_{LEAK}$	V_{IN} = 0V, V_{OUT} = +10V, R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	-1	1	µA
			3	-55°C	-1	1	µA
		V_{IN} = 2V	2	+125°C	-1	1	µA
	$-I_{LEAK}$	V_{IN} = 0V, V_{OUT} = -10V, R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	-1	1	µA
			3	-55°C	-1	1	µA
		V_{IN} = -2V	2	+125°C	-1	1	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 0Ω, A_{VCL} = +1, R_F = 1kΩ, R_{LOAD} = 400Ω, V_{OUT} = 0V, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Disable Pin Input Current	I_{LOGIC}	$V_{\overline{DIS}}$ = 0V	1, 2	+25^{o}C, +125^{o}C	-1	0	mA
			3	-55^{o}C	-1.5	0	mA
Minimum $\overline{DISABLE}$ Pin Current to Disable	I_{DIS}	Note 2	1	+25^{o}C	-	350	μA
			2, 3	+125^{o}C, -55^{o}C	-	350	μA
Maximum $\overline{DISABLE}$ Pin Current to Enable	I_{EN}	Note 3	1	+25^{o}C	20	-	μA
			2, 3	+125^{o}C, -55^{o}C	20	-	μA
Quiescent Power Supply Current	I_{CC}	R_L = 400Ω	1	+25^{o}C	-	10	mA
			2, 3	+125^{o}C, -55^{o}C	-	10	mA
	I_{EE}	R_L = 400Ω	1	+25^{o}C	-10	-	mA
			2, 3	+125^{o}C, -55^{o}C	-10	-	mA
Disabled Power Supply Current	I_{CCDIS}	R_L = 400Ω, $V_{\overline{DIS}}$ = 0V	1	+25^{o}C	-	5.6	mA
			2, 3	+125^{o}C, -55^{o}C	-	7.5	mA
	I_{EEDIS}	R_L = 400Ω, $V_{\overline{DIS}}$ = 0V	1	+25^{o}C	-5.6	-	mA
			2, 3	+125^{o}C, -55^{o}C	-7.5	-	mA
Offset Voltage Adjustment	$+V_{ADJ}$	Note 4	1	+25^{o}C	30	-	mV
			2, 3	+125^{o}C, -55^{o}C	25	-	mV
	$-V_{ADJ}$	Note 4	1	+25^{o}C	-	-30	mV
			2, 3	+125^{o}C, -55^{o}C	-	-25	mV

NOTES:

1. Guaranteed from V_{OUT} test by I_{OUT} = V_{OUT}/400Ω.
2. This is the minimum current which must be sourced from the $\overline{DISABLE}$ pin, to disable the output. The output is considered disabled when V_{OUT} ≤ 10mV. Conditions are: V_{IN} = 10V, R_L = 100Ω. The test is performed by sourcing 350μA from the $\overline{DISABLE}$ pin, and testing that the output decreases below the test limit (10mV).
3. This is the maximum current that can be sourced from the $\overline{DISABLE}$ pin with the device remaining enabled. The device is considered disabled when the supply current decreases by at least 0.5mA. Conditions are: R_L = 400Ω. Test is performed by sourcing 20μA from the $\overline{DISABLE}$ pin, and testing that the supply current decreases by no more than the test limit (0.5mA).
4. The offset adjustment range is referred to the output. The inverting input current ($-I_{BIAS}$) can be adjusted with an external pot between pins 1 and 5, wiper connected to V+. Since $-I_{BIAS}$ flows through R_F, an adjustment of offset voltage results. The amount of offset adjustment is proportional to the value of R_F. Test conditions are: R_L = Open, 10kΩ from pin 5 to V+, 1kΩ from pin 1 to V+, for $+V_{ADJ}$; R_L = Open, 1kΩ from pin 5 to V+, 10kΩ from pin 1 to V+, for $-V_{ADJ}$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 400Ω, C_{LOAD} ≤ 10pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{IN} = -10V to +10V	4	+25^{o}C	600	-	V/μs
			5, 6	+125^{o}C, -55^{o}C	400	-	V/μs
	-SR	V_{IN} = +10V to -10V	4	+25^{o}C	600	-	V/μs
			5, 6	+125^{o}C, -55^{o}C	400	-	V/μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 400Ω, R_F = 1kΩ, $V_{\overline{DISABLE}}$ = V+, C_{LOAD} ≤ 10pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
-3dB Bandwidth	BW_1	V_O = 100mV_{RMS}, A_V = +1	1	+25°C	105	-	MHz
	BW_{10}	V_O = 100mV_{RMS}, A_V = +10, R_F = 360Ω, R_L = Open	1	+25°C	77	-	MHz
Gain Flatness	GF_5	V_O = 100mV_{RMS}, f = 5MHz	1	+25°C	-0.075	+0.075	dB
	GF_{10}	V_O = 100mV_{RMS}, f = 10MHz	1	+25°C	-0.2	+0.2	dB
Rise Time	t_R	V_O = 0V to 1V, R_L = 100Ω	1, 2	+25°C	-	3.7	ns
Fall Time	t_F	V_O = 1V to 0V, R_L = 100Ω	1, 3	+25°C	-	4.0	ns
Overshoot	+OVS	V_O = 0V to 1V, R_L = 100Ω	1	+25°C	-	18.0	%
	-OVS	V_O = 1V to 0V, R_L = 100Ω	1	+25°C	-	16.6	%
Slew Rate	$+SR_{10}$	V_O = -10V to 10V, A_V = +10, R_F = 360Ω, R_L = Open	1, 4	+25°C	1070	-	V/µs
	$-SR_{10}$	V_O = 10V to -10V, A_V = +10, R_F = 360Ω, R_L = Open	1, 5	+25°C	860	-	V/µs
Disable Time	$+t_{DIS}$	V_O = 2V to 0V, 50% of $V_{\overline{DIS}}$ to 90% V_O	1, 6	+25°C	-	3.13	µs
	$-t_{DIS}$	V_O = -2V to 0V, 50% of $V_{\overline{DIS}}$ to 90% V_O	1, 6	+25°C	-	2.44	µs
Enable Time	$+t_{EN}$	V_O = 0V to 2V, 50% to 90%	1, 7	+25°C	-	1.45	µs
	$-t_{EN}$	V_O = 0V to -2V, 50% to 90%	1, 7	+25°C	-	1.49	µs

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Measured from 10% to 90% of the output waveform.
3. Measured from 90% to 10% of the output waveform.
4. Measured from 25% to 75% of the output waveform.
5. Measured from 75% to 25% of the output waveform.
6. $\overline{DISABLE}$ = +15V to 0V. Measured from the 50% of $\overline{DISABLE}$ to V_{OUT} = ±200mV.
7. $\overline{DISABLE}$ = 0V to +15V. Measured from the 50% of $\overline{DISABLE}$ to V_{OUT} = ±1.8V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
65 x 60 x 19 mils ± 1 mils
1640μm x 1520μm x 483μm ± 25.4μm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
5.77 x 10^4 A/cm^2 at 30mA

SUBSTRATE POTENTIAL (Powered Up): V-

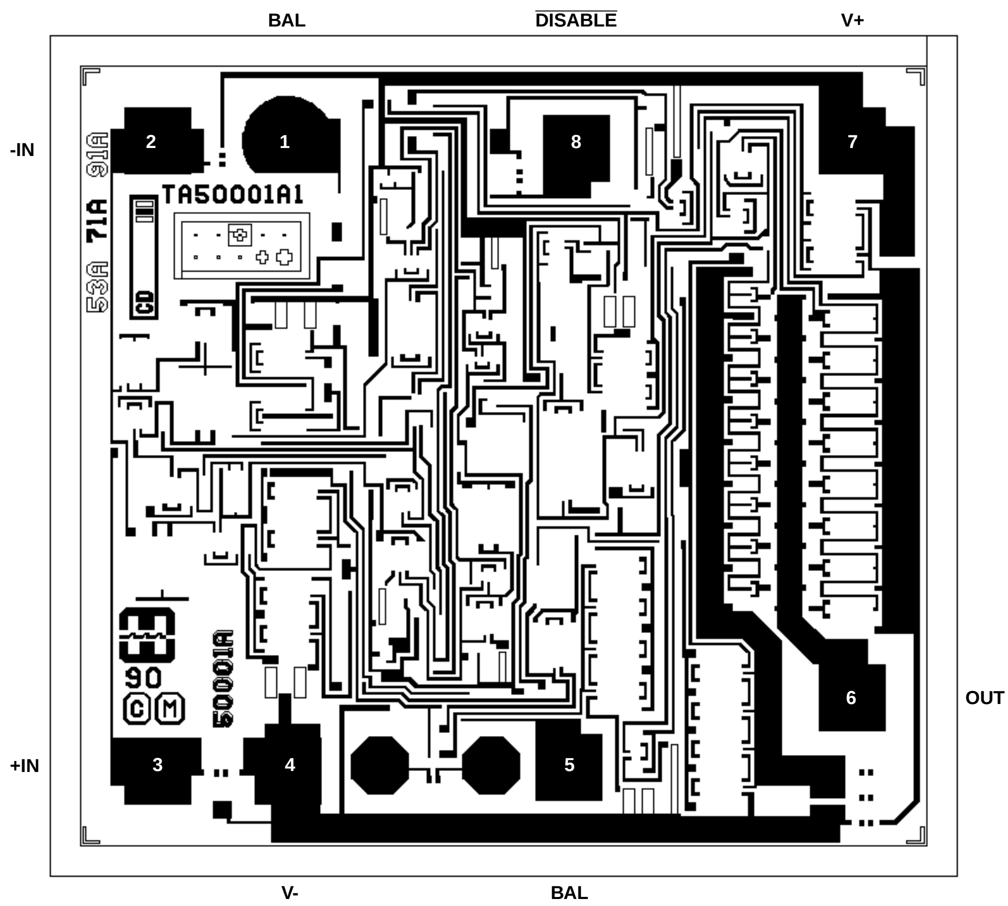
GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

TRANSISTOR COUNT: 62

PROCESS: Bipolar Dielectric Isolation

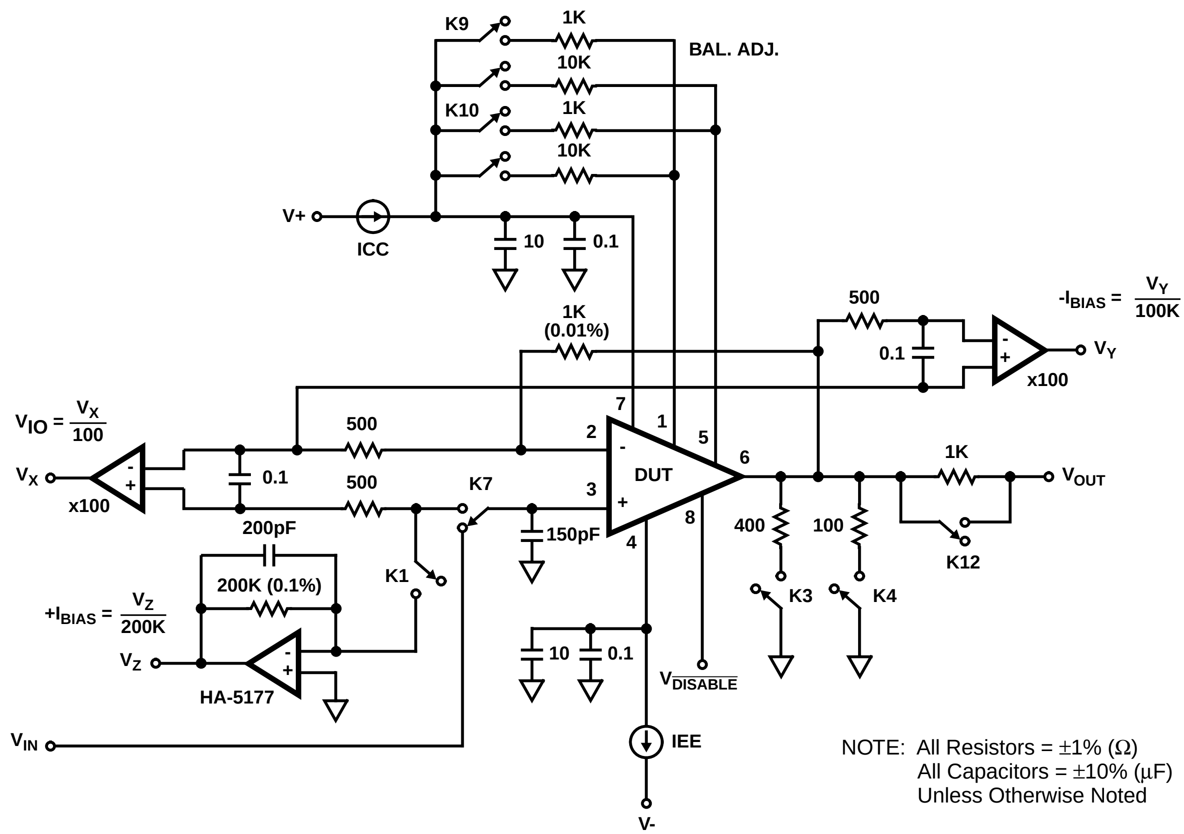
Metallization Mask Layout

HA-5020/883



Spec Number **511080-883**

Test Circuit (Applies to Table 1)

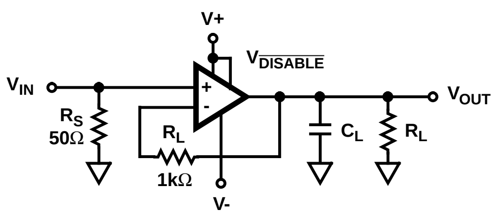


NOTE: All Resistors = ±1% (Ω)
All Capacitors = ±10% (μF)
Unless Otherwise Noted

Test Waveforms

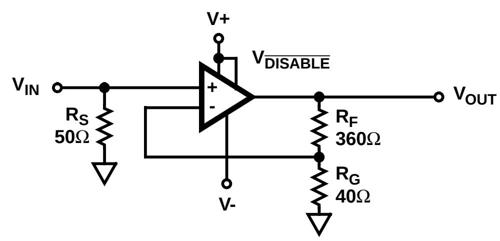
SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE (Applies to Tables 2 and 3)

A_V = +1 TEST CIRCUIT



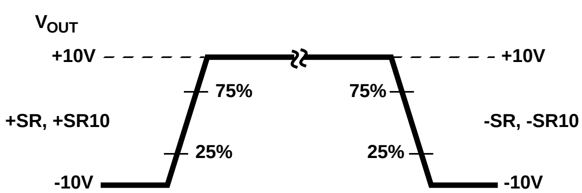
NOTE: V_S = ±15V, A_V = +1, C_L ≤ 10pF
R_F = 1kΩ, R_S = 50Ω
R_L = 400Ω For Large Signal
R_L = 100Ω For Small Signal

A_V = +10 TEST CIRCUIT

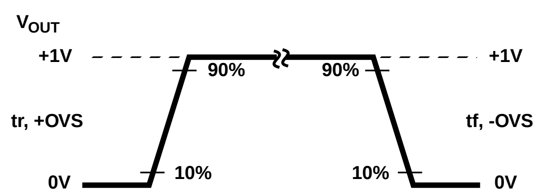


NOTE: V_S = ±15V, A_V = +10, C_L ≤ 10pF
R_F = 360Ω, R_G = 40Ω
R_S = 50Ω, R_L = Open

LARGE SIGNAL WAVEFORM



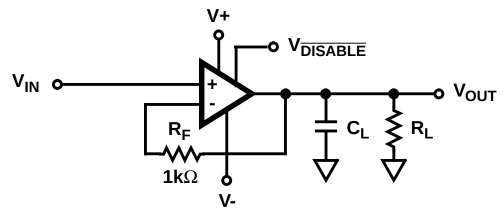
SMALL SIGNAL WAVEFORM



NOTE: A_V = +1: +SR, -SR
A_V = +10: +SR10, -SR10

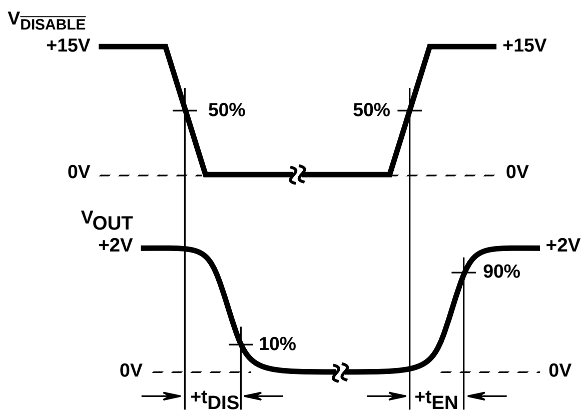
Test Waveforms (Continued)

SIMPLIFIED TEST CIRCUIT FOR ENABLE/DISABLE TIMES

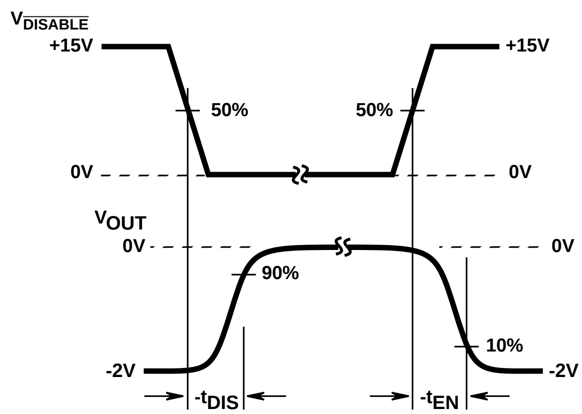


NOTE: V_S = ±15V, A_V = +1, C_L ≤ 10pF
R_F = 1kΩ, R_L = 400Ω

POSITIVE ENABLE/DISABLE SWITCHING WAVEFORMS

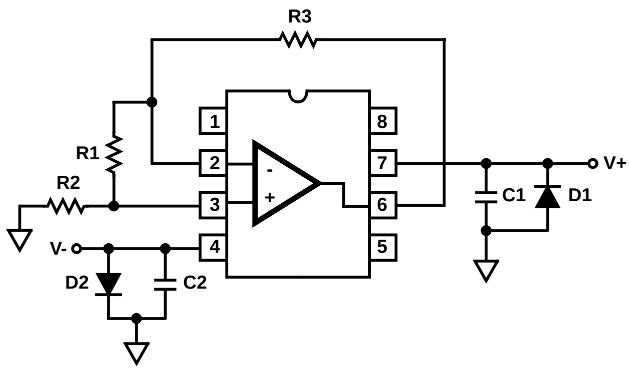


NEGATIVE ENABLE/DISABLE SWITCHING WAVEFORMS

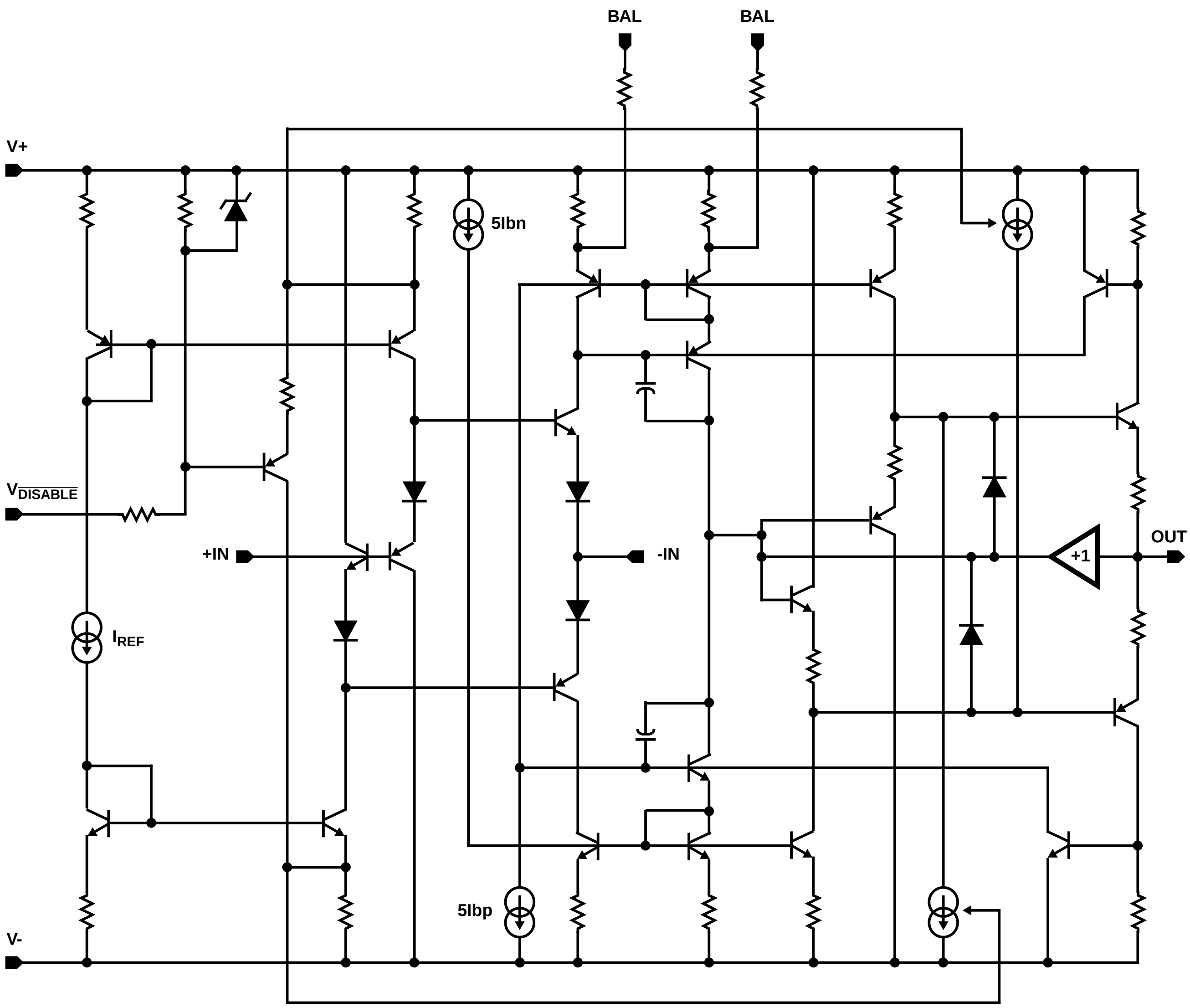


Burn-In Circuits

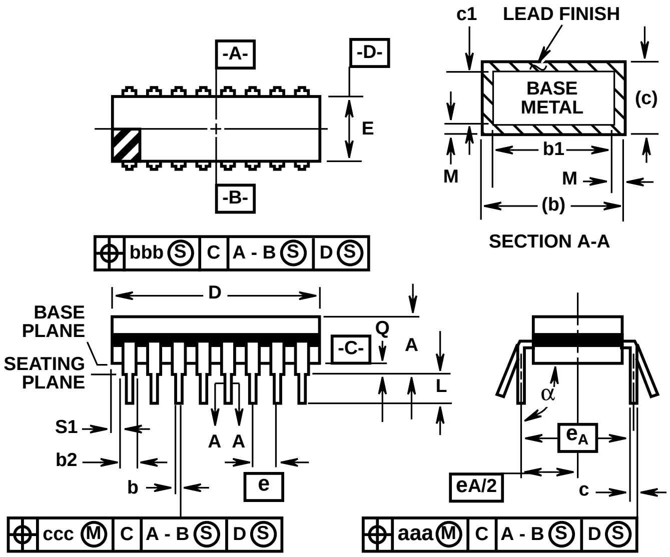
HA7-5020/883 CERAMIC DIP



Schematic Diagram



Packaging



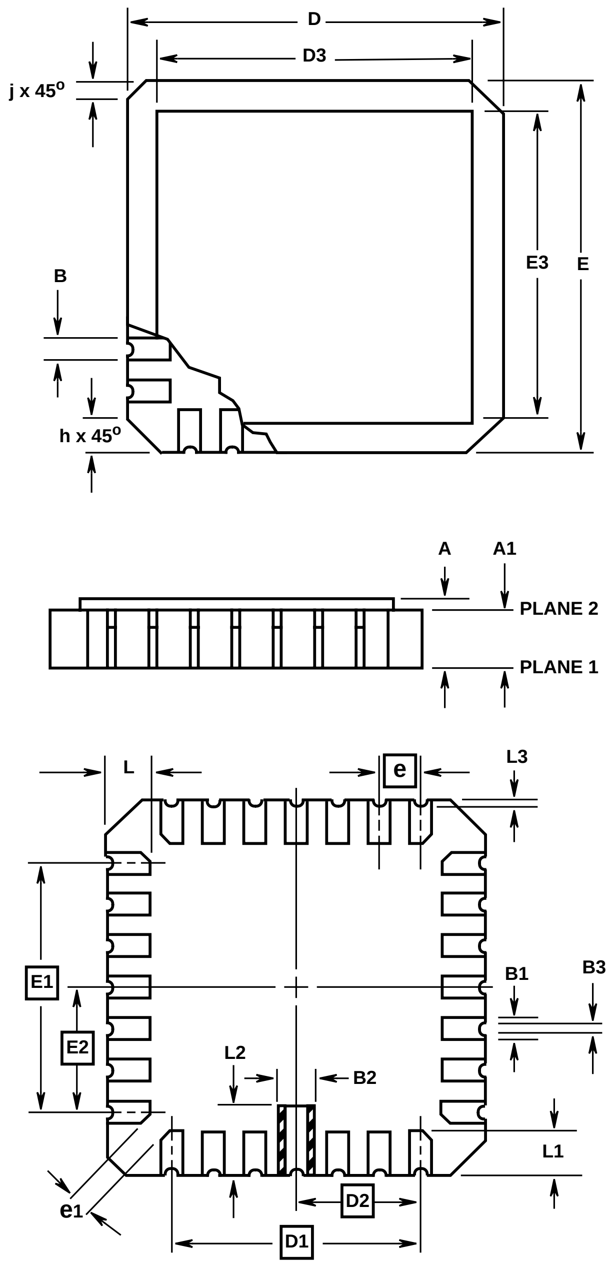
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.
11. Lead Finish: Type A.
12. Materials: Compliant to MIL-M-38510.

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Packaging (Continued)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.
8. Lead Finish: Type A.
9. Materials: Compliant to MIL-M-38510.

HA-5020

DESIGN INFORMATION

December 1999

100MHz Current Feedback Video Amplifier with Disable

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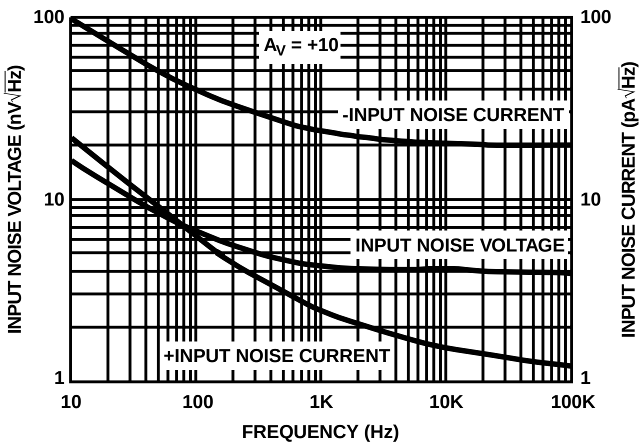
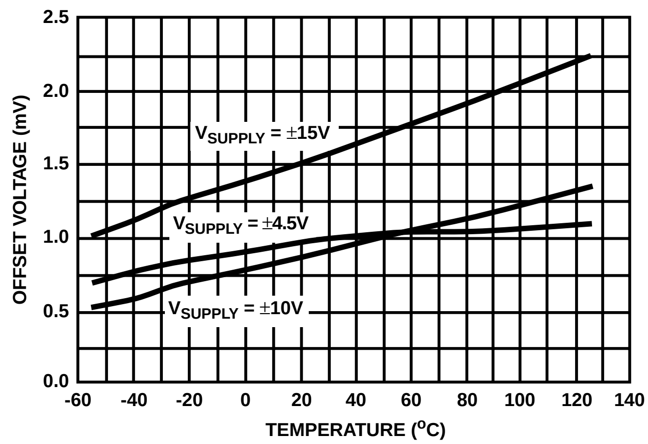
Typical Performance Curves V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

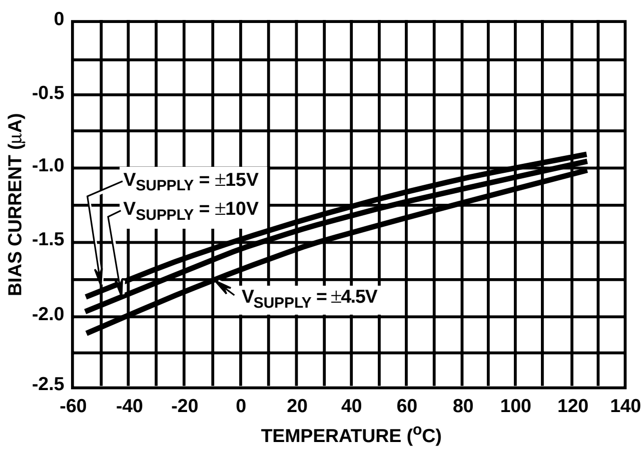
INPUT NOISE vs FREQUENCY
Average of 18 Units from 3 Lots



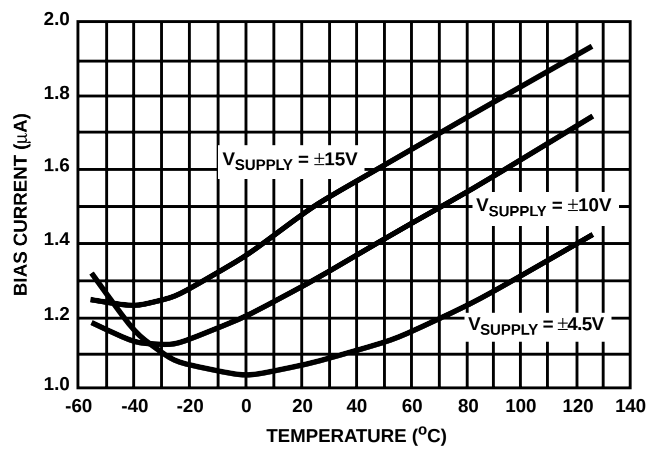
INPUT OFFSET VOLTAGE vs TEMPERATURE
Absolute Value Average of 30 Units from 3 Lots



+INPUT BIAS CURRENT vs TEMPERATURE
Average of 30 Units from 3 Lots



-INPUT BIAS CURRENT vs TEMPERATURE
Absolute Value Average of 30 Units from 3 Lots



DESIGN INFORMATION (Continued)

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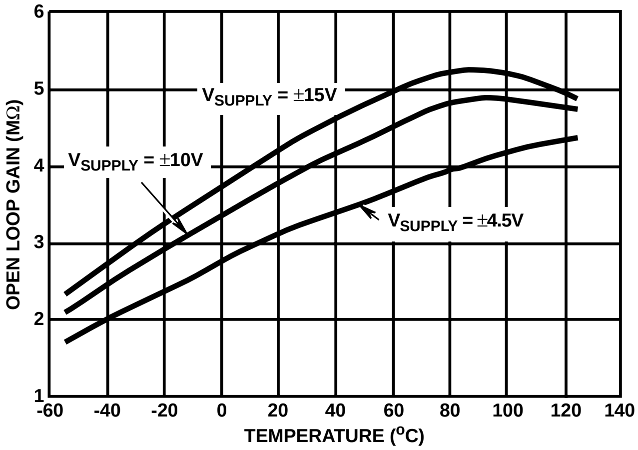
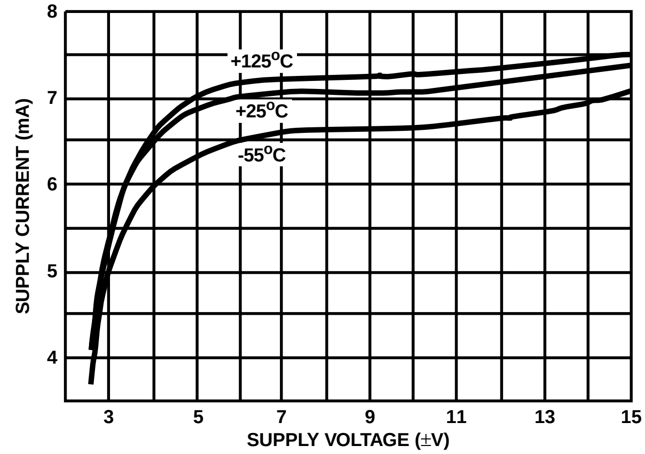
Typical Performance Curves V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

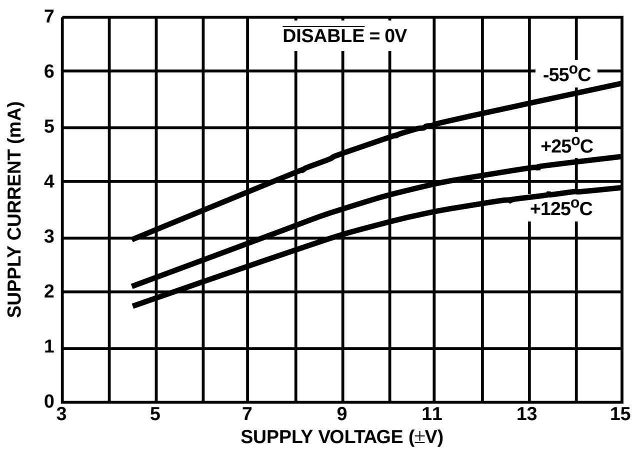
TRANSIMPEDANCE vs TEMPERATURE
Average of 30 Units from 3 Lots



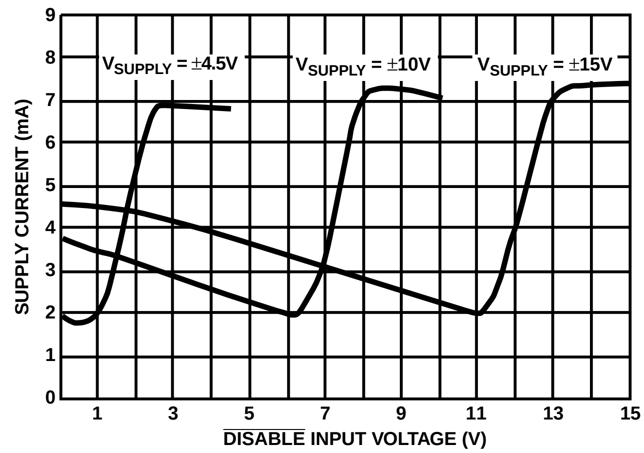
SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots



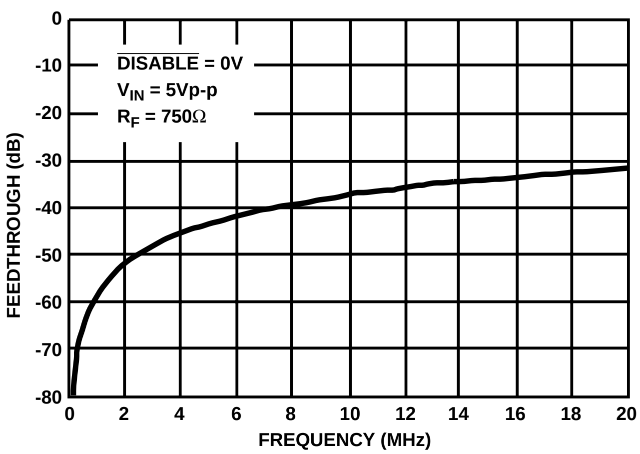
DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots



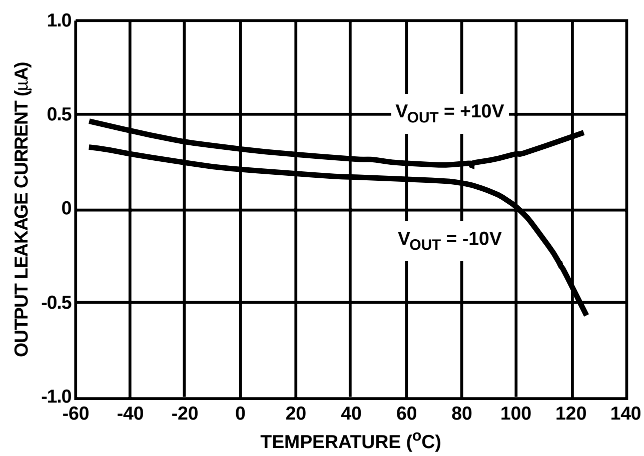
SUPPLY CURRENT vs DISABLE INPUT VOLTAGE



DISABLE MODE FEEDTHROUGH vs FREQUENCY



DISABLED OUTPUT LEAKAGE vs TEMPERATURE
Average of 30 Units from 3 Lots



DESIGN INFORMATION (Continued)

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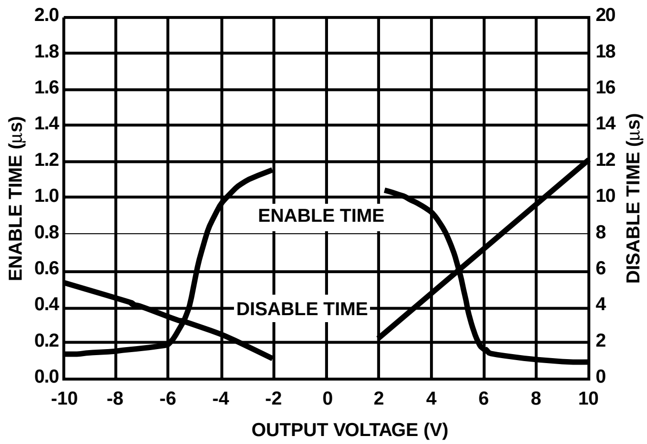
Typical Performance Curves

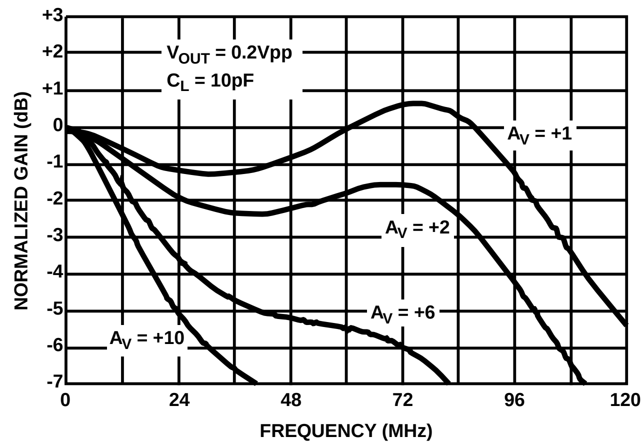
V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

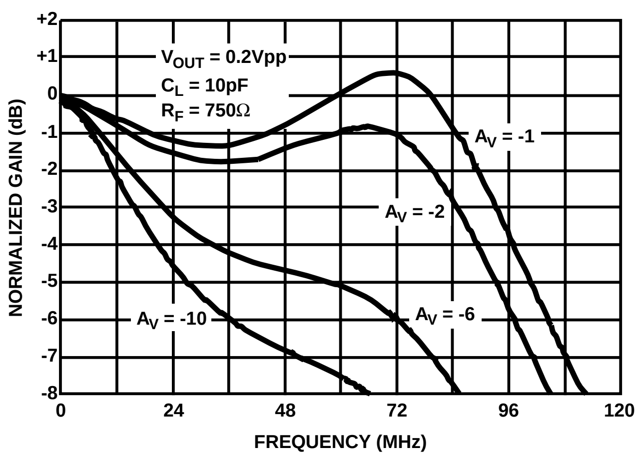
Average of 9 Units from 3 Lots



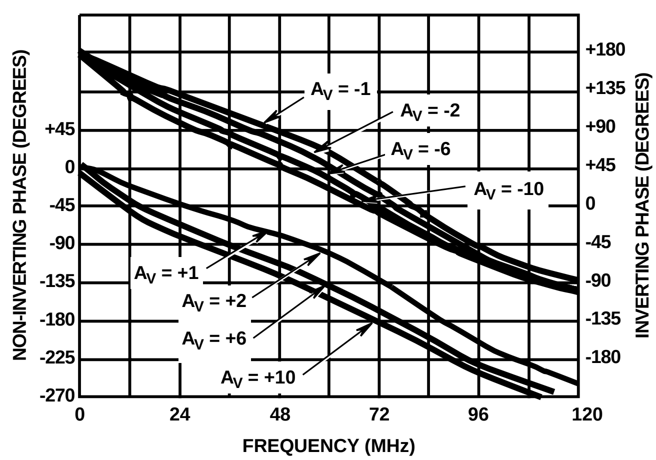
NON-INVERTING GAIN vs FREQUENCY



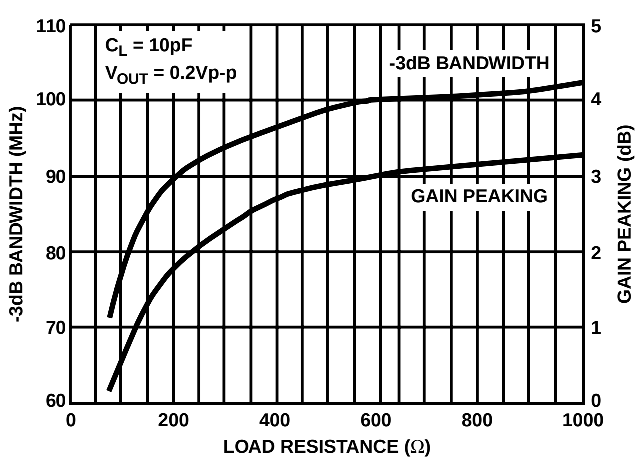
INVERTING FREQUENCY RESPONSE



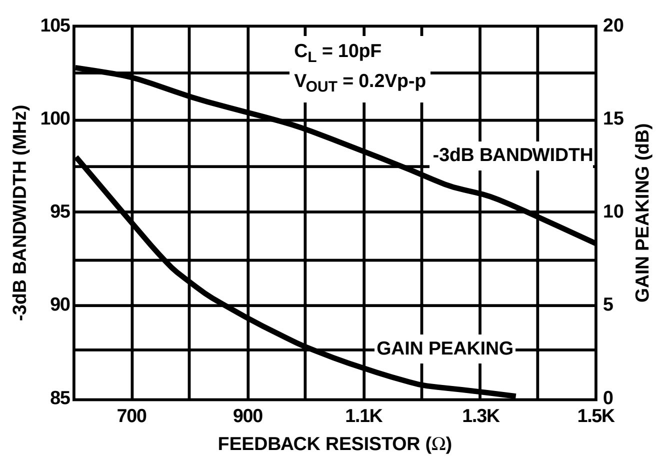
PHASE vs FREQUENCY



BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE



BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE



DESIGN INFORMATION (Continued)

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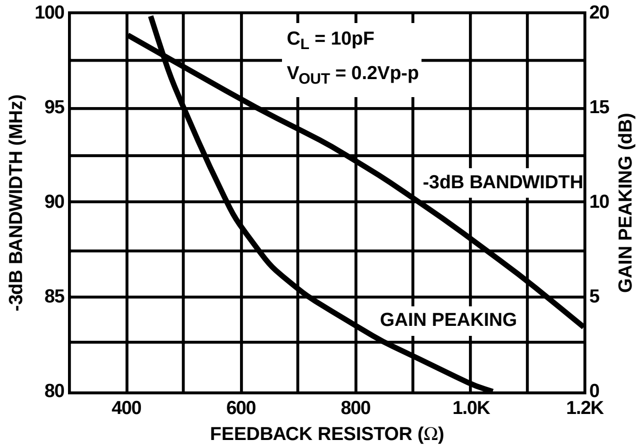
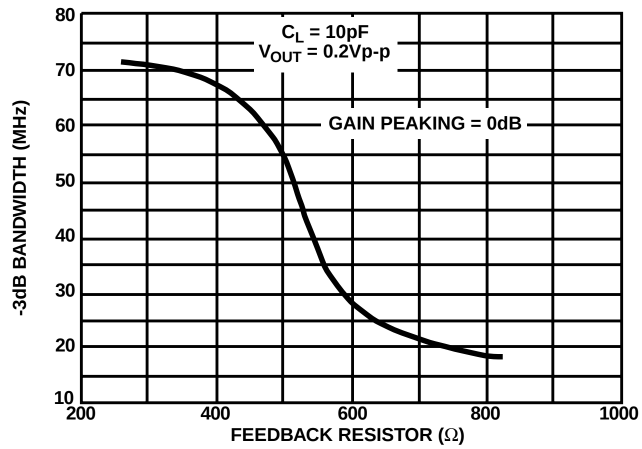
Typical Performance Curves

V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

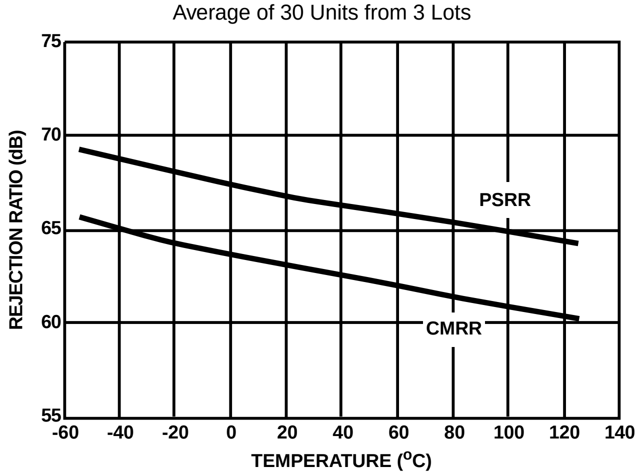
BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE
(A_V = +2)



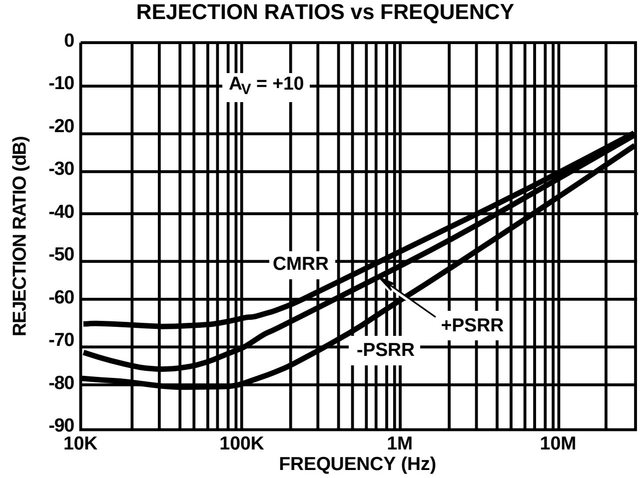
BANDWIDTH vs FEEDBACK RESISTANCE
(A_V = +10)



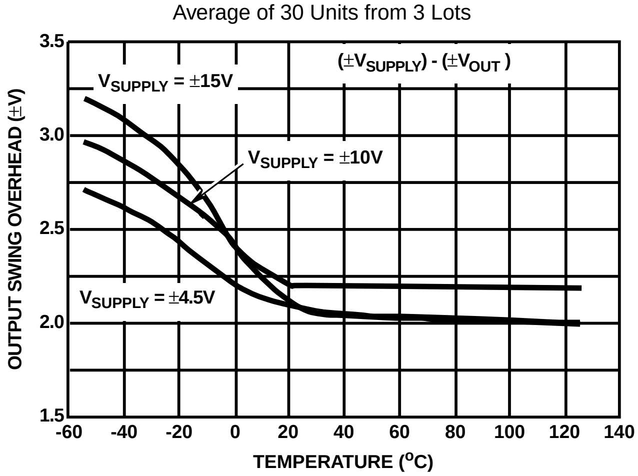
REJECTION RATIOS vs TEMPERATURE
Average of 30 Units from 3 Lots



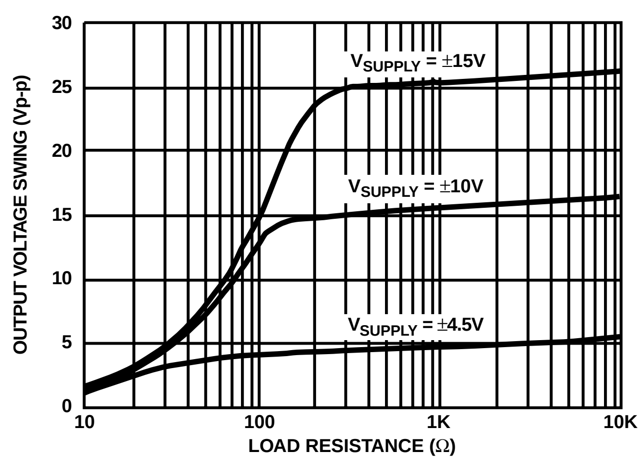
REJECTION RATIOS vs FREQUENCY



OUTPUT SWING OVERHEAD vs TEMPERATURE
Average of 30 Units from 3 Lots



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



DESIGN INFORMATION (Continued)

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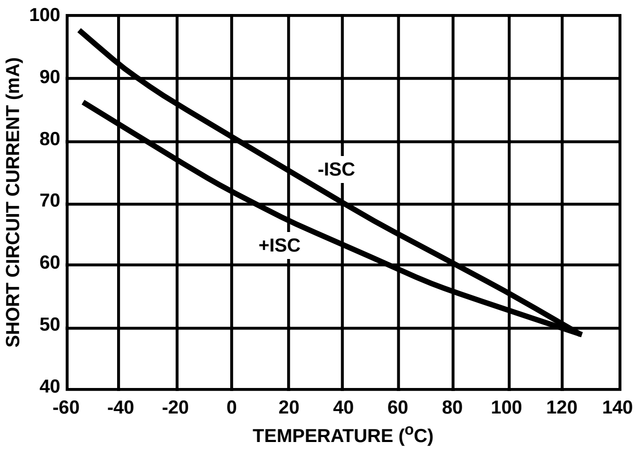
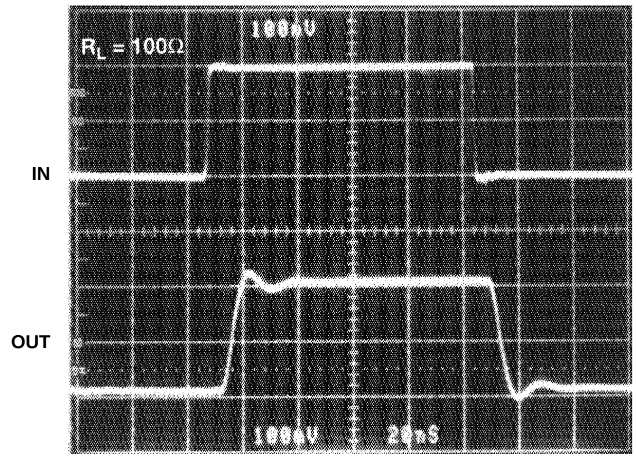
Typical Performance Curves V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

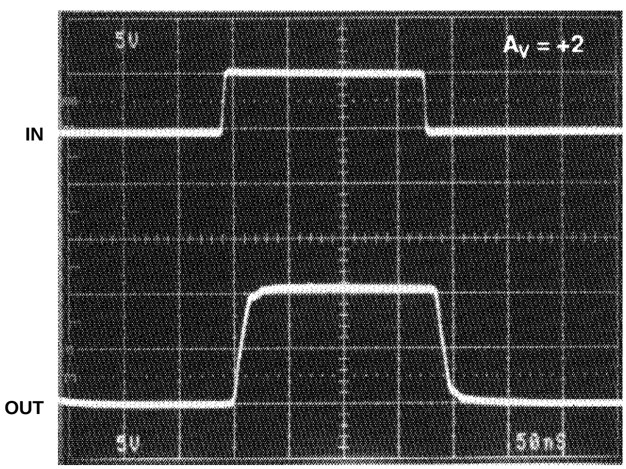
SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE



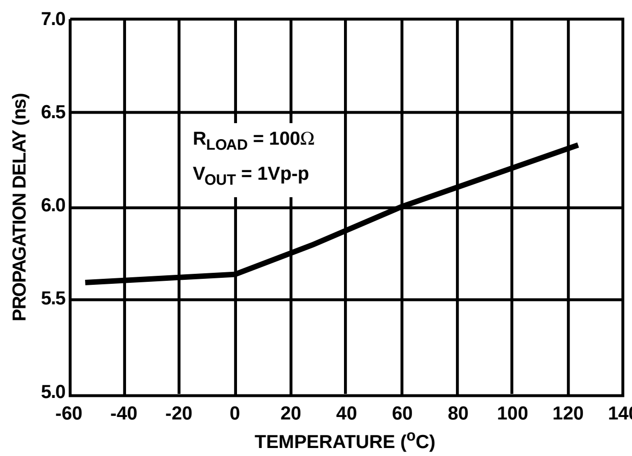
SMALL SIGNAL PULSE RESPONSE
Vertical Scale: V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.



LARGE SIGNAL PULSE RESPONSE
Vertical Scale: V_{IN} = 5V/Div.; V_{OUT} = 5V/Div.
Horizontal Scale: 50ns/Div.



PROPAGATION DELAY vs TEMPERATURE
Average of 18 Units from 3 Lots



DESIGN INFORMATION (Continued)

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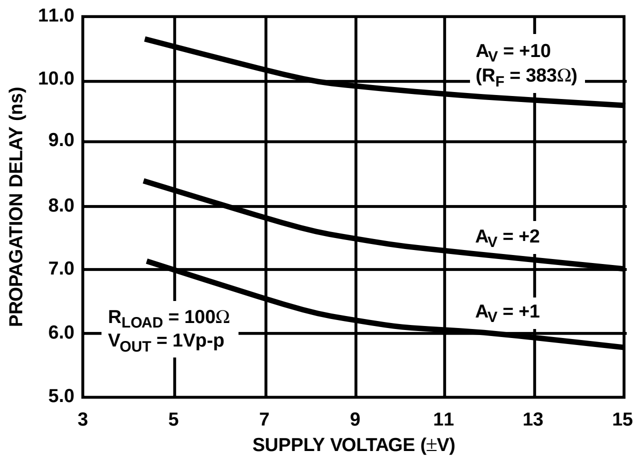
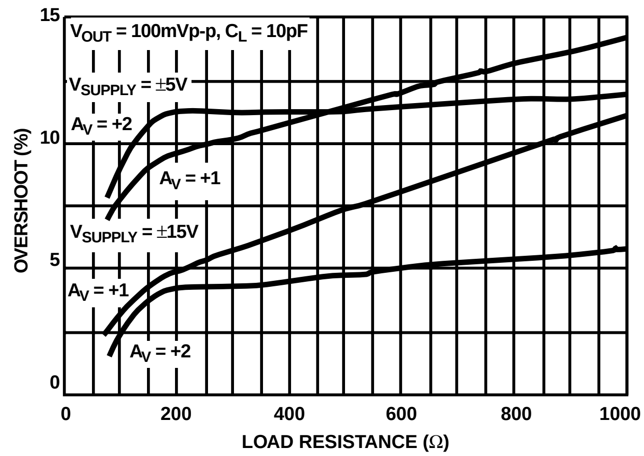
Typical Performance Curves
V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified

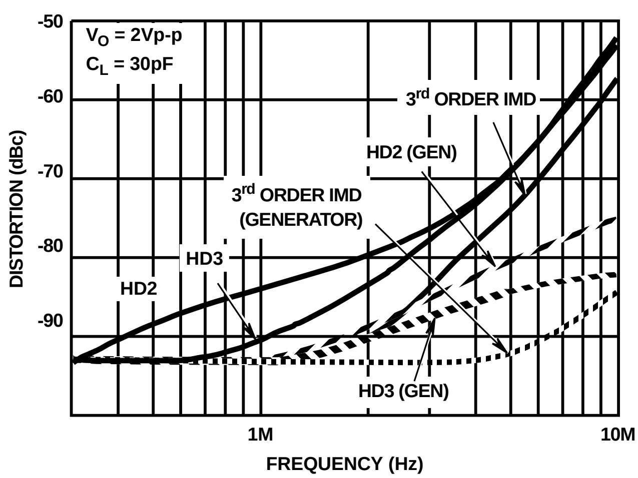
PROPAGATION DELAY vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots



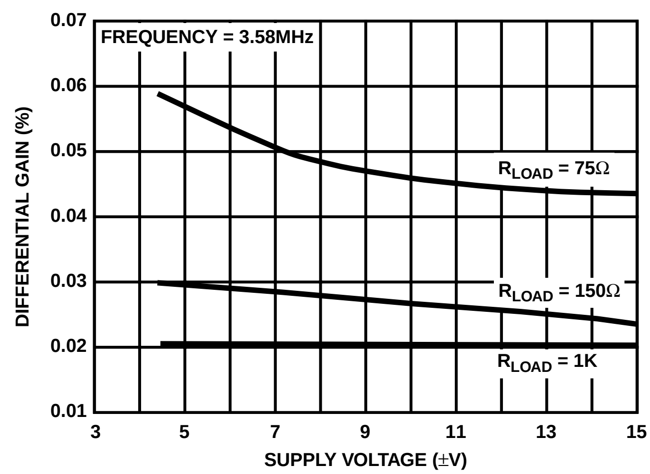
SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE



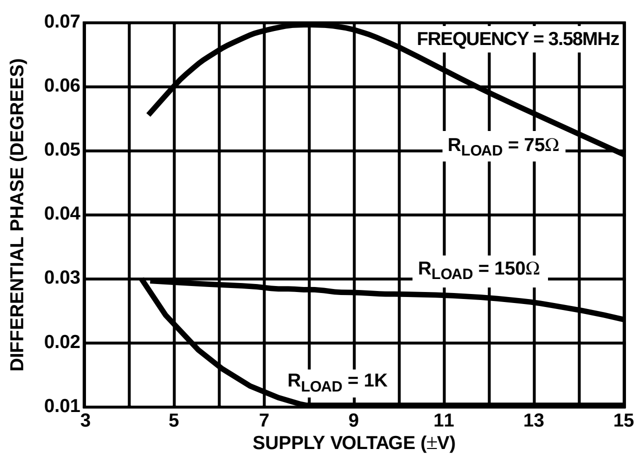
DISTORTION vs FREQUENCY



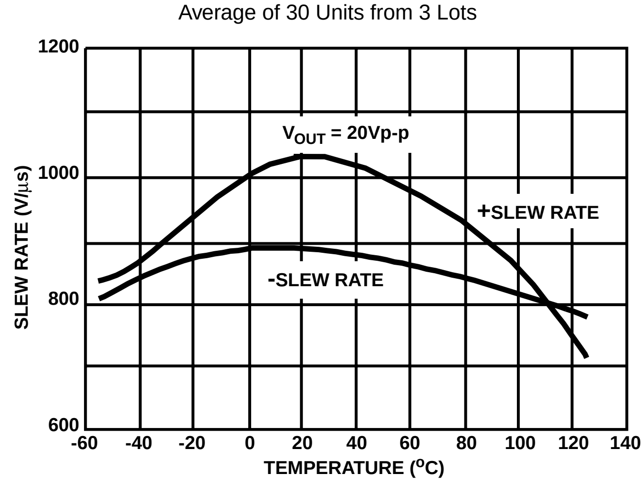
DIFFERENTIAL GAIN vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots



DIFFERENTIAL PHASE vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots



SLEW RATE vs TEMPERATURE
Average of 30 Units from 3 Lots



TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_F = 1kΩ, A_V = +1V/V, R_L = 400Ω, C_L ≤ 10pF, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	DESIGN LIMIT	UNITS
Input Offset Voltage	V_{CM} = 0V	+25°C	2	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	15	μV/°C
Positive Input Bias Current	V_{CM} = 0V	+25°C	3	Table 1	μA
Negative Input Bias Current	V_{CM} = 0V	+25°C	12	Table 1	μA
Input Common Mode Range		Full	±12	Table 1	V
Offset Voltage Adjustment	See Note 4, Table 1	Full	±40	Table 1	mV
Output Voltage Swing	V_{IN} = ±12.8	+25°C to +125°C	±12.7	Table 1	V
	V_{IN} = ±12.8	-55°C to 0°C	±11.8	Table 1	V
Output Current	Implied by V_{OUT}/400Ω	+25°C	31.7	Table 1	mA
Output Short Circuit Current	V_{IN} = ±10V, V_{OUT} = 0V	+25°C	65	Table 1	mA
Quiescent Supply Current	R_L = Open	Full	7.5	Table 1	mA
Supply Current, Disabled	R_L = Open, $V_{\overline{DIS}}$ = 0V	Full	5.0	Table 1	mA
Slew Rate	V_{IN} = 20Vp-p	+25°C	±800	Table 2	V/μs
Overshoot	V_O = 1Vp-p, R_L = 100Ω	+25°C	7	Table 3	%
Input Noise Voltage	f = 1kHz	+25°C	4.5	8	$nV/\sqrt{Hz}$
Positive Input Noise Current	f = 1kHz	+25°C	2.5	4	$pA/\sqrt{Hz}$
Negative Input Noise Current	f = 1kHz	+25°C	25	40	$pA/\sqrt{Hz}$
Differential Gain	R_L = 150Ω, NTC-7 Composite	+25°C	0.025	0.05	%
Differential Phase	R_L = 150Ω, NTC-7 Composite	+25°C	0.025	0.05	Degrees

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