

August 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD(Si)
- SEP Effective LET No Upsets: >100 MEV-cm²/mg
- Single Event Upset (SEU) Immunity < 2 x 10⁻⁹ Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10¹² Rads (Si)/s
- Dose Rate Upset >10¹⁰ RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
 - VIL = 30% of VCC Max
 - VIH = 70% of VCC Min
- Input Current Levels $I_i \leq 5\mu A$ at VOL, VOH

Description

The Intersil HCS02MS is a Radiation Hardened Quad 2-Input NOR Gate. A low on both inputs forces the output to a High state.

The HCS02MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

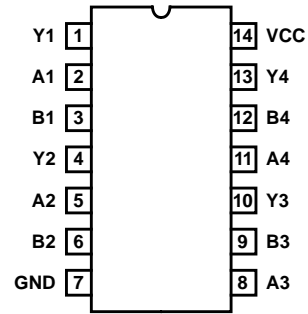
The HCS02MS is supplied in a 14 lead Ceramic Flatpack Package (K suffix) or a 14 lead SBDIP Package (D suffix).

Ordering Information

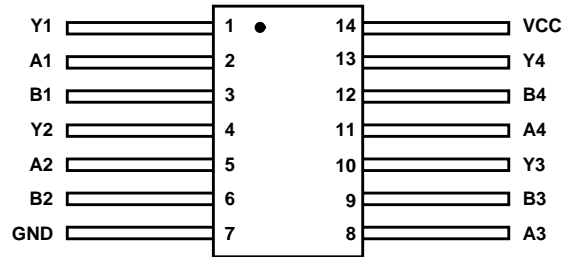
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS02DMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead SBDIP
HCS02KMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
HCS02D/ Sample	+25°C	Sample	14 Lead SBDIP
HCS02K/ Sample	+25°C	Sample	14 Lead Ceramic Flatpack
HCS02HMSR	+25°C	Die	Die

Pinouts

14 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T14
TOP VIEW



14 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP3-F14
TOP VIEW

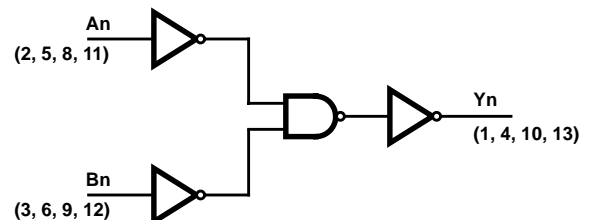


TRUTH TABLE

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	L
H	L	L
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



Specifications HCS02MS

Absolute Maximum Ratings

Supply Voltage	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal)	±25mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Junction Temperature (TJ)	+175°C
Lead Temperature (Soldering 10sec)	+265°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	74°C/W	24°C/W
Ceramic Flatpack Package	116°C/W	30°C/W
Maximum Package Power Dissipation at +125°C		
SBDIP Package	0.66W	
Ceramic Flatpack Package	0.43W	
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:		
SBDIP Package	13.5mW/°C	
Ceramic Flatpack Package	8.6mW/°C	

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 30% of VCC Max.
Input Rise and Fall Times at 4.5V VCC (TR, TF)	100ns/V Max	Input High Voltage (VIH)	70% of VCC to VCC Min.
Operating Temperature Range (TA)	-55°C to +125°C		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, $VO \geq 4.0V$ is recognized as a logic "1", and $VO \leq 0.5V$ is recognized as a logic "0".

Specifications HCS02MS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

- All voltages referenced to device GND.
- AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $T_R = T_F = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = V_{CC}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, $f = 1\text{MHz}$	1	+25°C	-	18	pF
			1	+125°C, -55°C	-	26	pF
Input Capacitance	CIN	VCC = 5.0V, $f = 1\text{MHz}$	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, $V_{IN} = V_{CC}$ or GND	+25°C	-	0.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, $V_{IN} = V_{CC}$ or GND, $V_{OUT} = 0.4V$	+25°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, $V_{IN} = V_{CC}$ or GND, $V_{OUT} = V_{CC} - 0.4V$	+25°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, $V_{IH} = 0.70(V_{CC})$, $V_{IL} = 0.30(V_{CC})$ at 200K RAD, $I_{OL} = 50\mu\text{A}$	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, $V_{IH} = 0.70(V_{CC})$, $V_{IL} = 0.30(V_{CC})$ at 200K RAD, $I_{OH} = -50\mu\text{A}$	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, $V_{IN} = V_{CC}$ or GND	+25°C	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, $V_{IH} = 0.70(V_{CC})$, $V_{IL} = 0.30(V_{CC})$ at 200K RAD, (Note 3)	+25°C	-	-	-
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	ns
	TPLH	VCC = 4.5V	+25°C	2	22	ns

NOTES:

- All voltages referenced to device GND.
- AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $T_R = T_F = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = V_{CC}$.
- For functional tests, $V_O \geq 4.0V$ is recognized as a logic "1", and $V_O \leq 0.5V$ is recognized as a logic "0".

Specifications HCS02MS

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

COMFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	
		TESTED	RECORDED
Initial Test	100% 5004	1, 7, 9	1 (Note 2)
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)
PDA	100% 5004	1, 7, Δ	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)
Subgroup B6	Sample 5005	1, 7, 9	
Group D	Sample 5005	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 Method 5005 may be exercised.
2. Table 5 parameters only.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

Specifications HCS02MS

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
1, 4, 10, 13	2, 3, 5, 6, 7, 8, 9, 11, 12	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 4, 10, 13	7	-	2, 3, 5, 6, 8, 9, 11, 12, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	1, 4, 10, 13	14	2, 3, 5, 6, 8, 9, 11, 12	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% static burn-in.
2. Each Pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 4, 10, 13	7	2, 3, 5, 6, 8, 9, 11, 12, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)	100% Interim Electrical Test 1 (T1)
GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Delta Calculation (T0-T1)
100% Nondestructive Bond Pull, Method 2023	100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015
Sample - Wire Bond Pull Monitor, Method 2011	100% Interim Electrical Test 2 (T2)
Sample - Die Shear Monitor, Method 2019 or 2027	100% Delta Calculation (T0-T2)
100% Internal Visual Inspection, Method 2010, Condition A	100% PDA 1, Method 5004 (Notes 1 and 2)
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles	100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015
100% Constant Acceleration, Method 2001, Condition per Method 5004	100% Interim Electrical Test 3 (T3)
100% PIND, Method 2020, Condition A	100% Delta Calculation (T0-T3)
100% External Visual	100% PDA 2, Method 5004 (Note 2)
100% Serialization	100% Final Electrical Test
100% Initial Electrical Test (T0)	100% Fine/Gross Leak, Method 1014
100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015	100% Radiographic, Method 2012 (Note 3)
	100% External Visual, Method 2009
	Sample - Group A, Method 5005 (Note 4)
	100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
 - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
 - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
 - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
 - X-Ray report and film. Includes penetrometer measurements.
 - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
 - Lot Serial Number Sheet (Good units serial number and lot number).
 - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
 - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Timing Diagrams

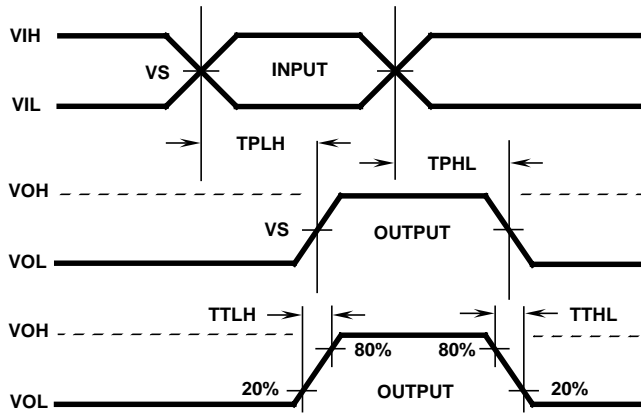


FIGURE 1

AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit

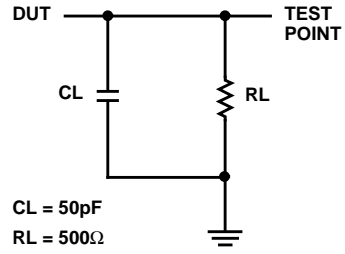


FIGURE 2

HCS02MS

Die Characteristics

DIE DIMENSIONS:

87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:

Type: AlSi
Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2
Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

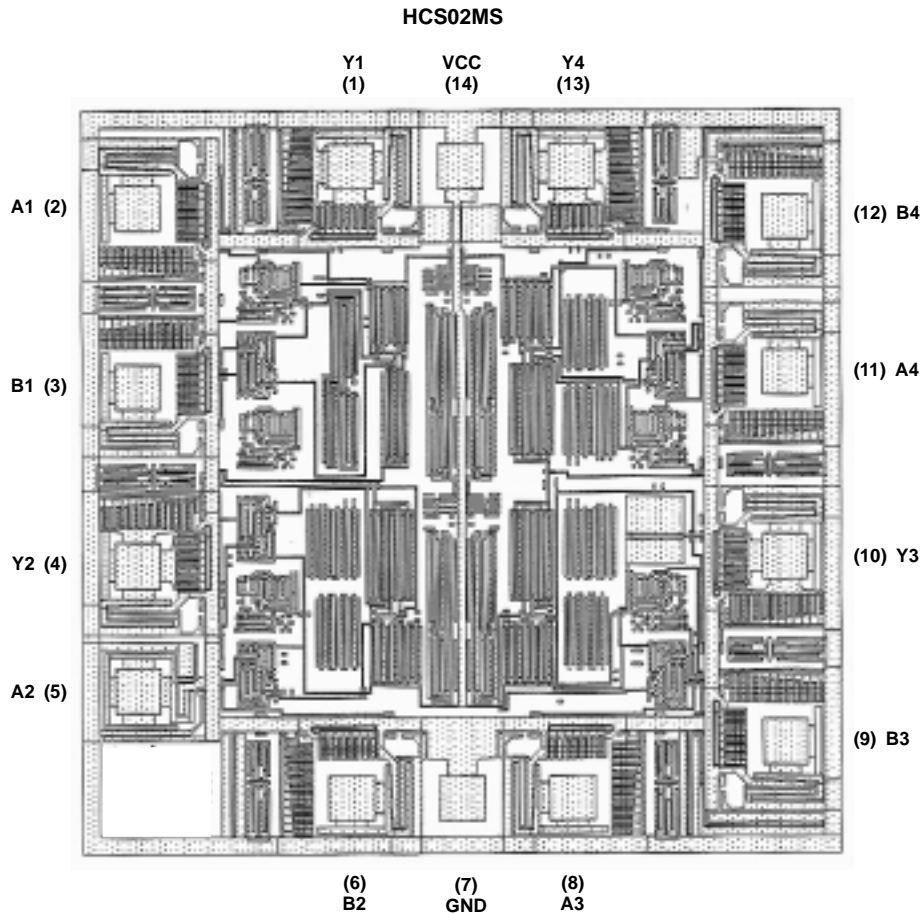
WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$
4 x 4 mils

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>