HD68450 DMAC (Direct Memory Access Controller)

HD68450 is a DMA Controller for the HMCS68000 16-bit microprocessor system. Increasingly large amounts of data are being processed by the 16-bit microprocessor systems and, consequently, the ability to transfer large amounts of data in a large memory space becomes a necessity. HD68450 has been designed to meet this requirement in a highly efficient manner.

HD68450 has 4 independent DMA channels of operation with programmable channel priorities. It can handle data sizes of byte, word (16-bits), and longword (32-bits), and has a direct addressing range of 16 megabytes. It performs 16-bit DMA transfers on an asynchronous bus as well as synchronous transfers with 8-bit HMCS6800 peripheral LSI's using the enable signal. It outputs function code signal for memory management and it can handle bus error, halt, and retry operations to compliment the highly reliable HMCS68000 system.

The transfer modes of HD68450 consists of transfer between memory and peripheral device, and also between memories. Transfer of blocks of data can be done by using the continue mode, array chain mode, or linked array chain mode. Single addressing mode is provided for transfer between memory and device having the same port size, as well as dual addressing mode for different port sizes. In the dual addressing mode, transfer is done in two bus cycles – memory to DMAC, then DMAC to device. As can be seen by its many features, HD68450 is a highly intelligent device to meet the different data transfer requirements for each individual applications.

FEATURES

- HMCS68000 Bus Compatible
- Interfaces Directly with HMCS68000/HMCS6800 Peripherals
- Memory-to-Device, Device-to-Memory, and Memory-to-Memory Transfers.
- Continue Mode and Array Chained, Linked Array Chained Operations
- 4 Independent Channels with Programmable Priorities
- Handles Byte, Word, and Longword Data Sizes
- External Request Mode and Auto-Request Mode
- Maximum Transfer Rate of 2 Mega Word/Sec
- PROGRAMMING MODEL



-ADVANCE INFORMATION-



PIN ARRANGEMENT

REO, 1 REO, 2		B4 DDIR 53 DBEN
REG. IT		BILLAS
PCE, 15		BOOWN
PCL, C		59 BR
PCL, 7		SEBG
134		57 A.
BGACK		50 A2
DTCIC		55 Aa
DTACK		54 A.
UDS12		SE As
LDS		52 🗛
ASLA		51V₀₀
H/WII5		50 A7
V 300 110	HD68450	49Vm
		48 A./D.
		A./D.
ACKER		40 A10/D2
IREO		Au/Ds
DONE 22		43 A12/D4
ACK. 23		42 4/D.
ACK. 24		ATA. /D.
ACK, 25		40 A
ACK. 28		39 A /D.
BEC. 27		38 Au /Die
BEC, 28		37 A10/D11
BEC, 29		A10/D12
FC, 30		33 An /Dis
FC I		34 A22/D14
FC. 32		33 A23/D15

(Top View)