

**Dual, SPDT CMOS Analog Switch**

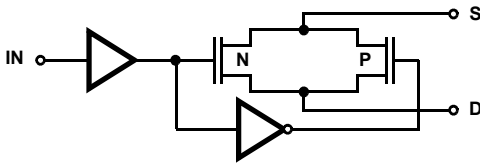
The HI-303 switch is a monolithic device fabricated using CMOS technology and the Intersil dielectric isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-303 is TTL compatible and has a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4V. (See pinouts for switch conditions with a logic "1" input.)

**Ordering Information**

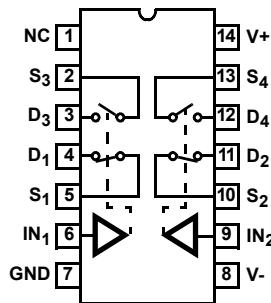
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0303-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0303-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0303-5	0 to 75	14 Ld PDIP	E14.3
HI9P0303-5	0 to 75	14 Ld SOIC	M14.15
HI9P0303-9	-40 to 85	14 Ld SOIC	M14.15

**Functional Diagram**



**Pinout** Switch States Shown For A Logic "1" Input

**HI-303 (PDIP, CERDIP, SOIC)**  
TOP VIEW



LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

**Features**

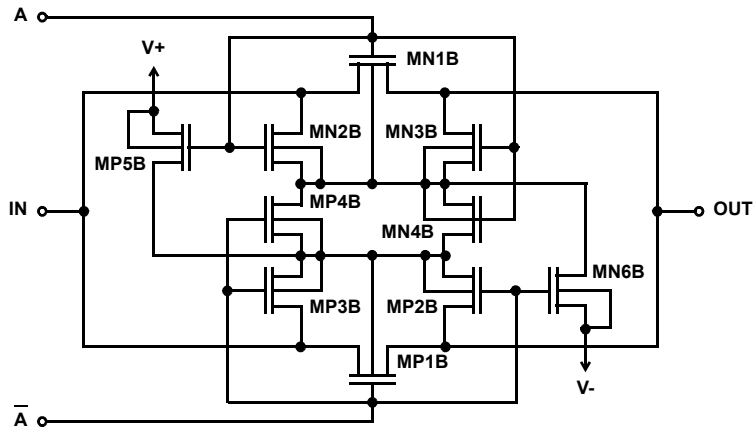
- Analog Signal Range ( $\pm 15V$  Supplies) . . . . .  $\pm 15V$
- Low Leakage at 25°C . . . . . 40pA
- Low Leakage at 125°C . . . . . 1nA
- Low On Resistance at 25°C . . . . . 35 $\Omega$
- Break-Before-Make Delay . . . . . 60ns
- Charge Injection . . . . . 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power (Typ) . . . . . 1.0mW

**Applications**

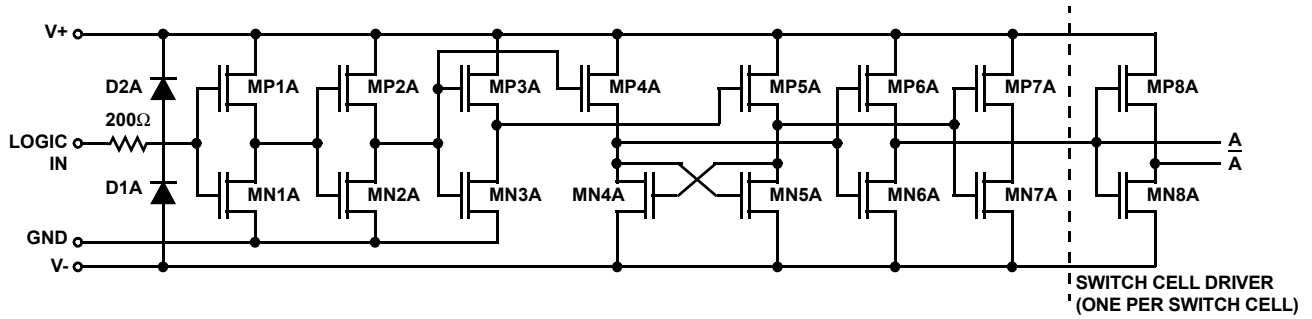
- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



**Absolute Maximum Ratings**

Voltage Between Supplies (V+ to V-) . . . . . 44V (±22V)  
 Digital Input Voltage . . . . . (V+) +4V to (V-) -4V  
 Analog Input Voltage . . . . . (V+) +1.5V to (V-) -1.5V  
 Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP  
 ESD Classification . . . . . Class 1

**Operating Conditions**

Temperature Range  
 HI-303-2 . . . . . -55°C to 125°C  
 HI-303-5 . . . . . 0°C to 75°C  
 HI-303-9 . . . . . -40°C to 85°C

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  $\theta_{JC}$  (°C/W)  
 CERDIP Package . . . . . 80 24  
 PDIP Package . . . . . 90 N/A  
 SOIC Package . . . . . 120 N/A  
 Maximum Junction Temperature  
 Ceramic Packages . . . . . 175°C  
 Plastic Packages . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications** Supplies = +15V, -15V;  $V_{IN}$  = Logic Input.  $V_{IN}$  - for Logic "1" = 4V, for Logic "0" = 0.8V. Unless Otherwise Specified

PARAMETER	TEMP (°C)	-2			-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>DYNAMIC CHARACTERISTICS</b>								
Switch ON Time, $t_{ON}$	25	-	210	300	-	210	300	ns
Switch OFF Time, $t_{OFF}$	25	-	160	250	-	160	250	ns
Break-Before-Make Delay, $t_{OPEN}$	25	-	60	-	-	60	-	ns
Charge Injection Voltage, $\Delta V$ (Note 7)	25	-	3	-	-	3	-	mV
OFF Isolation (Note 6)	25	-	60	-	-	60	-	dB
Input Switch Capacitance, $C_{S(OFF)}$	25	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$	25	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$	25	-	35	-	-	35	-	pF
Digital Input Capacitance, $C_{IN}$	25	-	5	-	-	5	-	pF
<b>DIGITAL INPUT CHARACTERISTICS</b>								
Input Low Level, $V_{INL}$	Full	-	-	0.8	-	-	0.8	V
Input High Level, $V_{INH}$ (Note 10)	Full	4	-	-	4	-	-	V
Input Leakage Current (Low), $I_{INL}$ (Note 5)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), $I_{INH}$ (Note 5)	Full	-	-	1	-	-	1	µA
<b>ANALOG SWITCH CHARACTERISTICS</b>								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
ON Resistance, $r_{ON}$ (Note 2)	25	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
OFF Input Leakage Current, $I_{S(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
OFF Output Leakage Current, $I_{D(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
ON Leakage Current, $I_{D(ON)}$ (Note 4)	25	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA

**Electrical Specifications** Supplies = +15V, -15V;  $V_{IN}$  = Logic Input.  $V_{IN}$  - for Logic "1" = 4V, for Logic "0" = 0.8V. Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (°C)	-2			-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>POWER SUPPLY CHARACTERISTICS</b>								
Current, I+ (Note 8)	25	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
Current, I- (Note 8)	25	-	0.01	10	-	0.01	100	$\mu$ A
	Full	-	-	100	-	-	-	$\mu$ A
Current, I+ (Note 9)	25	-	0.01	10	-	0.01	100	$\mu$ A
	Full	-	-	100	-	-	-	$\mu$ A
Current, I- (Note 9)	25	-	0.01	10	-	0.01	100	$\mu$ A
	Full	-	-	100	-	-	-	$\mu$ A

**NOTES:**

- $V_S = \pm 10V$ ,  $I_{OUT} = \mp 10mA$ . On resistance derived from the voltage measured across the switch under these conditions.
- $V_S = \pm 14V$ ,  $V_D = \mp 14V$ .
- $V_S = V_D = \pm 14V$ .
- The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
- $V_S = 1V_{RMS}$ ,  $f = 500kHz$ ,  $C_L = 15pF$ ,  $R_L = 1K$ .
- $V_S = 0V$ ,  $C_L = 10nF$ , Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged. Charge Injection =  $Q = C_L \times \Delta V$ .
- $V_{IN} = 4V$  (one input, all other inputs = 0V).
- $V_{IN} = 0.8V$  (all inputs).
- To drive from DTL/TTL circuits, pullup resistors to +5V supply are recommended.

**Test Circuits and Waveforms**

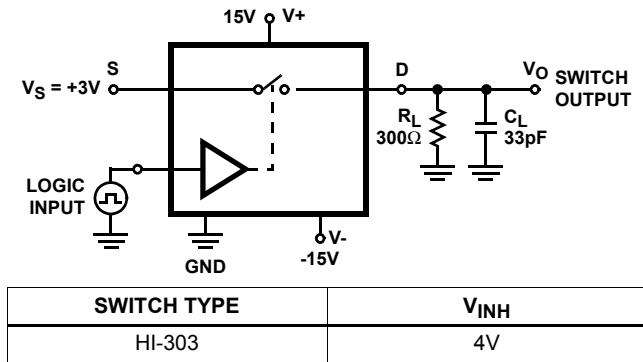


FIGURE 1A. TEST CIRCUIT

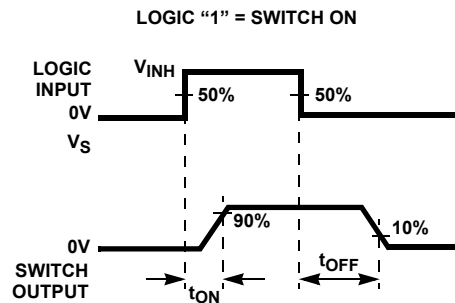


FIGURE 1B. MEASUREMENT POINTS

FIGURE 1. SWITCH  $t_{ON}$  AND  $t_{OFF}$

Test Circuits and Waveforms (Continued)

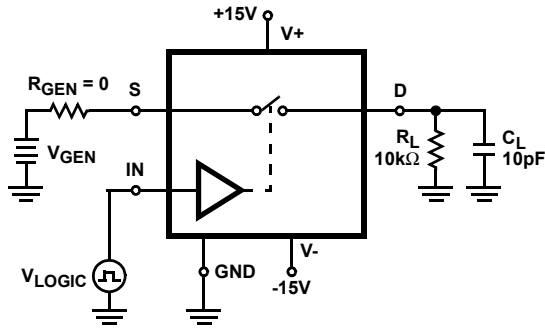


FIGURE 2A. TEST CIRCUIT

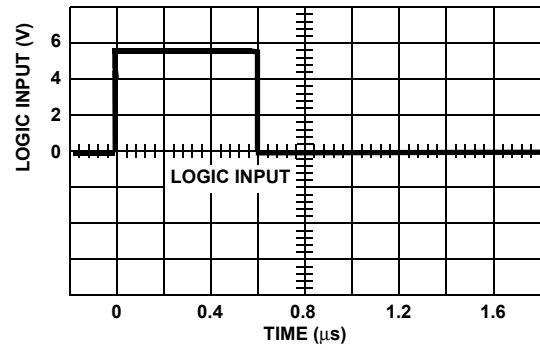


FIGURE 2B. TTL LOGIC INPUT

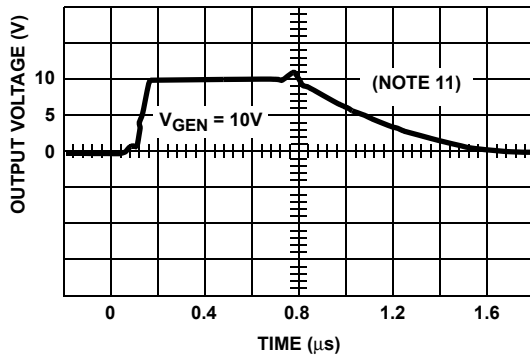


FIGURE 2C.  $V_{ANALOG} = 10V$

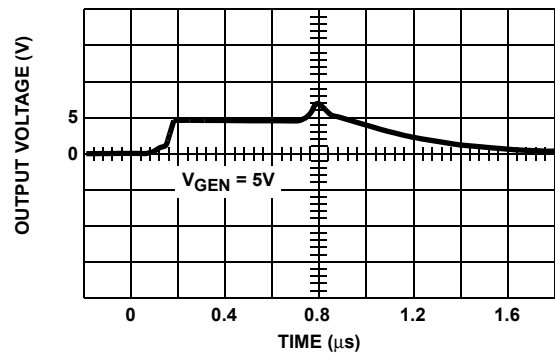


FIGURE 2D.  $V_{ANALOG} = 5V$

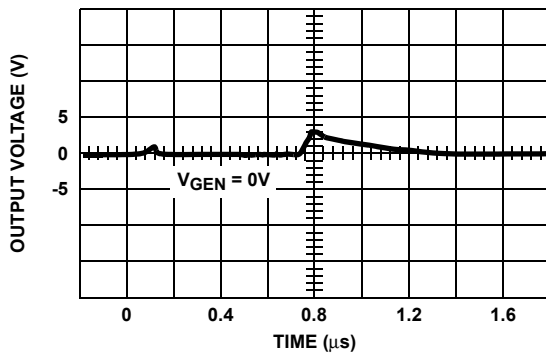


FIGURE 2E.  $V_{ANALOG} = 0V$

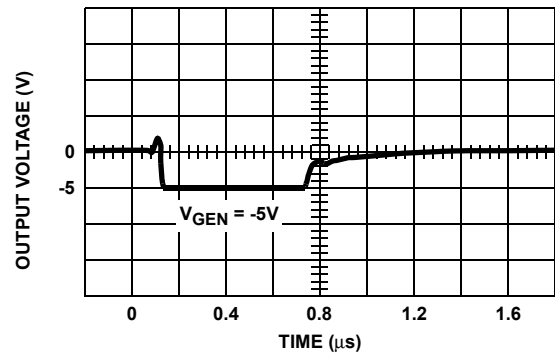


FIGURE 2F.  $V_{ANALOG} = -5V$

Test Circuits and Waveforms (Continued)

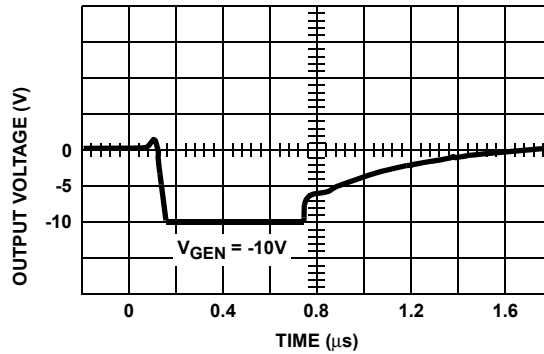
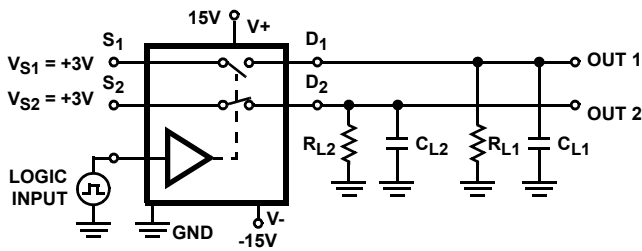


FIGURE 2G.  $V_{ANALOG} = -10V$

NOTE:

11. If  $R_{GEN}$ ,  $R_L$  or  $C_L$  is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 2. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES



SWITCH TYPE	$V_{INH}$
HI-303	5V

FIGURE 3A. TEST CIRCUIT

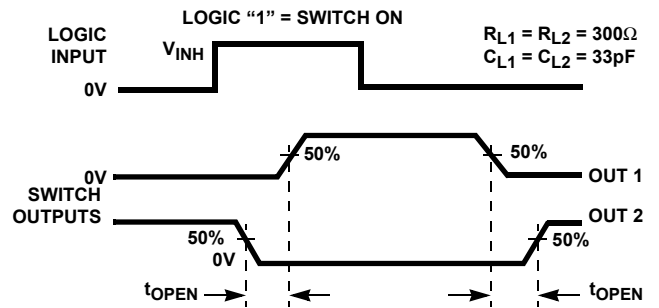


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. BREAK-BEFORE-MAKE DELAY ( $t_{OPEN}$ )

Typical Performance Curves

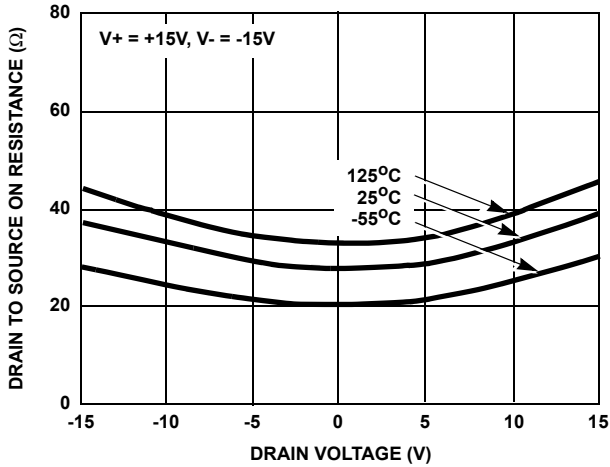


FIGURE 4.  $r_{DS(ON)}$  vs  $V_D$

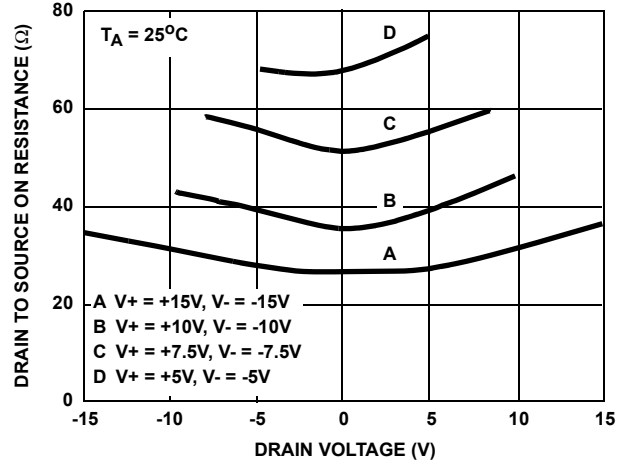


FIGURE 5.  $r_{DS(ON)}$  vs  $V_D$

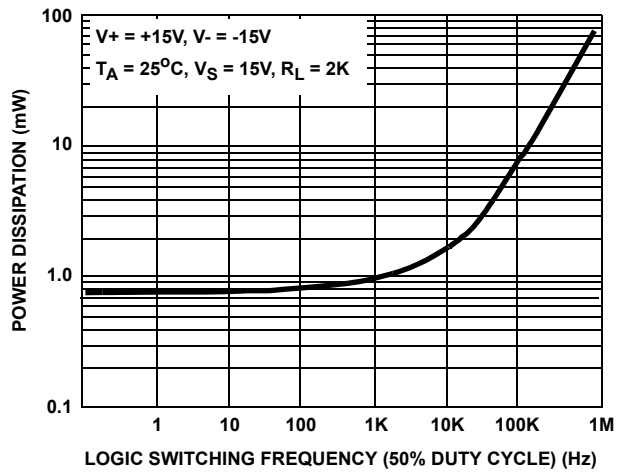


FIGURE 6. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

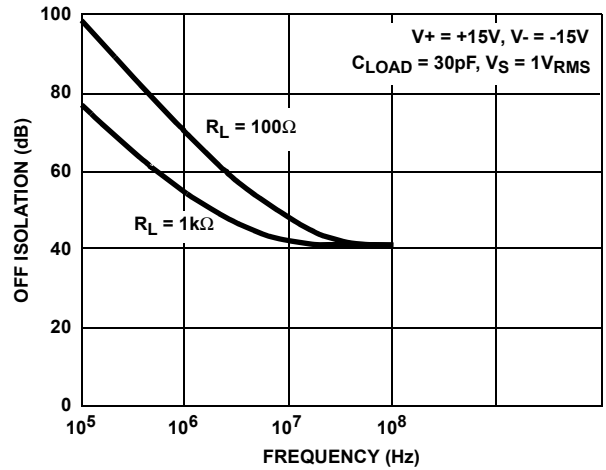


FIGURE 7. OFF ISOLATION vs FREQUENCY

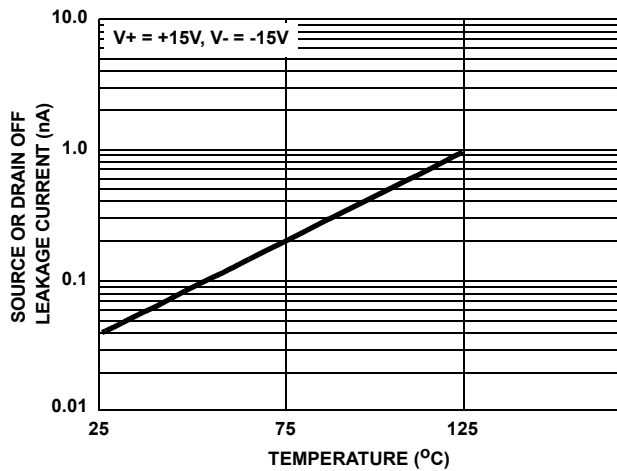


FIGURE 8.  $I_{S(OFF)}$  OR  $I_{D(OFF)}$  vs TEMPERATURE\*

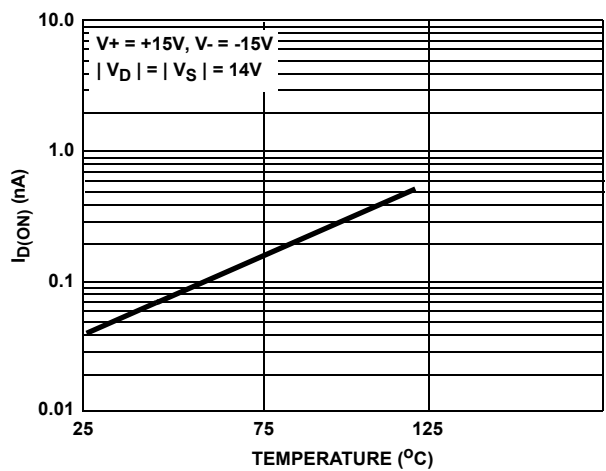


FIGURE 9.  $I_{D(ON)}$  vs TEMPERATURE\*

\* The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical Performance Curves (Continued)

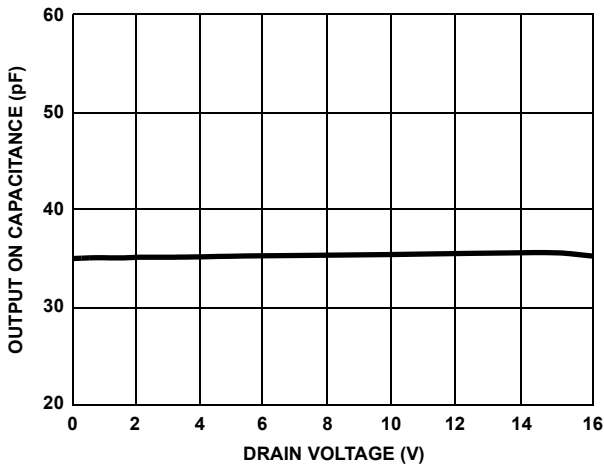


FIGURE 10. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

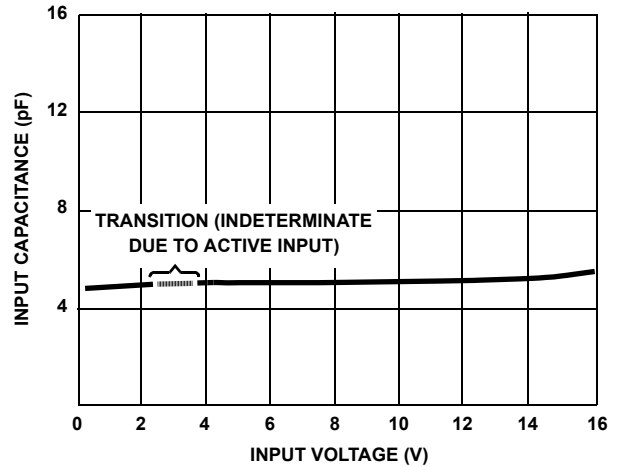


FIGURE 11. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

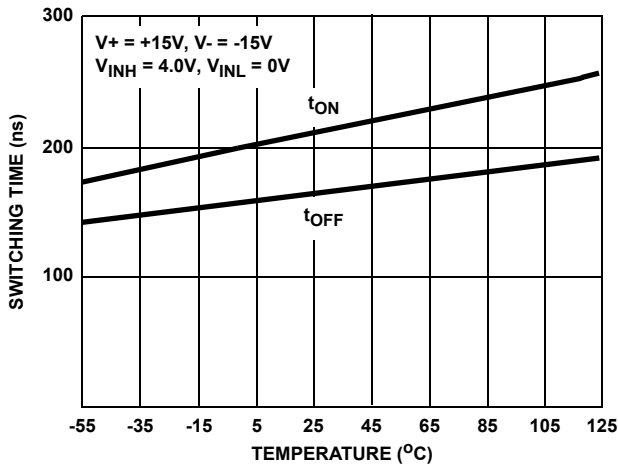


FIGURE 12. SWITCHING TIME vs TEMPERATURE

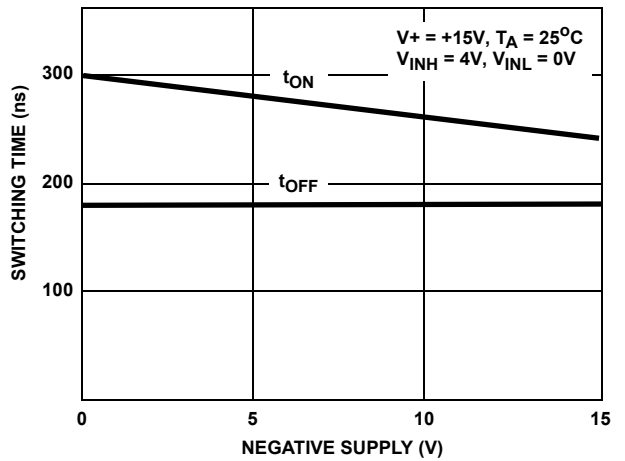


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

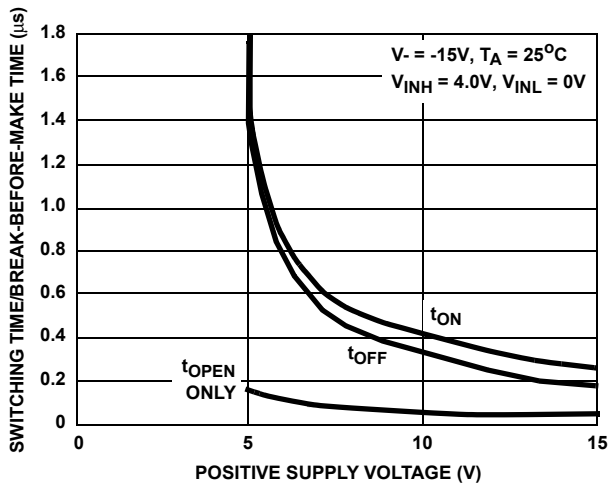


FIGURE 14. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE

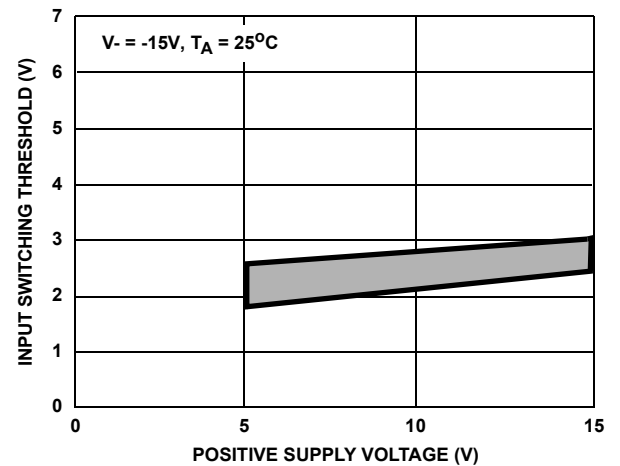
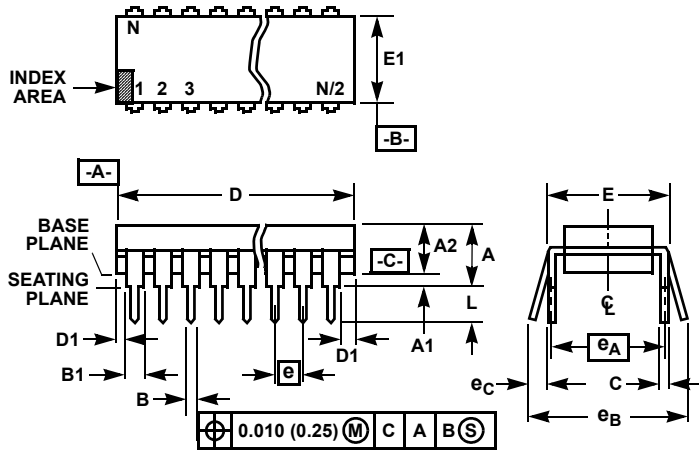


FIGURE 15. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE



Dual-In-Line Plastic Packages (PDIP)



NOTES:

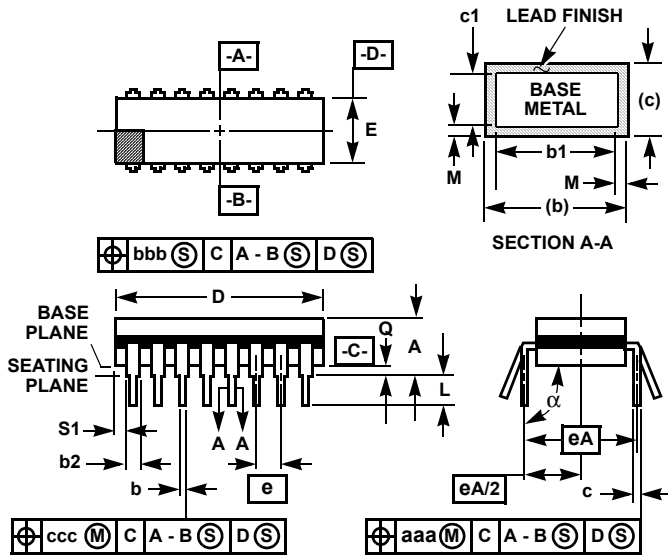
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum [-C-].
7. e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)  
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.300 BSC		7.62 BSC		6
e <sub>B</sub>	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

**Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**



**NOTES:**

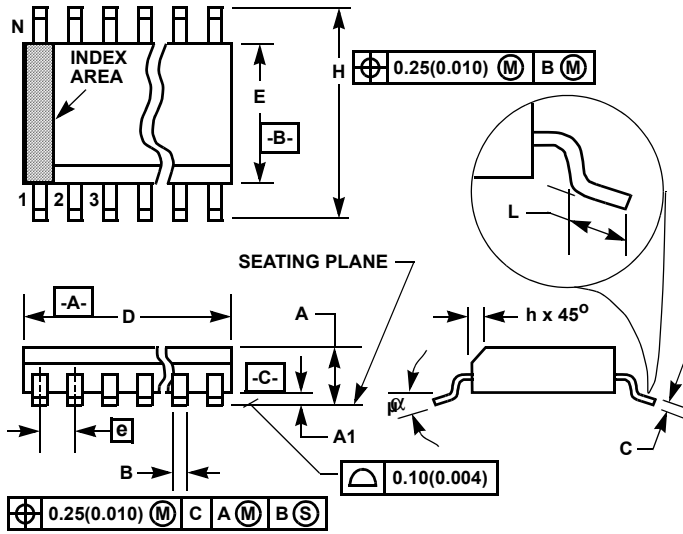
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)  
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
$\alpha$	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

**Small Outline Plastic Packages (SOIC)**



**M14.15 (JEDEC MS-012-AB ISSUE C)  
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)