

**Radiation Hardened 8-Bit Bidirectional CMOS/TTL Level Converter**

The Intersil HS-3374RH is a radiation hardened 8-bit bidirectional level converter designed to interface CMOS logic levels with TTL logic levels in radiation hardened bus oriented systems. The HS-3374RH is fabricated using a radiation hardened EPI-CMOS process and features eight parallel bidirectional buffer/level converters.

Two control inputs, ENABLE and DISABLE, are used to determine the direction of data flow, and to set both the in puts and outputs in the high impedance state. The control inputs may be driven by either TTL or CMOS logic drivers capable of sinking one standard TTL load.

The HS-3374RH is a non-inverting version of the industry standard CD40116. The non-inverting outputs of the HS-3374RH reduce PC board chip count by eliminating the need to restore data back to a non-inverted format.

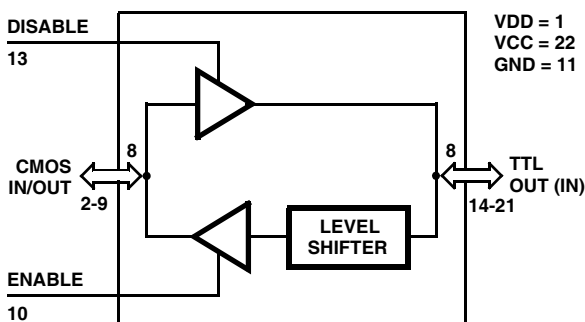
**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.**

**Detailed Electrical Specifications for these devices are contained in SMD 5962-96786. A "hot-link" is provided on our homepage for downloading.**  
[www.intersil.com/spacedefense/space.asp](http://www.intersil.com/spacedefense/space.asp)

**Ordering Information**

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962R9678601QWC	HS1-3374RH-8	-55 to 125
5962R9678601VWC	HS1-3374RH-Q	-55 to 125

**Functional Diagram**



**Features**

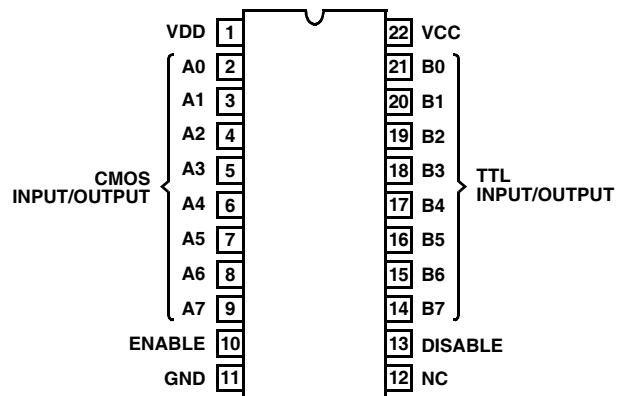
- Electrically Screened to SMD # 5962-96786
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardened EPI-CMOS
  - Total Dose . . . . . 1 x 10<sup>5</sup>RAD(Si)
  - Latch-Up Immune . . . . . >1 x 10<sup>12</sup>RAD(Si)/s (Note 1)
- Low Propagation Delay Time
  - Typical CMOS to TTL Pre-RAD . . . . . 40ns
  - Typical CMOS to TTL Post 100KRAD . . . . . 40ns
  - Typical TTL to CMOS Pre-RAD . . . . . 50ns
  - Typical TTL to CMOS Post 100KRAD . . . . . 50ns
- Low Standby Power
- +10V CMOS and +5V TTL Power Supply Inputs
- Eight Non-Inverting Three-State Input/Output Channels
- No External TTL Input Pull-Up Resistors Required
- High TTL Sink Current
- Equivalent to Sandia SA2996
- Military Temperature Range . . . . . -55°C to 125°C

**NOTE:**

1. For operation at 10V and transient levels above 1 x 10<sup>10</sup>RAD(Si)/s, please refer to Application Note 401.

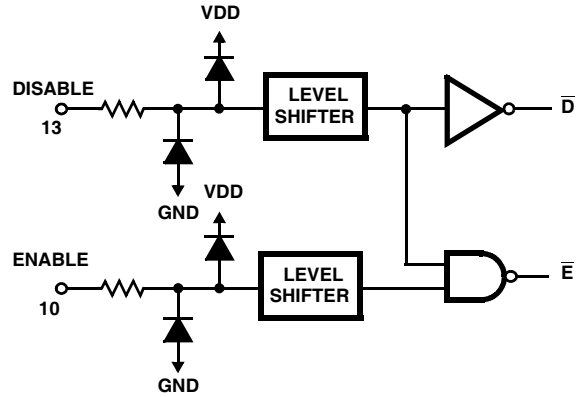
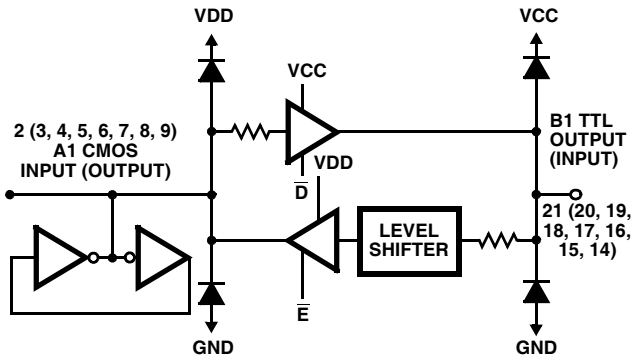
**Pinout**

**HS-3374RH  
MIL-STD-1835, CDIP2-T22  
(SBDIP)  
TOP VIEW**



Functional Block Diagram

1 OF 8 IDENTICAL CIRCUITS



NOTES:

- 2. Enable and disable are TTL type inputs
- 3. D and E outputs are common to all 8 channels

INPUT (OUTPUT)		OUTPUT (INPUT)	
DATA	TERMINAL NUMBER	DATA	TERMINAL NUMBER
A0	2	B0	21
A1	3	B1	20
A2	4	B2	19
A3	5	B3	18
A4	6	B4	17
A5	7	B5	16
A6	8	B6	15
A7	9	B7	14

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

0 = Low Level 1 = High Level X = Don't Care  
Z = High Impedance on Both CMOS and TTL sides.

NOTE: An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-3374RH pins: A0 - 7.

The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of  $\pm 1.5\text{mA}$  at  $V_{DD}/2 \pm 0.5\text{V}$  for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

WARNING: Do not activate the Disable input by hardwiring to any TTL input pins. This is an incorrect mode of operation.

**Die Characteristics**

**DIE DIMENSIONS:**

89.4 mils x 76.0 mils x 14 mils ±1 mil

**INTERFACE MATERIALS:**

**Glassivation:**

Type: SiO<sub>2</sub>  
 Thickness: 11kÅ ±2kÅ

**Top Metallization:**

Type: AlSi  
 Thickness: 8kÅ ±1kÅ

**Substrate:**

Radiation Hardened Silicon Gate,  
 Dielectric Isolation

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

Unbiased (DI)

**Metallization Mask Layout**

