High-Voltage Ring Generator

Ordering Information

Operating Voltage	Package Options		
V _{NN1}	SOW-16		
-220V	HV450WG		

Features

- Integrated high voltage transistors
- 67V_{RMS} ring signal
- Output over current protection
- Can drive external MOSFETs for larger loads

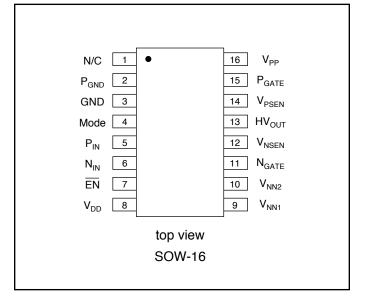
Applications

- High voltage ring generator
- □ Set-top/Street box ring generator
- D Pair gain ring generator

General Description

The Supertex HV450 is a PWM high voltage ring generator. The high voltage output P- and N-channel transistors are controlled independently by the logic inputs P_{IN} and N_{IN}. For application where a single control pin (N_{IN}) is desired, the mode pin should be connected to Gnd. This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on N_{IN} will turn the high voltage P-Channel on and the N-Channel off. The outputs can drive up to 5 RENs. The HV450 can drive external MOSFETs for applications requiring larger loads. The IC can be powered down by connecting the enable pin to V_{DD}. The high voltage outputs have pulse by pulse over current protection.

Pin Configuration



V_{NN2}, N-channel gate voltage supply V_{DD}, logic supply

Absolute Maximum Ratings*

Storage temperature
Power dissipation

V_{NN1}, power supply voltage

V_{PP}, P-channel gate voltage supply

* All voltages referenced to ground

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-240V

-20V

+7.5V

600mW

V_{NN1}+20V

-65°C to +150°C

Electrical Characteristics

(Over operating supply voltages unless otherwise specified, T_{A} = -40 $^{\circ}C$ to +85 $^{\circ}C.)$

Symbol	Parameters	Min	Тур	Max	Unit	Conditions
V _{PP}	P-channel linear regulator output voltage	-10		-18	V	
V _{NN1}	High voltage negative supply	- 220		-110	V	
V _{NN2}	Negative linear regulator output voltage	V _{NN1} + 6.0		V _{NN1} + 10.0	V	
V _{DD}	Logic supply voltage	4.5		5.5	V	
I _{NN1Q}	V _{NN1} quiescent current		300	500		$P_{IN} = N_{IN} = \overline{EN} = L$
				25	μA	$P_{IN} = N_{IN} = L, \overline{EN} = H$
I _{DDQ}	V _{DD1} quiescent current		90	200	μΑ	$P_{IN} = N_{IN} = \overline{EN} = L$
			35	100		$P_{IN} = N_{IN} = L, \overline{EN} = H$
I _{NN1}	V _{NN1} operating current		1.4		mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz
I _{DD}	V _{DD} operating current			1.0	mA	
I	Mode logic input low current		25		μΑ	Mode = 0V
V _{IL}	Logic input low voltage	0		1.0	V	$V_{DD} = 5.0 V$
V _{IH}	Logic input high voltage	4.0		5.0	V	$V_{DD} = 5.0 V$

High Voltage Output

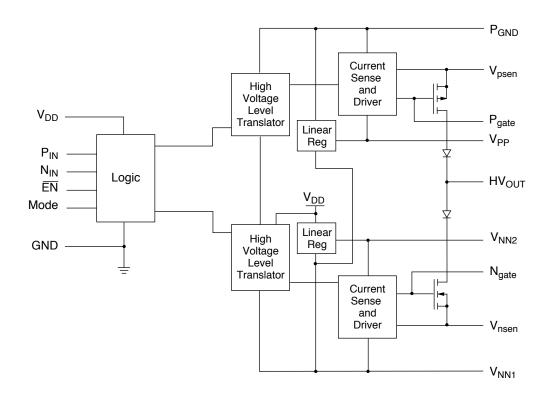
Symbol	Parameters	Min	Тур	Max	Unit	Conditions
R _{SOURCE}	V _{OUT} P source resistance		65		Ω	I _{OUT} = 100mA
R _{SINK}	V _{OUT} P sink resistance		65		Ω	I _{OUT} = -100mA
t _{d(ON)}	HV _{OUT} delay time		150		ns	P_{IN} = high to low, Mode = high
t _{rise}	HV _{OUT} rise time		50		ns	P _{IN} = high to low
t _{d(OFF)}	HV _{OUT} delay time		200		ns	N_{IN} = low to high, Mode = high
t _{fall}	HV _{OUT} fall time		50		ns	N _{IN} = low to high
t _{db}	Logic deadband time		250		ns	Mode = low
V _{psen}	HV _{OUT} current source sense voltage	-1.2		-0.8	V	
V _{nsen}	$\mathrm{HV}_{\mathrm{OUT}}$ current sink sense voltage	V _{NN1} + 0.8		V _{NN1} + 1.2	V	
t _{shortP}	HV _{OUT} off delay time when current source sense is activiated		70	150	ns	
t _{shortN}	HV _{OUT} off delay time when current sink sense is activated		70	150	ns	
t _{whout}	Minimum pulse width for $\mathrm{HV}_{\mathrm{OUT}}$ at $\mathrm{P}_{\mathrm{GND}}$			500	ns	
t _{wlout}	Minimum pulse width for $\mathrm{HV}_{\mathrm{OUT}}$ at $\mathrm{V}_{\mathrm{NN1}}$			500	ns	

Truth Table

N _{IN}	P _{IN}	Mode	EN	HV _{OUT}
L	L	Н	L	Pgnd
L	Н	Н	L	High Z
H*	L*	Н	L	*
Н	Н	Н	L	V _{NN1}
L	Х	L	L	V _{NN1}
Н	Х	L	L	Pgnd
Х	Х	Х	Н	High Z

*This state will short $\mathrm{V}_{_{\mathrm{NN1}}}$ to Pgnd and should therefore be avoided.

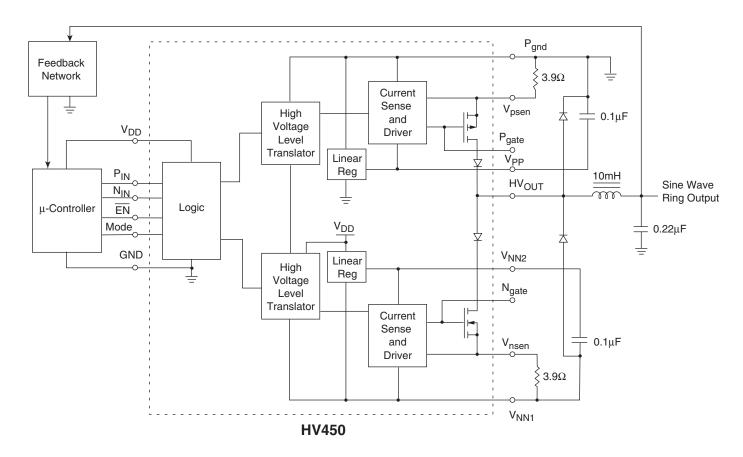
Block Diagram



Pin Description

V _{PP}	P-channel gate voltage supply. Generated by an internal linear regulator. A 0.1μ F capacitor should be connected between P_{GND} and V_{PP} .
V _{NN1}	Negative high voltage supply.
V _{NN2}	N-channel gate voltage supply. Generated by an internal linear regulator. A $0.1\mu F$ capacitor should be connected between V_{NN2} and $V_{NN1}.$
V _{DD}	Logic supply voltage.
GND	Low voltage ground.
P _{GND}	High voltage power ground.
P _{IN}	Logic control input. When mode is high, logic input high turns OFF output high voltage P-Channel.
N _{IN}	Logic control input. When mode is high, logic input high turns ON output high voltage N-Channel.
EN	Logic enable input. Logic low enables IC.
Mode	Logic mode input. Logic low activates 200nsec deadband. When mode is low, N_{IN} turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to V_{DD} or ground.
HV _{OUT}	High voltage output. Voltage swings from P_{GND} to V_{NN1} .
V _{psen}	Pulse by pulse over current sensing for P-Channel MOSFET.
V _{nsen}	Pulse by pulse over current sensing for N-Channel MOSFET.
P _{gate}	Gate drive for external P-channel MOSFET.
N _{gate}	Gate drive for external N-channel MOSFET.

Typical Application Circuit



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