High Voltage Liquid Crystal Shutter Driver

Ordering Information

Device	HV _{IN} Maximum Voltage	Package Options
		SO-8
HV508	45V	HV508LG

Features

- □ HVCMOS[®] technology for high performance
- Logic-selectable output voltage
- 100nF drive capability
- □ Up to 90V_{P-P}
- 25µs response time

General Description

The Supertex HV508 is a 45V liquid crystal shutter driver in an SO-8 surface mount package. It consist of two outputs that provide square waves of opposite phase. The liquid crystal shutter is connected between the two outputs. Its equivalent load can be approximated as a resistor in parallel with a capacitor. Minimum resistance is $1.0M\Omega$ and maximum capacitance is 0.1μ F.

The HV508 has three input supply voltages, HV_{IN}, LV_{IN}, and V_{DD}. The output's amplitude will be either LV_{IN} or HV_{IN}. A logic high on the HV_{EN} input will set the output to operate from the HV_{IN} supply. A logic low on the HV_{EN} input will set the output to operate from the LV_{IN} supply. The output frequency is set by the logic input frequency applied on the POL input.

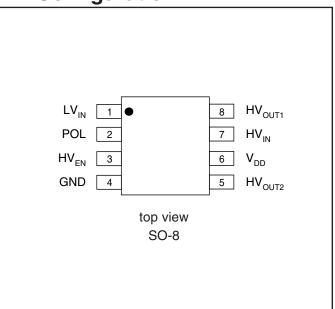
Absolute Maximum* Ratings

HV _{IN} , high voltage input	+60V
LV _{IN} , low voltage input	+7.5V
V _{DD} , logic supply voltage	+12V
Continuous total power dissipation	700mW
Operating temperature	-5°C to +60°C
Storage temperature	–65°C to +150°C
Soldering temperature	+300°C

* All voltages are referenced to GND.

For operation above 25°C ambient derate linearly at 6mW/°C.

Pin Configuration



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Electrical Characteristics

DC Electrical Characteristics (over operating supply voltages unless otherwise specified, $T_A = -5^{\circ}C$ to $+60^{\circ}C$)

Symbol	Parameter	Min	Тур	Мах	Unit	Conditions
I _{HVQ}	HV _{IN} quiescent current			10	μΑ	
I _{LVQ}	LV _{IN} quiescent current			10	μΑ	
IDDQ	V _{DD} quiescent current			10	μΑ	
I _{HV}	HV _{IN} operating current			2.8	mA	$\begin{array}{l} POL = 100Hz, \ HV_{EN} = high, \\ T_A = 25^{\circ}C, \ Load = 1M\Omega \ in \ parallel \\ with \ 0.1\mu F \ between \ HV_{OUT1} \ and \\ HV_{OUT2} \end{array}$
I _{LV}	LV _{IN} operating current			380	μA	$\begin{array}{l} POL = 100Hz, \ HV_{EN} = low, \\ T_A = 25^{\circ}C, \ Load = 1M\Omega \ in \ parallel \\ with \ 0.1\mu F \ between \ HV_{OUT1} \ and \\ HV_{OUT2} \end{array}$
IL	Logic input current low	-5			μA	
I _{IH}	Logic input current high			5.0	μA	
C _{LOAD}	Output capacitive load*	0		0.25	μF	C_{LOAD} in parallel with a 1M $\!\Omega$ resistor

*The device can operate continuously without any damage within this range. AC limits are not implemented.

AC Electrical Characteristics (HV_{IN} = 45V, LV_{IN} = 6V, V_{DD} = 5V, T_A = -5°C to +60°C)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions
f _{POL}	POL input frequency	0		100	Hz	
t _{HV(ON)}	Turn-on time when high voltage is enable			16	μS	Load = $1M\Omega$ in parallel with 0.1μ F between HV _{OUT1} and HV _{OUT2} .
$t_{\rm HV(OFF)}$	Turn-off time when high voltage is enabled			16	μS	$HV_{EN} = High.$ Outputs rise to HV_{IN} . See Fig. 1.
t _{LV(ON)}	Turn-on time when high voltage is disabled			40	μS	Load = $1M\Omega$ in parallel with 0.1μ F between HV _{OUT1} and HV _{OUT2} .
$t_{\text{LV}(\text{OFF})}$	Turn-off time when high voltage is disabled			6.0	μs	$HV_{EN} = Low.$ Outputs rise to LV_{IN} . See Fig. 1.
t _{EN(ON)}	Turn-on time from HV_{EN} to HV_{OUT}			25	μs	Load = $1M\Omega$ in parallel with $0.1\mu F$ between HV_{OUT1} and HV_{OUT2} . See Fig. 2.

Recommended Operating Conditions

Symbol	Parameter	Min	Тур	Max	Unit
V _{DD}	Logic supply voltage	5.0		10.0	V
LV _{IN}	Low output supply voltage	3.0		6.0	V
HV _{IN}	High output supply voltage	5.0		45	V
V _{IL}	Logic input voltage low	0		$0.3V_{DD}$	V
V _{IH}	Logic input voltage high	$0.7V_{DD}$		V _{DD}	V
T _A	Ambient Temperature	-5.0		+60	°C

Notes:

Power-up sequence should be the following:

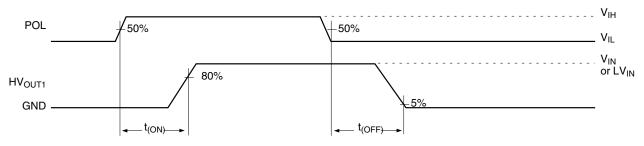
1. Connect GND, V_{DD} , logic inputs, HV_{IN} , and LV_{IN} .

Power-down sequence should be the reverse of the above.

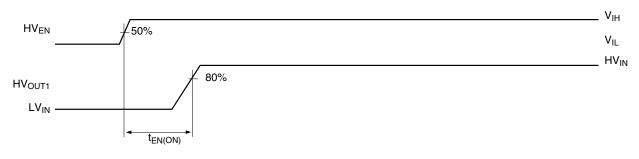
Truth Table

HV	POL	HV _{OUT1}	HV_{OUT2}
Н	Н	HV _{IN}	GND
Н	L	GND	HV _{IN}
L	Н	LV	GND
L	L	GND	LV

Timing Diagram

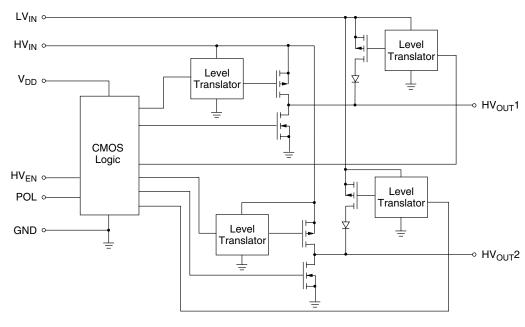








Block Diagram





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