Intel® i960® RM/RN/RS I/O Processor

Specification Update

September 4, 2001

Notice: The 80960RM/RN/RS processor may contain design defects or errors known as errata. Characterized errata that may cause the product's behavior to deviate from pubished specifications are documented in this specification update.

Order Number: 273164-020

Contents

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Revision History

Date	Version	Description
08/22/01	020	Added Document Changes 71 through 73.
04\04\01	019	Added Document Change 70.
03/2001	018	Revised Document Change 59. Added Document Changes 67, 68 and 69.
06/27/00	017	Added Document Change #66. Revised "Device ID Registers" on page 15, changed Bridge and ATU C-0 stepping values.
05/10/00	016	Modified Documentation Changes #8, #50, #55, #56, #59, #60, #61, #62 and #63 (Design Guide and Datasheet revised to include previous Documentation Changes). Added Documentation Changes #64 and #65.
04/04/00	015	Added Errata #14. Added Document Changes #57, #58, #59, #60, #61, #62 and #63. Removed Document Change #6, duplicate of #7. Changed Document Change #7 to #6. Covered same issue as old #6, but text gives clearer explanation.
3/15/00	014	Modified and added data to the Die Details table. Added Documentation changes #53, #54, #55, and #56.
2/04/00	013	Corrected stepping information in the *Summary Table of Changes* section. Added "C-0" stepping and marked Specification Changes #12 and 13 for this stepping only.
1/17/00	012	Added Topside Markings for the i960® RS I/O processor. Added information to the Die Details table. Added information to the Device ID Registers table. Added Specification Change #12, 13. Added Documentation Changes #51, #52. Removed documentation changes referencing changes to the *i960® RM I/O Processor Datasheet* and the *i960® RN I/O Processor Datasheet.* These changes were incorporated into the datasheets.
12/08/99	011	Added Errata #11, 12, 13. Added Specification Change #10, 11. Added Documentation Changes #46, #47, #48, #49, #50. Removed documentation changes referencing the schematics in the *i960® RM/RN I/O Processor Design Guide*; these changes were previously incorporated into the document.
8/11/99	010	Added Specification Change #9. Modified Documentation Change #12. Added Documentation Changes#41, #42, #43, #44, #45.
7/14/99	009	Modified Specification Change #7. Added Specification Change #8. Added Documentation Changes #39 and #40.
6/7/99	008	Added Documentation Change #38.
5/18/99	007	Added Die Details table under Markings section. Added Errata #10. Added Specification Change #7. Added Documentation Change #37.

Date	Version	Description
04/09/99	006	Added the following Specification Changes: #5 and #6, Modified the following Specification Changes: #1, #2, #3 and #4, Added the following Documentation Changes: #8 through #36.
03/11/99	005	Added Specification Change #4. Added Specification Clarification #3.
02/23/99	004	Added the following Errata: #9. Modified the following Errata: #7. Modified the following Specification Clarifications: #1, #2. Added the following Documentation Changes: #2, through #6.
01/20/99	003	Added the following Errata: #7 and #8. Added the following Specification Changes: #1 through #3. Added the following Documentation Change: #1.
01/13/99	002	Added the following Specification Clarifications: #1 and #2.
8/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
i960® RM/RN I/O Processor Developer's Manual	273158
80960RM I/O Processor Data Sheet	273156
80960RN I/O Processor Data Sheet	273157
i960® RM/RN I/O Processor Design Guide	273139

Nomenclature

Errata are design defects or errors. These may cause the Intel® i960® RM/RN/RS I/O Processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® i960® RM/RN/RS I/O Processor product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	Errata
	A-0	B-0	C-0			
1	X	X	X	16	NoFix	The ATU Discard Timer Status Bit in ATUCR Gets Set Even Though Delayed Read/Write Completes Before Discard Timer Expires
2	X	X	X	16	NoFix	A Target Abort Occurs on the Internal Bus when Target Abort Passing from the Internal Bus to the PCI Buses through the ATUs is Disabled
3	X	X	X	17	NoFix	After Initialization, Changing the Configuration Cycle Retry Bit in the EBCR to Retry Configuration Cycles while they are Occurring can Cause Data Corruption
4	X	X	X	17	NoFix	A Target Abort from the Internal Bus may be Reported to the PCI Bus, Without the Target Abort Being Returned
5	X	X	X	17	NoFix	Secondary Interrupts are Routed to the Core Processor, Rather than the Primary PCI Bus, as their Default
6	X	X	X	18	NoFix	Secondary IDSEL Select Register (SISR) Bits are in Reverse Order
7	X			19	Fixed	Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the DMA Channels The four case illustrations on page 19 have been changed.
8	X			20	Fixed	Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the Application Accelerator Unit
9	X			21	Fixed	In battery backup mode, data corruption occurs if a write to SDRAM is coincident with the assertion of P_RST#
10	X	X	X	21	NoFix	The Primary ATU (PATU) will, under certain circumstances, do Slow Decode Timing
11	X	X	X	21	NoFix	Potential Bridge Lockup Condition if Back to Back Exclusive Accesses are Used
12	X	X	X	21	NoFix	I^2C Busy Bit in ISR (0x1684) Is Active Only When I^2C Unit is Enabled
13	X	X	X	22	NoFix	Single-bit and Multi-bit Error Reporting Cannot Be Individually Enabled by ECC Control Register
13	X	X	X	22	NoFix	Single-bit and Multi-bit Error Reporting Cannot Be Individually Enabled by ECC Control Register
14	X	X	X	22	NoFix	A 32-bit ATU Write, When Retried, Always Will Retry as a 64-bit Write.

Specification Changes

No.	Steppings			Page	Status	Specification Changes
	A-0	B-0	C-0			
1		X		23	Fixed	Default Value of the Memory Controller's Refresh Frequency Register (RFR)
2		X		23	Fixed	Resetting the Memory Controller's SDRAM Output Buffers during the Power-Fail Sequence
3		X		23	Fixed	PCI-to-PCI Bridge Configuration Registers: Bridge Subsystem Vendor ID Register (BSVIR) and Bridge Subsystem ID Register (BSIR)
4	X	X		23	Fixed	PCI Local Bus Specification, Revision 2.2
5.		X		23	Fixed	PCI Bus Power Management Interface Specification, Revision 1.1
6.		X		23	Fixed	Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)
7.		X		23	Fixed	Default Value of the Primary Inbound ATU Limit Register (PIALR)
8.		X		24	Fixed	CompactPCI Hot Swap Specification, Revision 1.0
9.		X		24	Fixed	PCI-to-PCI Bridge Architecture Specification, Revision 1.1
10.		X		24	Fixed	128Mbit SDRAM Support
11.		X		24	Fixed	New Spec: (T_{LOCK}) for 80960RM/RN Internal PLL
12.			X	24	Fixed	Support for 3.3 Volt PCI Signalling
13.			X	24	Fixed	Summary of 80960RS

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	A-0	B-0	C-0			
1	X			25	Doc	Hooking up the SDRAM Clock Enable Inputs on the SDRAM DIMM for Non- Battery-Backup Applications
2	X			25	Doc	Hooking up the SDRAM Clock Enable Outputs (SCKE0 and SCKE1) from the i960® RM/RN I/O Processor to the Clock Enable Inputs on the SDRAM DIMM in a Battery-Backup Application
3	X	X	X	25	Doc	HALT Mode is Not Supported

Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	273158-001	28	Doc	Section 12.3.1 of the i960® RM/RN I/O Processor Developer's Manual
2	273158-001	28	Doc	Section 8.5.4 of the i960® RM/RN I/O Processor Developer's Manual
3	273158-001	29	Doc	Section 13.4 of the i960® RM/RN I/O Processor Developer's Manual
4	273158-001	29	Doc	Section 13.5.1 of the i960® RM/RN I/O Processor Developer's Manual
5	273158-001	29	Doc	Section 15.1 of the i960® RM/RN I/O Processor Developer's Manual
6	273158-001	30	Doc	Section 15.2.1.2 of the i960® RM/RN I/O Processor Developer's Manual
7	273158-001	30	Doc	Section 11.3.1.3 of the i960® RM/RN I/O Processor Developer's Manual
8	273139-001	30	Revised	Section 4.2.2 of the i960® RM/RN I/O Processor Design Guide
9	273158-001	30	Doc	Documentation change in the i960® RM/RN I/O Processor Developer's Manual
10	273158-001	30	Doc	Section 14.15 in the i960® RM/RN I/O Processor Developer's Manual
11	273158-001	31	Doc	Section 14.15 in the i960® RM/RN I/O Processor Developer's Manual
12	273158-001	32	Doc	Section 14.15 in the i960® RM/RN I/O Processor Developer's Manual
13	273158-001	33	Doc	Section 14.15 in the i960® RM/RN I/O Processor Developer's Manual
14	273158-001	33	Doc	Section 14.15 in the i960® RM/RN I/O Processor Developer's Manual
15	273158-001	35	Doc	Section 14.15.4 in the i960® RM/RN I/O Processor Developer's Manual
16	273158-001	36	Doc	Section 14.15.21 in the i960® RM/RN I/O Processor Developer's Manual
17	273158-001	36	Doc	Section 14.15.22 in the i960® RM/RN I/O Processor Developer's Manual
18	273158-001	36	Doc	Section 14.15.22 in the i960® RM/RN I/O Processor Developer's Manual
19	273158-001	36	Doc	Section 14.15.24 of the i960® RM/RN I/O Processor Developer's Manual
20	273158-001	37	Doc	Section 14.15.26 of the i960® RM/RN I/O Processor Developer's Manual
21	273158-001	38	Doc	Section 14.15.34 of the i960® RM/RN I/O Processor Developer's Manual
22	273158-001	40	Doc	Section 14.15.34 of the i960® RM/RN I/O Processor Developer's Manual
23	273158-001	41	Doc	Section 14.15.34 of the i960® RM/RN I/O Processor Developer's Manual
24	273158-001	42	Doc	Section 14.15.34 of the i960® RM/RN I/O Processor Developer's Manual

Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
25	273158-001	43	Doc	Section 15.7 of the i960® RM/RN I/O Processor Developer's Manual
26	273158-001	43	Doc	Section 15.7 of the i960® RM/RN I/O Processor Developer's Manual
27	273158-001	44	Doc	Section 15.7 of the i960® RM/RN I/O Processor Developer's Manual
28	273158-001	46	Doc	Section 15.7 of the i960® RM/RN I/O Processor Developer's Manual
29	273158-001	47	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
30	273158-001	49	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
31	273158-001	50	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
32	273158-001	51	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
33	273158-001	52	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
34	273158-001	53	Doc	Section 15.7.4 of the i960® RM/RN I/O Processor Developer's Manual
35	273158-001	54	Doc	Section 15.7.34 of the i960® RM/RN I/O Processor Developer's Manual
36	273158-001	56	Doc	Section 15.7.44 of the i960® RM/RN I/O Processor Developer's Manual
37	273158-001	57	Doc	Section 15.7.20, Table 15-49
38	273158-001	57	Doc	Section 15.7 of the i960® RM/RN I/O Processor Developer's Manual
39	273158-001	58	Doc	Section 3.5.1, page 3-11
40	273158-001	58	Doc	Section 13.2.3, page 13-8
41	273158-001	58	Doc	Section 12.3.1, page 12-4
42	273158-001	58	Doc	Section 11.2.8, page 11-5
43	273158-001	58	Doc	Section 14.15 Bridge Configuration Header Bottom Address Offset 60H
44	273158-001	59	Doc	Power Management Control/Status Register - PMCSR (address 106C)
45	273158-001	60	Doc	PMCSR PCI to PCI Bridge Support - PMCSR_BSE
46	273158-001	61	Doc	128Mbit SDRAM Technology
47	273158-001	61	Doc	64 Bit Operation
48	273158-001	62	Doc	Scrubbing
49	273158-001	64	Doc	I^2C Reset Condition/Lockup
50	273139-001	64	Revised	New PCI Clock Buffer
51	273158-001	64	Doc	Section 13.6.4 SDRAM Boundary Register 0 - SBR0
52	273158-001	64	Doc	Section 13.6.5 SDRAM Boundary Register 1- SBR1
53	273158-001	64	Doc	Section 13.2.3 Flash Write Cycle (pg 13-8)

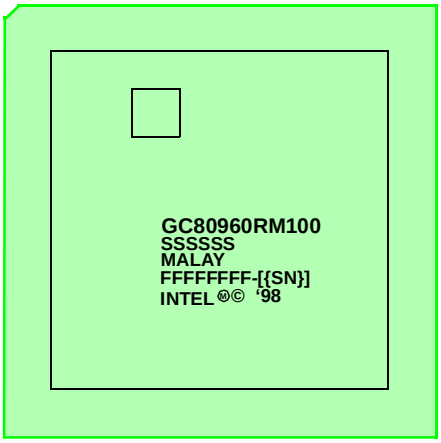
Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
54	273158-001	64	Doc	Section 11.5 Device Identification on Reset
55	273139-001	65	Revised	Table 21, line 7, Symbol "V_{OH1}", Notes Section Next to I_{OH} = -200uA (3) Add Note (6)
56	273139-001	65	Revised	Section 5.0, pg 54, Last Sentence of the First Paragraph
57	273158-001	65	Doc	Section 13.4.1.2, System Assumptions
58	273158-001	65	Doc	Section 13.4.1.2, System Assumptions
59	273139-001	65	Revised	Section 8.0, Table 8-12, 80960RM Signals Requiring Pull-Up/Down Resistors
60	273139-001	65	Revised	Section 9.5, VCCPLL Pins Requirement
61	273139-001	65	Revised	Section 10.2, Bulk Decoupling Capacitance
62	273139-001	66	Revised	Section 14.1, Thermal Recommendations
63	273156-004 273157-004 273328-001	66	Revised	Section 4.3, VCCPLL Pins Requirement
64	273158-001	66	Doc	Section 14.15.2 of the i960® RM/RN I/O Processor Developer's Manual
65	273158-001	67	Doc	Section 15.7.2 of the i960® RM/RN I/O Processor Developer's Manual
66	273158-001	67	Doc	Section 12.2.2 Bus Control Register - BCON of the i960® RM/RN I/O Processor Developer's Manual
67	273158-001	68	Doc	Section 7.0 of the i960® RM/RN I/O Processor Design Guide
68	273158-001	68	Doc	Section 8.0 of the i960® RM/RN I/O Processor Design Guide
69	273158-001	68	Doc	Section 8.0, Table 8-12. of the i960® RM/RN I/O Processor Design Guide
70	273158-001	68	Doc	Section 11.3.1.5 FAIL# Code of the i960® RM/RN I/O Processor Developer's Manual
71	273158-001	68	Doc	Table 13-13, page 13-31 of the i960® RM/RN I/O Processor Developer's Manual
72	273158-001	68	Doc	Section 13.3.7.3 of the i960® RM/RN I/O Processor Developer's Manual
73	273158-001	68	Doc	Section 13.3.7.3 of the i960® RM/RN I/O Processor Developer's Manual

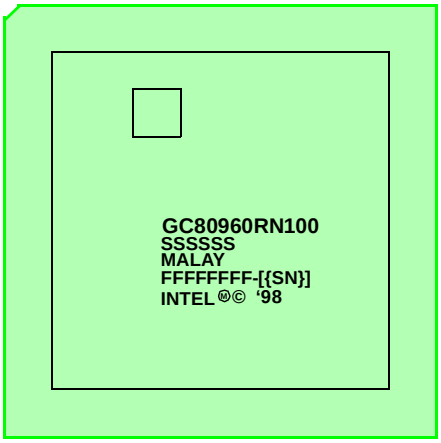
Identification Information

Markings

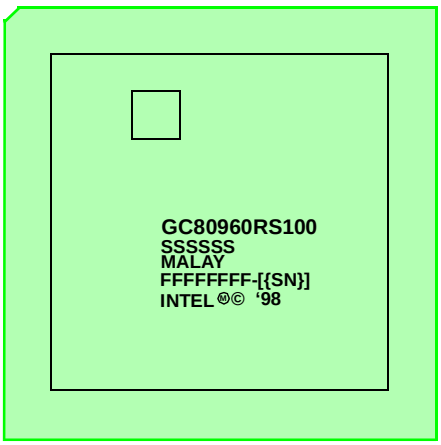
Topside Markings



80960RM



80960RN



80960RS

Die Details

Part Number	Stepping	QDF/ Spec Number	Voltage (V)	i960® Core Processor Speed (MHz)	Notes
GC80960RN100	A-0	Q 120	3.3	100	Samples - limited testing
GC80960RM100	A-0	Q 121	3.3	100	Samples - limited testing
GC80960RN100	A-0	SL37Y	3.3	100	Production*
GC80960RN100	A-0	SL3FM	3.3	100	Production*
GC80960RM100	A-0	SL39Q	3.3	100	Production*
GC80960RN100	B-0	Q 136	3.3	100	Samples - limited testing
GC80960RM100	B-0	Q 137	3.3	100	Samples - limited testing
GC80960RN100	B-0	Q 126	3.3	100	Samples - limited testing
GC80960RM100	B-0	Q 127	3.3	100	Samples - limited testing
GC80960RN100	B-0	SL3G6	3.3	100	Production*
GC80960RM100	B-0	SL3G7	3.3	100	Production*
GC80960RM100	C-0	Q173	3.3	100	Samples - limited testing
GC80960RM100	C-0	Q162	3.3	100	Samples - limited testing
GC80960RN100	C-0	Q160	3.3	100	Samples - limited testing
GC80960RN100	C-0	Q161	3.3	100	Samples - limited testing
GC80960RS100	C-0	Q174	3.3	100	Samples - limited testing
GC80960RM100	C-0	SL3YZ	3.3	100	Production
GC80960RN100	C-0	SL3YW	3.3	100	Production
GC80960RS100	C-0	SL3ZJ	3.3	100	Production

Note: For A-0 and B-0 step RM and RN, the S-spec was not printed on the die.

Device ID Registers

Device and Stepping	Processor Device ID Register (PDIDR - 0x1710)	PCI-to-PCI Bridge Unit Revision ID (RIDR - 0x1008)	Address Translation Unit Revision ID Register (ATURID - 0x1208)	i960® Core Processor Device ID (DEVICEID - 0xFF00 8710)
80960RM A-0	08863013	0x0	0x0	00823013
80960RN A-0	08862013	0x0	0x0	00823013
80960RM B-0	18863013	0x01	0x01	00823013
80960RN B-0	18862013	0x01	0x01	00823013
80960RM C-0	28863013	0x02	0x02	00823013
80960RN C-0	28862013	0x02	0x02	00823013
80960RS C-0	28867013	0x02	0x02	00823013
NOTE: The Processor ID registers for A-0 were incorrect in the Revision 5 of the *i960® RM/RN I/O Processor Specification Update*.				

Errata

1. The ATU Discard Timer Status Bit in ATUCR Gets Set Even Though Delayed Read/Write Completes Before Discard Timer Expires

Problem: The ATU Discard Timer Status bit (bit 15, in the Address Translation Unit Configuration Register, local bus address 1288H) is getting set even though the transaction completed correctly. This scenario occurs when a single-word delayed read or write is completing on the PCI bus through either the primary ATU or the secondary ATU at the same time that the discard timer is timing out. This should not affect multi-word transactions, but should occur with all configuration reads and writes that line up with the discard timer time-out.

Implication: Although the discard timer time-out bit is being set, the transaction is completing properly, so the only implication here is the handling of any actions that occur as a result of the discard timer being set.

Workaround: Software that handles the discard timer status bit, should just reset the ATU Discard Timer Status bit (bit 15, in the Address Translation Unit Configuration Register, local bus address 1288H) in this scenario. The likelihood of seeing the problem is reduced if the timer value is set to 2^{15}.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

2. A Target Abort Occurs on the Internal Bus when Target Abort Passing from the Internal Bus to the PCI Buses through the ATUs is Disabled

Problem: If a target abort occurs on the Internal Bus due to an ECC error, and target abort passing from the internal bus to the PCI busses is disabled, the ATU can deadlock when all the following conditions are true:

- The PCI master must be a 32-bit master
- The PCI master induces data-to-data wait states
- A target abort occurs on the internal bus
- The Primary (bit 0, in the Primary ATU Interrupt Mask Register, local bus address 12BCH) or Secondary (bit 0, in the Secondary ATU Interrupt Mask Register, local bus address 12C0H) ATU ECC Target Abort Enable bit is clear.

Implication: Under these conditions the relevant ATU will not pass the target abort back to the PCI master, and the ATU will enqueue subsequent read transactions, but will never return data. The discard timer will not rescue this case, since pointers have been corrupted.

Workaround: Always set The Primary ATU ECC Target Abort Enable bit (bit 0, in the Primary Interrupt Mask Register, local bus address 12BCH) and the Secondary ATU ECC Target Abort ENable bit (bit 0, in the Secondary Interrupt Mask Register, local bus address 12C0H) to allow the ATUs to pass the target abort back to the PCI master.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

3. After Initialization, Changing the Configuration Cycle Retry Bit in the EBCR to Retry Configuration Cycles while they are Occurring can Cause Data Corruption

Problem: After initialization, if the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Configuration Register, local bus address 1040H) is changed to retry configurations cycles at the same time that a configuration read completion is starting on the primary PCI bus, the ATU will return data, but will not dequeue it.

Implication: Under the above conditions, if another read of the same address were to occur, the old, stale data in the queue would be returned to the master.

Workaround: Do not change the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Configuration Register, local bus address 1040H) after initialization.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

4. A Target Abort from the Internal Bus may be Reported to the PCI Bus, Without the Target Abort Being Returned

Problem: If a target abort occurs on the internal bus before the 'primary' Memory Enable Bit (bit 1, in the Primary ATU Command Register, local bus address 1204H) is cleared, or the 'secondary' Memory Enable Bit (bit 1, in the Secondary ATU Command Register, local bus address 1298H) is cleared, the target abort will be reported incorrectly in the ATU error registers, when the transaction master aborts on the relevant PCI bus. Furthermore, the transaction will be dequeued.

Implication: If the memory enables are turned back on, the original target abort will be lost. Also, if enabled, this WILL generate an interrupt to the core.

Workaround: Ensure that the queues in the ATUs are cleared before changing the Memory Enable Bit (bit 1, in the Primary ATU Command Register, local bus address 1204H) or the Memory Enable Bit (bit 1, in the Secondary ATU Command Register, local bus address 1298H) after initialization.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

5. Secondary Interrupts are Routed to the Core Processor, Rather than the Primary PCI Bus, as their Default

Problem: The secondary interrupts (S_INTA#, S_INTB#, S_INTC#, and S_INTD#) are routed to the 80960RM/RN core processor as their default. They should be routed to the primary PCI bus as their default.

Implication: When booting in configuration mode 0, cards located on the secondary PCI bus will have their interrupts routed to the i960 core processor and may not function correctly in the system.

Workaround: Boot the processor in Mode 3 (Default Mode), and set the S_INTA# Select Bit, S_INTB# Select Bit, S_INTC# Select Bit, and S_INTD# Select Bit (Bits 3:0, in the PCI Interrupt Routing Select Register, local bus address 1050H) in the initialization software. Then make sure to clear the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Control Register, local bus address 1040H) to allow the bridge and the ATU to accept configuration cycles. If the system must boot in mode 0, these bits can be modified by an external agent on the PCI bus by using PCI configuration cycles.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

6. Secondary IDSEL Select Register (SISR) Bits are in Reverse Order

Problem: The bits in the Secondary IDSEL Select Register (SISR) are in reverse order. Refer to Table "SISR Bit Mapping" on page 18 for the bit descriptions.

SISR Bit Mapping

Bit Number	Description
Bit 09	AD16 IDSEL Disable
Bit 08	AD17 IDSEL Disable
Bit 07	AD18 IDSEL Disable
Bit 06	AD19 IDSEL Disable
Bit 05	AD20 IDSEL Disable
Bit 04	AD21 IDSEL Disable
Bit 03	AD22 IDSEL Disable
Bit 02	AD23 IDSEL Disable
Bit 01	AD24 IDSEL Disable
Bit 00	AD25 IDSEL Disable

Implication: When private devices are being used on the secondary side and the SISR is programmed without taking the bit reversal into account, the private devices may not be hidden from the host. In addition, public devices may be hidden from the host.

Workaround: Program the SISR with the new bit mapping as described above.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

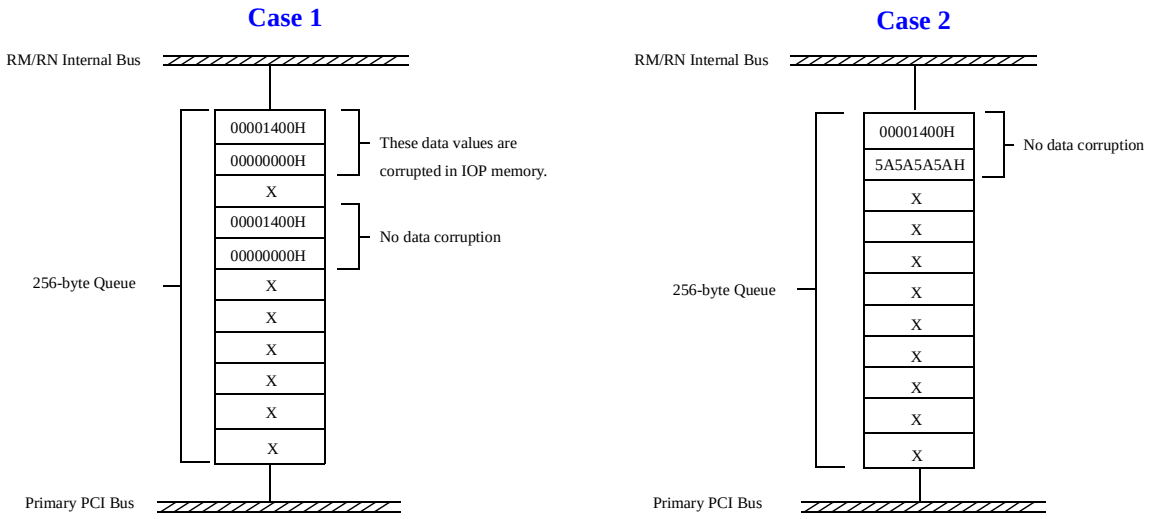
7. Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the DMA Channels

Problem: This problem appears across all 3 DMA channels: DMA Ch-0, Ch-1, and Ch-2. If the transfer data value falls within the MMR address range of the active DMA channel (1400H - 143FH for Ch-0, 1440H - 147FH for Ch-1, and 1480H - 14FFH for Ch-2), data corruption will occur.

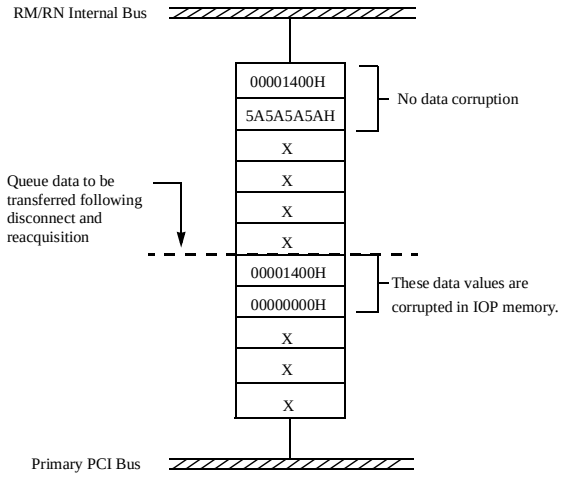
Examples on page 19 describe the error condition.

Assumption: DMA channel 0 is used to transfer data from PCI to IOP memory.

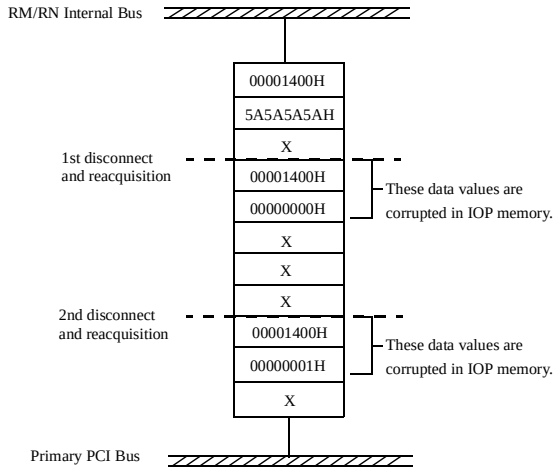
Single Transaction on the Internal Bus



Case 3: Two Transactions on the Internal Bus (one disconnect)



Case 4: Three Transactions on the Internal Bus (two disconnects)



Implication: Data corruption results when the data value matches the MMR address range of the active DMA channel.

Workaround: There are two possible workarounds for this errata:

- Use the Primary Address Translation Unit (PATU) to transfer data from Primary PCI to IOP memory and Secondary Address Translation Unit (SATU) to transfer data from Secondary PCI to IOP memory.
- Configure the Memory Controller Unit to execute in 32-bit mode. For further information, refer to Section 13.3.3 on page 13-14 of the *i960® RM/RN I/O Processor Developer's Manual* and to Table 4 in the 80960RM/RN I/O processor datasheets.

Status: Fixed. A change intended to fix this erratum was implemented in the B-0 stepping.

8. Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the Application Accelerator Unit

Problem: If the transfer data value falls within the MMR address range of the Application Accelerator Unit (1800H - 18FFH), data corruption will occur.

Implication: Data corruption results when the data value matches the MMR address range of the Application Accelerator Unit.

Workaround: There are two possible workarounds for this errata:

- Compute the XOR Parity calculation through software by using the i960® JT processor.
- Configure the Memory Controller Unit to execute in 32-bit mode. For further information, refer to Section 13.3.3 on page 13-14 of the *i960® RM/RN I/O Processor Developer's Manual* and to Table 4 in the 80960RM/RN I/O processor datasheets.

Status: Fixed. A change intended to fix this erratum was implemented in the B-0 stepping.

9. In battery backup mode, data corruption occurs if a write to SDRAM is coincident with the assertion of P_RST#

Problem: When operating the RM/RN in battery backup mode, the last qword of data will be corrupted if P_RST# is pulled while writing to SDRAM.

Implication: The last write into SDRAM contains corrupted data.

Workaround: A workaround may be possible but is application specific. This only affects customers that use battery backup memory (See Section 13.4, page 13-34 of the RM/RN Developer's Manual)

Status: Fixed. A change intended to fix this erratum was implemented in the B-0 stepping.

10. The Primary ATU (PATU) will, under certain circumstances, do Slow Decode Timing

Problem: In general, the primary ATU uses Medium decode timing. However, when the messaging unit is enabled and the inbound or outbound message ports are hit with a 64-bit access, the PATU will need to pre-decode the C/BE# bus. As a result, the PATU claims the access using slow decode timing.The *PCI Local Bus Specification*, Revision 2.2 requires this field of the PATUSR (bits 10:9) to indicate the slowest DEVSEL# timing possible.

Implication: If a subtractive decode agent is present on the PATUs bus segment and has been programmed to accept all slow decode transactions, there is a possibility of contention on the PCI bus between the subtractive decode agent and the PATU.

Workaround: Subtractive decode agents that share the PCI bus with the PCI primary bus interface of the i960® RM/RN should not be programmed to claim transactions with slow decode timing.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

11. Potential Bridge Lockup Condition if Back to Back Exclusive Accesses are Used

Problem: If a device on the primary PCI bus attempts to do two back-to-back exclusive accesses through the i960RM/RN processor, with an ATU/DMA transfer occurring immediately after the first exclusive access, the bridge may not unlock properly.

Implication: The bridge will lock up, causing no further transactions across the bridge.

Workaround: A workaround may be possible but is application specific.

This affects customers that use back-to-back exclusive accesses.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

12. I^2C Busy Bit in ISR (0x1684) Is Active Only When I^2C Unit is Enabled

Problem: Bit 3 of the I^2C Status register (ISR) described in Table 22-10 of the *i960® RM/RN I/O Processor Developer's Manual* only gets updated when the I^2C unit is enabled on the i960® RM/RN processor.

Implication: The I^2C bus must be idle before enabling the I^2C unit on the i960® RM/RN processor or a potential lockup condition may occur on the I^2C bus. The I^2C busy bit was used as the method used to check the status of the I^2C bus. Since this is inactive when the I^2C unit is disabled, it is not a reliable gauge of the status of the I^2C bus.

Workaround: The developer is advised to find another means of determining the status of the I^2C bus, perhaps using external logic.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

13. Single-bit and Multi-bit Error Reporting Cannot Be Individually Enabled by ECC Control Register

Problem: The ECC Control Register ECCR is described as having the ability to select multi-bit error and/or single-bit error reporting (see Table 13-24 on page 13-50 of the *i960® RM/RN I/O Processor Developer's Manual*). However, the algorithm does not allow individual enabling; that is, the reporting is either on or off for both multi-bit and single bit error reporting.

Implication: The error reporting selection (enabled or disabled) will apply to both multi-bit and single-bit errors.

Workaround: There is no current workaround. If either the ECCR.0 bit or the ECCR.1 bit is selected for reporting, then both multi-bit and single-bit error reporting are enabled. If neither bit is selected for reporting, then both multi-bit and single-bit error reporting are disabled.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

14. A 32-bit ATU Write, When Retried, Always Will Retry as a 64-bit Write.

Problem: A performance optimization in the 80960 RM/RN ATU sometimes causes a normal 64-bit write to be executed as two, 32-bit writes. If the first 32-bit write gets retried, it always will retry as a 64-bit write.

Implication: While there are no issues with this in practice, the PCI local bus specification states that all retries must be repeated exactly.

Workaround: None required.

Status: NoFix. See the Table "Summary Table of Changes" on page 8.

Specification Changes

1. Default Value of the Memory Controller's Refresh Frequency Register (RFR)

Issue: The Refresh Frequency Register (RFR) will default to the value 00H. The desired value of the RFR will need to be specified during the SDRAM initialization sequence/routine.

Status: Fixed. This change has been fixed in the B-0 stepping.

2. Resetting the Memory Controller's SDRAM Output Buffers during the Power-Fail Sequence

Issue: SDRAM output buffers will be reset to the default value (low-drive strength) after the power-fail sequence has executed with the current buffer strength configuration.

Status: Fixed. This change has been fixed in the B-0 stepping.

3. PCI-to-PCI Bridge Configuration Registers: Bridge Subsystem Vendor ID Register (BSVIR) and Bridge Subsystem ID Register (BSIR)

Issue: To guarantee compliance with the PCI-to-PCI Bridge Architecture Specification Rev 1.0, the Bridge Subsystem Vendor ID Register (BSVIR@PCI configuration offset 34H) and the Bridge Subsystem ID Register (BSIR@PCI configuration offset 36H) will be specified to be reserved in the configuration address space. Configuration software should therefore not write to these reserved locations.

Status: Fixed. This change has been fixed in the B-0 stepping.

4. *PCI Local Bus Specification*, Revision 2.2

Issue: The 80960RM/RN I/O processor is compliant with the *PCI Local Bus Specification*, Revision 2.2.

Status: Fixed. This change has been fixed in the B-0 stepping.

5. PCI Bus Power Management Interface Specification, Revision 1.1

Issue: The 80960RM/RN B-0 stepping is compliant with the *PCI Bus Power Management Interface Specification, Revision 1.1*. See the Documentation section of this document and the *ACPI Implementation White paper* for specific changes related to this compliance.

Status: Fixed. This change has been fixed in the B-0 stepping.

6. Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)

Issue: The 80960RM/RN I/O processor B-0 stepping is compliant with the *Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)*. See the Documentation section of this document and the *ACPI Implementation White paper* for specific changes related to this compliance.

Status: Fixed. This change has been fixed in the B-0 stepping.

7. Default Value of the Primary Inbound ATU Limit Register (PIALR)

Issue: In the A-0 stepping of the i960 RM/RN I/O processor, the Primary ATU Limit Register (PIALR) had a default value of FFFFEH which corresponded to an inbound window of 8KB. To ease Flash programming, the ATU limit register was changed to a value of FF0000H which corresponds to a window of 16MB.

Status: Fixed. This change has been fixed in the B-0 stepping.

8. CompactPCI Hot Swap Specification, Revision 1.0

Issue: The i960 RM/RN I/O processor B-0 stepping meets the criteria to be considered a CompactPCI Hot Swap “capable” device.

Status: Fixed. This change has been fixed in the B-O stepping.

9. PCI-to-PCI Bridge Architecture Specification, Revision 1.1

Issue: The 80960 RM/RN I/O processor B-0 stepping is compliant with the *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1.

Status: Fixed. This change has been fixed in the B-O stepping.

10. 128Mbit SDRAM Support

Issue: Table 13-6 of the i960 RM/RN I/O Processor Developer’s Manual, lists the supported SDRAM configurations. The table only lists 16Mbit and 64Mbit SDRAM technology.

Status: Fixed. The 80960 RM/RN (A and B steppings) will support 128 Mbit SDRAM with some qualifications. Refer to the spec update documentation changes section for specifics on using 128 Mbit SDRAM on the 80960 RM/RN.

11. New Spec: (T_{LOCK}) for 80960RM/RN Internal PLL

Issue: A new specification, T_{LOCK}, is being added to the 80960 RM/RN data sheet. Table 4-6 of the PCI Local Bus Specification and the PCI Hot-Plug Specification states that $T_{RST-CLK}$ time, the time from a stable PCI clock to RST# going high should be a minimum of 100 us. If a board design intends to implement the minimum time, the 80960 RM/RN would have to lock its internal PLL in less than 100 us. In addition, since the 80960 RM/RN requires a clock buffer for secondary PCI clocks, the combined PLL lock times for the clock buffer and the 80960 RM/RN PLLs need to be less than 100 us. While current board/chip set designs typically have $T_{RST-CLK}$ times in the range of several hundred ms, specifically stating this specification may aid board designers for future designs.

Status: Fixed. T_{LOCK} (max) for 80960RM/RN (A and B steppings) is specified at 65 us.

12. Support for 3.3 Volt PCI Signalling

Issue: The C-X stepping of the 80960 RM/RN/RS now supports 3.3 Volt PCI signalling.

Status: Fixed. This change has been implemented on the C-X steppings of the 80960 RM/RN/RS

13. Summary of 80960RS

Issue: The C-X stepping of the 80960 RX silicon includes the 80960 RS. This new processor is a 32 bit PCI device, similar to the 80960 RM but without an application accelerator (AAU).

Status: Fixed. This new processor will be introduced with the C-X stepping.

Specification Clarifications

1. Hooking up the SDRAM Clock Enable Inputs on the SDRAM DIMM for Non-Battery-Backup Applications

Problem: During the power-up reset sequence, as the RM/RN supply voltage ramps to 3.3 Volts, a glitch occurs on the Clock Enable pins (SCKE) to the SDRAM at around 2 Volts. Occasionally this causes the SDRAM to enter a pseudo, self-refresh mode which causes a lock-up condition on the SDRAM device. The only way to clear this condition is to power-down the SDRAM. The SDRAM initialization sequence will not clear the lock-up condition.

Workaround: Tie the Clock Enable Inputs on the SDRAM DIMM to V_{CC}.

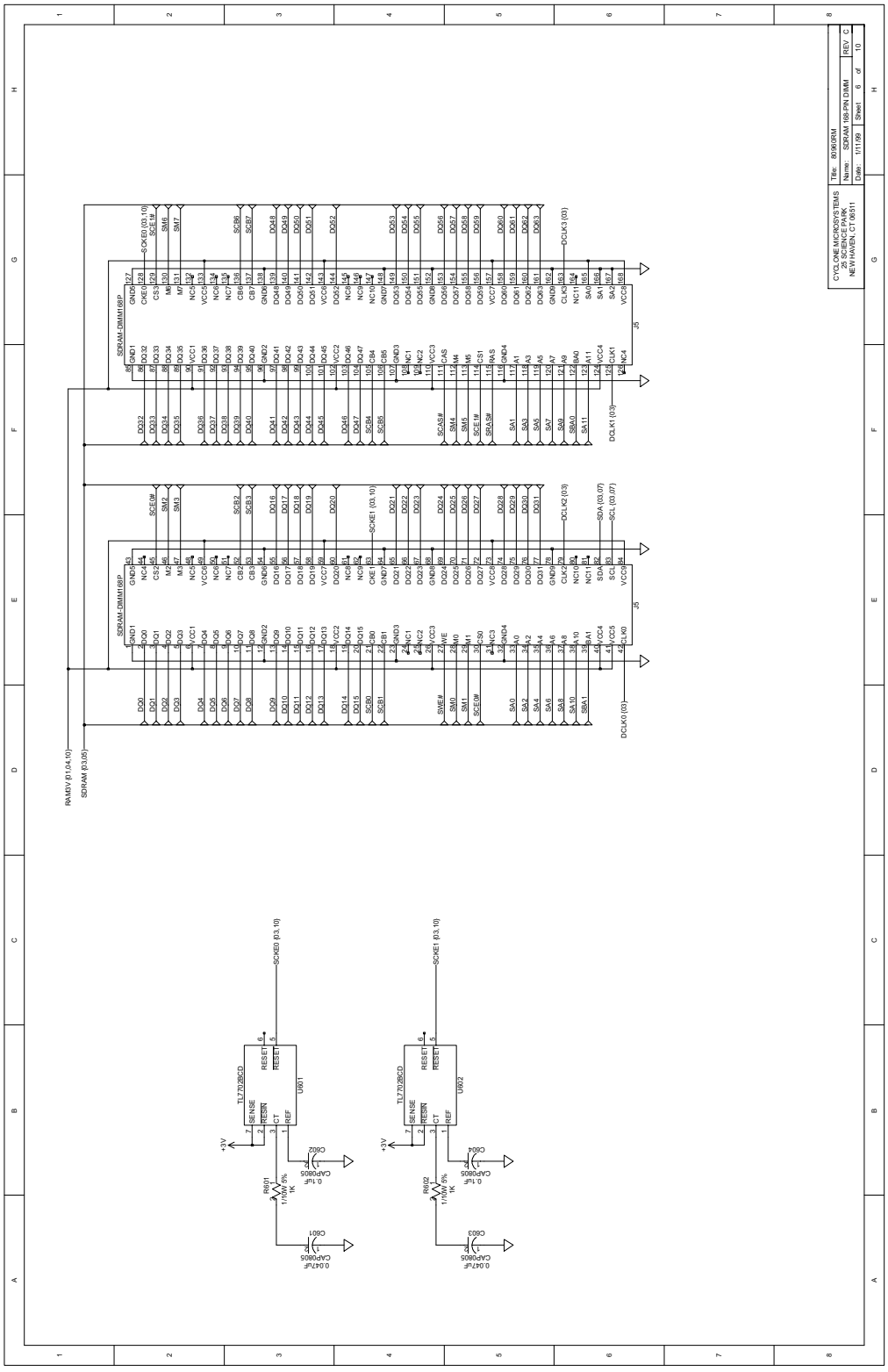
2. Hooking up the SDRAM Clock Enable Outputs (SCKE0 and SCKE1) from the i960® RM/RN I/O Processor to the Clock Enable Inputs on the SDRAM DIMM in a Battery-Backup Application

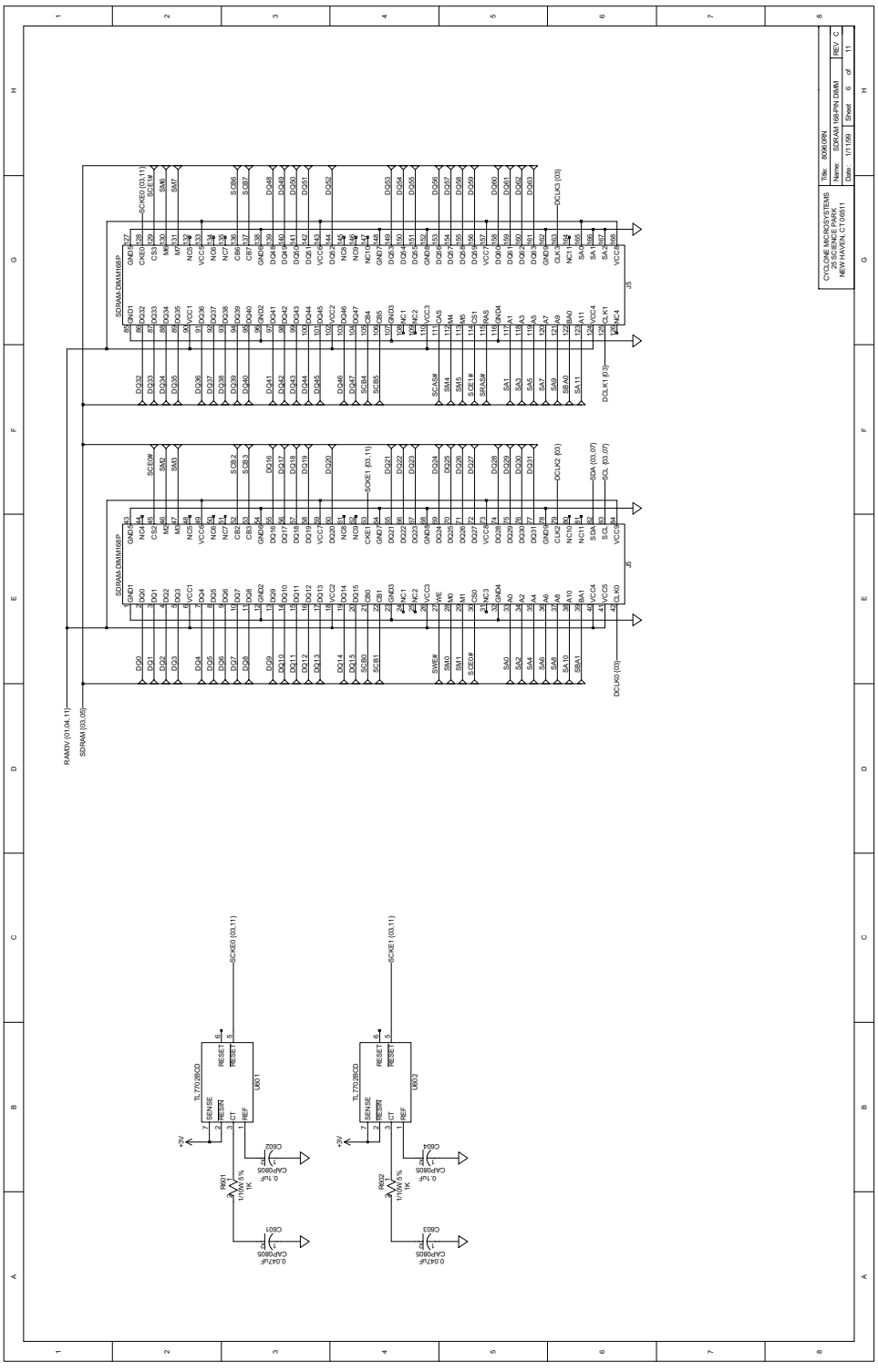
Problem: During the power-up reset sequence, as the RM/RN supply voltage ramps to 3.3 Volts, a glitch occurs on the Clock Enable pins (SCKE) to the SDRAM at around 2 Volts. Occasionally this causes the SDRAM to enter a pseudo, self-refresh mode which causes a lock-up condition on the SDRAM device. The only way to clear this condition is to power-down the SDRAM. The SDRAM initialization sequence will not clear the lock-up condition.

Workaround: Ensure that the Clock Enable Inputs to the SDRAM DIMM are held low during power-up. An example workaround is shown in the following circuit schematics and was tested on the i960RM/RN evaluation boards (Sheet 6 – 80960RM schematics and Sheet 6 – 80960RN schematics in *i960® RM/RN I/O Processor Design Guide*).

3. HALT Mode is Not Supported

Issue: Although the product manual lists 'HALT' as a valid instruction, the 80960RM/RN I/O processor does not support HALT mode. HALT mode is not validated and tested, therefore, we cannot guarantee proper operation.





Documentation Changes

1. Section 12.3.1 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: The last sentence of the third paragraph has been changed to:

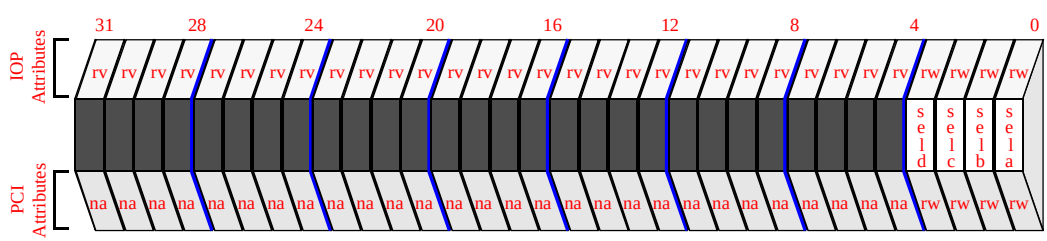
- Old:
  Logical Memory Mask register (LMMSK).
- New:
  Logical Memory Mask register (LMMR).

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

2. Section 8.5.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 8-21 has been changed to match errata #5 in this spec update. In the description column, the bits were swapped. See Table 8-21.

Table 8-21 PCI Interrupt Routing Select Register (PIRSR)



80960 Core internal bus address
0000 1050H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA= Not Accessible

Bit	Default	Description
31:4	0	Reserved (initialize to 0)
3	0	**S_INTD#** Select Bit - PIRSR, xsel (0) Interrupt routed to 80960 core interrupt controller input (XINT3#) (1) Interrupt routed to P_INTD# pin
2	0	**S_INTC#** Select Bit - PIRSR, xsel (0) Interrupt routed to 80960 core interrupt controller input (XINT2#) (1) Interrupt routed to P_INTC# pin
1	0	**S_INTB#** Select Bit - PIRSR, xsel (0) Interrupt routed to 80960 core interrupt controller input (XINT1#) (1) Interrupt routed to P_INTB# pin
0	0	**S_INTA#** Select Bit - PIRSR, xsel (0) Interrupt routed to 80960 core interrupt controller input (XINT0#) (1) Interrupt routed to P_INTA# pin

NOTE: Please check the *i960® RM/RN I/O Processor Specification Update* for possible issues with the PIRSR.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

3. Section 13.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: The note on page 13-34 has been removed.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

4. Section 13.5.1 of the *i960® RM/RN I/O Processor Developer's Manual*

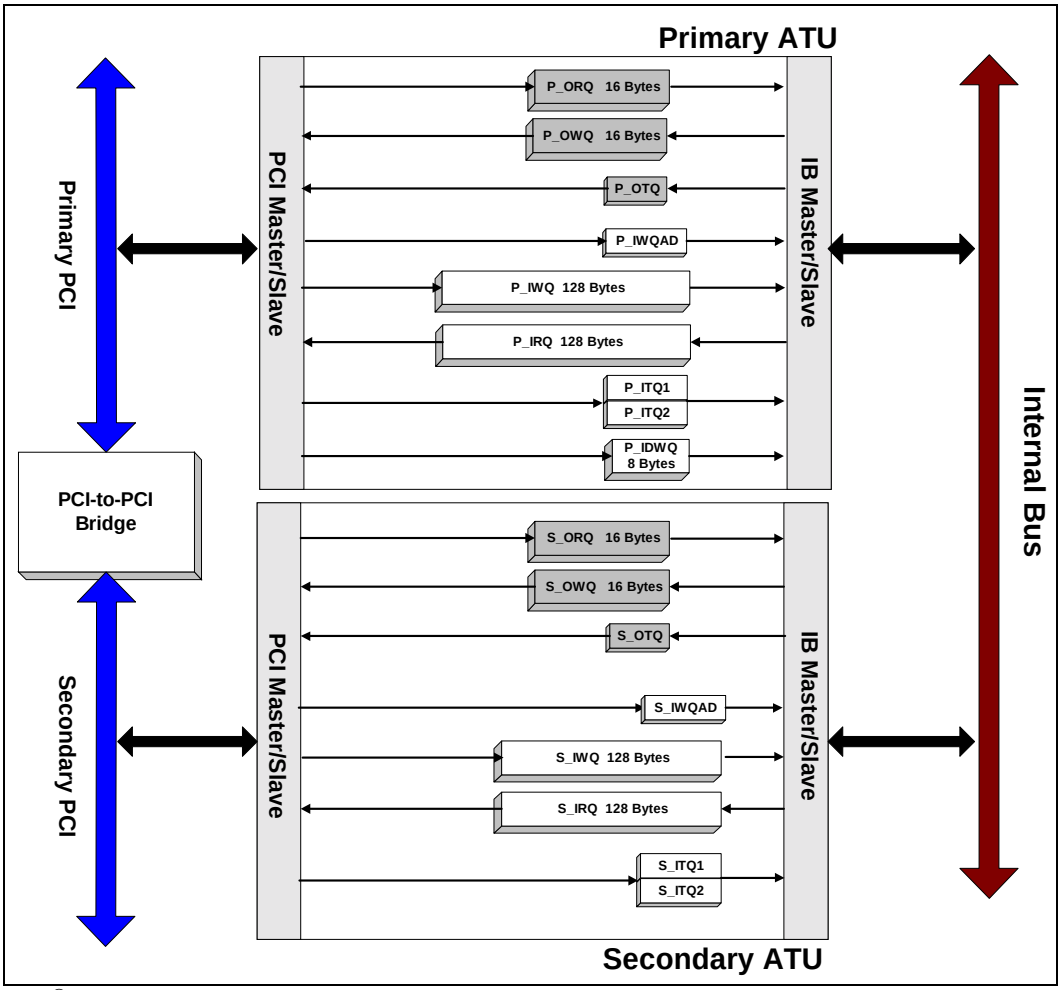
Issue: The second to last paragraph on page 13-40 ("ESTAT, ECARx...") has been removed.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

5. Section 15.1 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Figure 15-2 on page 15-3 has been changed. The arrows in the box containing P_IRQ 128 Bytes have been reversed. See Figure 15-2.

Figure 15-2. ATU Queue Architecture Block Diagram



Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

6. Section 15.2.1.2 of the *i960® RM/RN I/O Processor Developer's Manual*

In the section describing "Data flow for the inbound write transaction on the internal bus..."

The first bulleted paragraph has been changed to:

- The ATU internal bus master requests the internal bus, when the IWQAD/IWQ contains the PCI address and data for the current transaction, which has crossed at least a 2 QWORD boundary or, a PCI address from an earlier posted PCI transaction has moved to the head of the IWQAD.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

7. Section 11.3.1.3 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Figure 11-3 of the user's manual shows three cycle times that need to be updated for the 80960RM/RN processors. The following timings are approximations:

- Built-In Self-Test: ~138,000 cycles
- Built-In Self-Test Status: ~10 cycles
- 80960 Local Bus Confidence Test: ~44 cycles

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

8. Section 4.2.2 of the *i960® RM/RN I/O Processor Design Guide*

Issue: Table 4-6 (pg. 13) has been changed to:

Manufacturer	Part Number
Cypress	CY2310NZPVC-1
Motorola	MPC9140SD
Pericom	P16C182
Pericom	P16C180V

Affected Docs: *i960® RM/RN I/O Processor Design Guide*

Status: ***Design Guide revised.***

9. Documentation change in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: All references to PCI Local Bus specification, revision 2.1 have been changed to PCI Local Bus specification, revision 2.2.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

10. Section 14.1 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Bullet numbers 1 and 3 have been changed.

Bullet 1 should read:

- "Full compliance to the *PCI Local Bus Specification* Revision 2.2"

Bullet 3 should read:

- Full Compliance to the *PCI Bus Power Management Interface Specification* Revision 1.1
  - Defines the PCI hardware support required by the Advanced Configuration and Power Interface Specification, Revision 1.0 initiative

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

11. Section 14.15 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: The following paragraph has been added between the 1st and 2nd paragraphs of the section:

The bridge has a 9 byte extended configuration space residing at configuration offset 68H that supports the Advanced Configuration and Power Interface Specification, Revision 1.0 by providing the Power Management registers defined by the *PCI Bus Power Management Interface Specification* Revision 1.1

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*)

12. Section 14.15 in the *i960® RM/RN I/O Processor Developer's Manual*

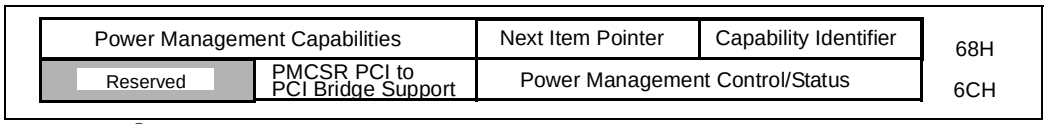
Issue: Figure 14-11 should be replaced with the following changed figure. (Change is highlighted)

Bridge Configuration Header				PCI Address Offset	
Device ID		Vendor ID		00H	
Primary Status		Primary Command		04H	
Class Code			Revision ID	08H	
Reserved	Header Type	Primary Latency Timer	Cacheline Size	0CH	
Reserved				10H 14H	
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18H	PCI to PCI Bridge
Secondary Status		I/O Limit	I/O BASE	1CH	
Memory Limit		Memory Base		20H	
Prefetchable Memory Limit		Prefetchable Memory Base		24H	
Reserved				28H 2CH 30H	
Reserved		Reserved	Capabilities Pointer	34H	
Reserved				38H	
Bridge Control		Reserved		3CH	
Secondary IDSEL Control		Extended Bridge Control		40H	
Primary Bridge Interrupt Status				44H	
Secondary Bridge Interrupt Status				48H	
Secondary Arbitration Control				4CH	i960 RM/RN Specific
PCI Interrupt Routing Control				50H	
Reserved		Secondary I/O Limit	Secondary I/O BASE	54H	
Secondary Memory Limit		Secondary Memory Base		58H	
Queue Control		Secondary Decode Enable		5CH	
Reserved				60H	

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

13. Section 14.15 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new figure has been added after Figure 14-11, "Extended Bridge Configuration Header Format."



Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

14. Section 14.15 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 14-23 should read: (New registers have been added.)

Internal Bus Address	Section, Register Name - Acronym (Page)
1000H	Section 14.15.1, "Vendor Identification Register - VIDR" on page 14-74
1002H	Section 14.15.2, "Device ID Register - DIDR" on page 14-75
1004H	Section 14.15.3, "Primary Command Register - PCR" on page 14-76
1006H	Section 14.15.4, "Primary Status Register - PSR" on page 14-77
1008H	Section 14.15.5, "Revision ID Register - RID" on page 14-78
1009H	Section 14.15.6, "Class Code Register - CCR" on page 14-78
100CH	Section 14.15.7, "Cacheline Size Register - CLSR" on page 14-79
100DH	Section 14.15.8, "Primary Latency Timer Register - PLTR" on page 14-80
100EH	Section 14.15.9, "Header Type Register - HTR" on page 14-81
1018H	Section 14.15.10, "Primary Bus Number Register - PBNR" on page 14-82
1019H	Section 14.15.11, "Secondary Bus Number Register - SBNR" on page 14-83
101AH	Section 14.15.12, "Subordinate Bus Number Register - SubBNR" on page 14-84
101BH	Section 14.15.13, "Secondary Latency Timer Register - SLTR" on page 14-85
101CH	Section 14.15.14, "I/O Base Register - IOBR" on page 14-86
101DH	Section 14.15.15, "I/O Limit Register - IOLR" on page 14-87
101EH	Section 14.15.16, "Secondary Status Register - SSR" on page 14-88
1020H	Section 14.15.17, "Memory Base Register - MBR" on page 14-89
1022H	Section 14.15.18, "Memory Limit Register - MLR" on page 14-90
1024H	Section 14.15.19, "Prefetchable Memory Base Register - PMBR" on page 14-91
1026H	Section 14.15.20, "Prefetchable Memory Limit Register - PMLR" on page 14-92
1034H	Capabilities Register Pointer - Cap_Ptr
103EH	Section 14.15.23, "Bridge Control Register - BCR" on page 14-94
1040H	Section 14.15.24, "Extended Bridge Control Register - EBCR" on page 14-97
1042H	Section 14.15.25, "Secondary IDSEL Select Register - SISR" on page 14-100
1044H	Section 14.15.26, "Primary Bridge Interrupt Status Register - PBISR" on page 14-102
1048H	Section 14.15.27, "Secondary Bridge Interrupt Status Register - SBISR" on page 14-104
104CH	Section 14.15.28, "Secondary Arbitration Control Register - SACR" on page 14-106
1050H	Section 14.15.29, "PCI Interrupt Routing Select Register - PIRSR" on page 14-106
1054H	Section 14.15.30, "Secondary I/O Base Register - SIOBR" on page 14-106
1055H	Section 14.15.31, "Secondary I/O Limit Register - SIOLR" on page 14-107

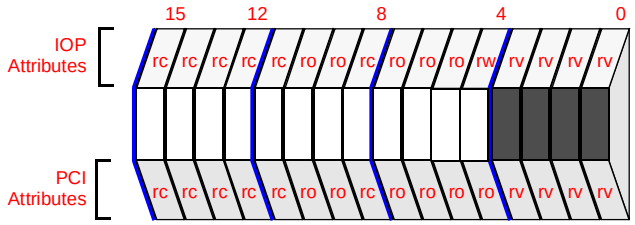
Internal Bus Address	Section, Register Name - Acronym (Page)
1058H	Section 14.15.32, “Secondary Memory Base Register - SMBR” on page 14-108
105AH	Section 14.15.33, “Secondary Memory Limit Register - SMLR” on page 14-109
105CH	Section 14.15.34, “Secondary Decode Enable Register - SDER” on page 14-110
105EH	Section 14.15.35, “Queue Control Register - QCR” on page 14-112
1060H	Reserved
1064H	Reserved
1068H	Capability Identifier Register - Cap_ID
1069H	Next Item Pointer Register - Next_Item_Ptr
106AH	Power Management Capabilities Register - PMCR
106CH	Power Management Control/Status Register - PMCSR
106EH	PMCSR PCI to PCI Bridge Support - PMCSR_BSE

Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

15. Section 14.15.4 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Figure 14-12 has been changed.

Bit 04 of the PSR is no longer reserved. It is now the "capabilities" bit - when set it this bit indicates the presence of extended capabilities, such as PCI power management. It it off by default for compatibility with legacy designs.



PCI Configuration Offset
06 - 07H

80960 Core Local Bus Address
0000 1006H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
15	0_2	Detected Parity Error - This bit is set when a parity error is detected during a data transfer on the primary bus even if parity handling is disabled. Set under the following conditions: • Write Data Parity Error when the Primary interface of the Bridge is a slave (downstream write). • Read Data Parity Error when the Primary interface of the Bridge is a master (upstream read). • Any Address Parity Error on the Primary Bus (including one generated by the Primary interface of the Bridge).
14	0_2	Signaled System Error - This bit is set if **P_SERR#** is asserted on the primary bus.
13	0_2	Master Abort - This bit is set whenever a transaction initiated by the bridge on the primary bus (except Special Cycles) ends in a Master-Abort.
12	0_2	Target Abort (master) - This bit is set whenever a transaction initiated by the primary interface ends in a Target-Abort
11	0_2	Target Abort (target) - This bit is set whenever the bridge, acting as a target, terminates the transaction on the primary bus with a Target-Abort.
10:09	01_2	**DEVSEL#** Timing - This indicates the primary interface uses Medium Decode timing.
08	0_2	Data Parity Error Detected - This bit is set when the bridge: • asserted **P_PERR#** (or saw asserted) on the primary bus • and was the master of the transaction when it occurred • and the Primary Parity Error Response bit is set in the PCR.
07	1_2	Fast Back-to-Back Capable - Indicates that the primary interface capable of accepting Fast Back-to-Back transactions as a target.
06	0_2	UDF Supported - User Definable Features are not supported
05	0_2	66 MHz. Capable - 66 MHz. operation is not supported.
04	0_2	**Capabilities** - When set, this function implements extended capabilities.
03:00	0000_2	Reserved

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

16. Section 14.15.21 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: The Bridge Subsystem Vendor ID Register (BSVIR) has been removed in the RM/RN B-0 stepping. This field is optional according to the *PCI Local Bus Specification* Revision 2.2.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

17. Section 14.15.22 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: The Bridge Subsystem ID Register (BSIR) has been removed in the RM/RN B-0 stepping. This field is optional according to the *PCI Local Bus Specification* Revision 2.2.

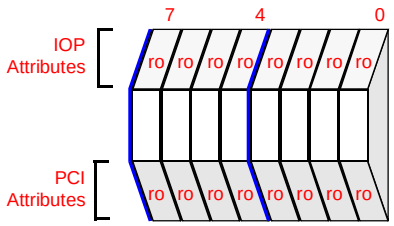
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

18. Section 14.15.22 in the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: Capabilities Pointer Register - Cap_Ptr (Address 1034H).

The Capabilities Pointer Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register provides an offset in this function's PCI Configuration Space for the location of the first item in the Capabilities linked list. In the case of the i960 RM/RN I/O processor, this is the PCI Bus Power Management extended capability as defined by the *PCI Bus Power Management Interface Specification* Revision 1.1.

Capabilities Pointer Register - Cap_Ptr



PCI Configuration Offset
34H

80960 Core Local Bus Address
0000 1034H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07:00	68H	Capability List Pointer - This provides an offset in this function's configuration space that points to the i960 RM/RN I/O processor's PCI Bus Power Management extended capability.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

19. Section 14.15.24 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 14-47.

Additional comments for bit 02:

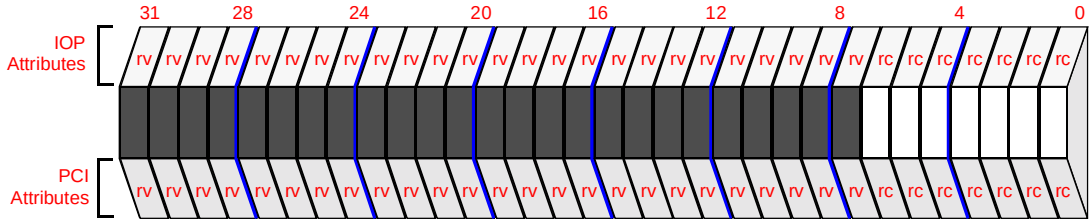
Bit 02 of this register should be cleared for ACPI configuration.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

20. Section 14.15.26 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 14-49 has been changed.

Bit 06 of this register is no longer reserved: it is now the "Power State Transition" bit.



PCI Configuration Offset
44 - 47H

80960 Core Local Bus Address
0000 1044H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

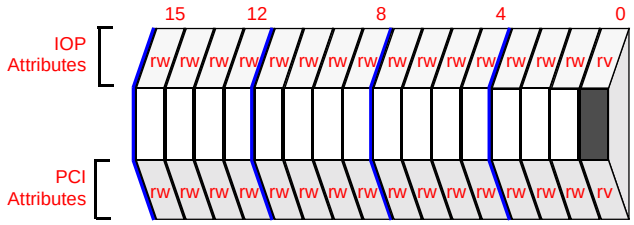
Bit	Default	Description
31:07	0000000H	Reserved
06	0_2	Power State Transition - When the Power State Field of the Power Management Control/Status Register is written to transition the Bridge function Power State from either D3 to D0 or D0 to D3 and the Power State Transition Interrupt mask is cleared, this bit is set.
05	0_2	Detected Parity Error - This bit is set when a parity error is detected during a data transfer on the primary bus even if parity handling is disabled. Set under the following conditions: • Write Data Parity Error when the Primary interface of the Bridge is a slave (downstream write). • Read Data Parity Error when the Primary interface of the Bridge is a master (upstream read). • Any Address Parity Error on the Primary Bus (including one generated by the Primary interface of the Bridge).
04	0_2	**P_SERR#** Asserted - This bit is set if **P_SERR#** is asserted on the primary PCI bus.
03	0_2	PCI Master Abort - This bit is set whenever a transaction initiated by the primary master interface ends in a Master-Abort.
02	0_2	PCI Target Abort (Master) - This bit is set whenever a transaction initiated by the primary master interface ends in a Target-Abort.
01	0_2	PCI Target Abort (Target) - This bit is set whenever the primary interface, acting as a target, terminates the transaction on the PCI bus with a Target-Abort.
00	0_2	PCI Master Parity Error - The primary interface sets this bit when three conditions are met: 1) the bus agent asserted **P_PERR#** itself or observed **P_PERR#** asserted 2) the agent setting the bit acted as the bus master for the operation in which the error occurred 3) the Parity Checking Enable bit (PCR Register) is set

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

21. Section 14.15.34 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 14-55 has been changed.

Bit 01 of this register is no longer reserved. It is now the "Power State Transition Interrupt Mask" bit.



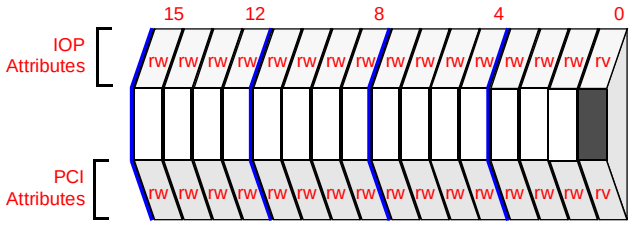
PCI Configuration Offset
5C - 5DH

80960 Core Local Bus Address
0000 105CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
15	1_2	**S_SERR#** Detected Interrupt Mask - When set, detecting **S_SERR#** on the secondary interface resulting in bit 14 of the SSR being set will *not* result in bit 4 of the SBISR being set. When clear, an error that sets bit 14 of the SSR will cause bit 4 of the SBISR to be set
14	1_2	Secondary PCI Master Abort Interrupt Mask - When set, a master abort error resulting in bit 13 of the SSR being set will *not* result in bit 3 of the SBISR being set. When clear, an error that sets bit 13 of the SSR will cause bit 3 of the SBISR to be set.
13	1_2	Secondary PCI Target Abort (Master) Interrupt Mask- When set, a target abort error resulting in bit 12 of the SSR being set will *not* result in bit 2 of the SBISR being set. When clear, an error that sets bit 12 of the SSR will cause bit 2 of the SBISR to be set.
12	1_2	Secondary PCI Target Abort (Target) Interrupt Mask - When set, a target abort error resulting in bit 11 of the SSR being set will *not* result in bit 1 of the SBISR being set. When clear, an error that sets bit 11 of the SSR will cause bit 1 of the SBISR to be set.
11	1_2	Secondary PCI Master Parity Error Interrupt Mask - When set a parity error resulting in bit 8 of the SSR being set will *not* result in bit 0 of the SBISR being set. When clear, an error that sets bit 8 of the SSR will cause bit 0 of the SBISR to be set.
10	1_2	**P_SERR#** Asserted Interrupt Mask - When set, detecting or asserting **P_SERR#** on the primary interface resulting in bit 14 of the PSR being set will *not* result in bit 4 of the PBISR being set. When clear, an error that sets bit 14 of the PSR will cause bit 4 of the PBISR to be set
09	1_2	Primary PCI Master Abort Interrupt Mask - When set, a master abort error resulting in bit 13 of the PSR being set will *not* result in bit 3 of the PBISR being set. When clear, an error that sets bit 13 of the PSR will cause bit 3 of the PBISR to be set.
08	1_2	Primary PCI Target Abort (Master) Interrupt Mask- When set, a target abort error resulting in bit 12 of the PSR being set will *not* result in bit 2 of the PBISR being set. When clear, an error that sets bit 12 of the PSR will cause bit 2 of the PBISR to be set.
07	1_2	Primary PCI Target Abort (Target) Interrupt Mask - When set, a target abort error resulting in bit 11 of the PSR being set will *not* result in bit 1 of the PBISR being set. When clear, an error that sets bit 11 of the PSR will cause bit 1 of the PBISR to be set.



PCI Configuration Offset
5C - 5DH

80960 Core Local Bus Address
0000 105CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

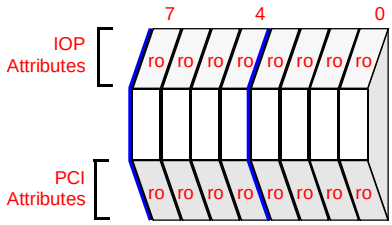
Bit	Default	Description
06	1_2	Primary PCI Master Parity Error Interrupt Mask - When set a parity error resulting in bit 8 of the PSR being set will *not* result in bit 0 of the PBISR being set. When clear, an error that sets bit 8 of the PSR will cause bit 0 of the PBISR to be set.
05	1_2	Secondary Detected Parity Error Bit Interrupt Mask - When set a parity error resulting in bit 15 of the SSR being set will not result in bit 5 of the SBISR being set.
04	1_2	Primary Detected Parity Error Bit Interrupt Mask - When set a parity error resulting in bit 15 of the PSR being set will not result in bit 5 of the PBISR being set.
03	1_2	Secondary Bus Reset Occurred Interrupt Mask - When this bit is set, and the bridge senses the deassertion (by software only) of bit 6, Secondary Bus Reset, in the BCR, bit 6 of the SBISR will not be set.
02	0_2	Private Memory Space Enable - when set, this bit disables Bridge forwarding of addresses in the SMBR/SMLR and SIOBR/SIOLR address ranges. This creates a private memory space on the secondary PCI bus that allows peer to peer transactions.
01	1_2	Power State Transition Interrupt Mask - When this bit is set and the Power Management Control/Status Register is written to transition the Bridge Function Power State from either D0 to D3 or D3 to D0, bit 6 of the PBISR is not set.
00	0_2	Reserved

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

22. Section 14.15.34 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: Capability Pointer Register-Cap_ID (Address 1068H).

The Capability Identifier Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register in the PCI Extended Capability header identifies the type of Extended Capability contained in that header. In the case of the i960 RM/RN I/O processor, this is the PCI Bus Power Management extended capability with an ID of 01H as defined by the *PCI Bus Power Management Interface Specification* Revision 1.1.



PCI Configuration Offset
68H

80960 Core Local Bus Address
0000 1068H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

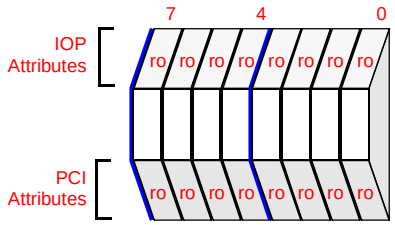
Bit	Default	Description
07:00	01H	Cap_Id - This field with its' 01H value identifies this item in the linked list of Extended Capability Headers as being the PCI Power Management Registers.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

23. Section 14.15.34 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: Next Item Pointer Register-Next_Item_Ptr (Address 1069H).

The Next Item Pointer Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register describes the location of the next item in the function's capability list. For the i960 RM/RN I/O processor, the Power Management Registers are the only Extended Capability Supported, thus the Next_Item_Ptr is set to 00H, indicating the end of the Capabilities List.



PCI Configuration Offset
69H

80960 Core Local Bus Address
0000 1069H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

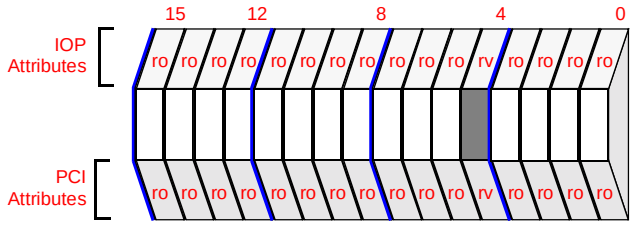
Bit	Default	Description
07:00	00H	Next_ Item_ Pointer - This field provides an offset into the function's configuration space pointing to the next item in the function's capability list. Since there are no other Extended Capabilities besides PCI Power Management in the i960 RM/RN I/O processor, the register is set to 00H.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

24. Section 14.15.34 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: Power Management Capabilities Register-PMCR (Address 106AH).

Power Management Capabilities bits adhere to the definitions in the *PCI Bus Power Management Interface Specification* Revision 1.1. This register is a 16-bit read-only register which provides information on the capabilities of the bridge function related to power management



PCI Configuration Offset
6A- 6BH

80960 Core Local Bus Address
0000 106AH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

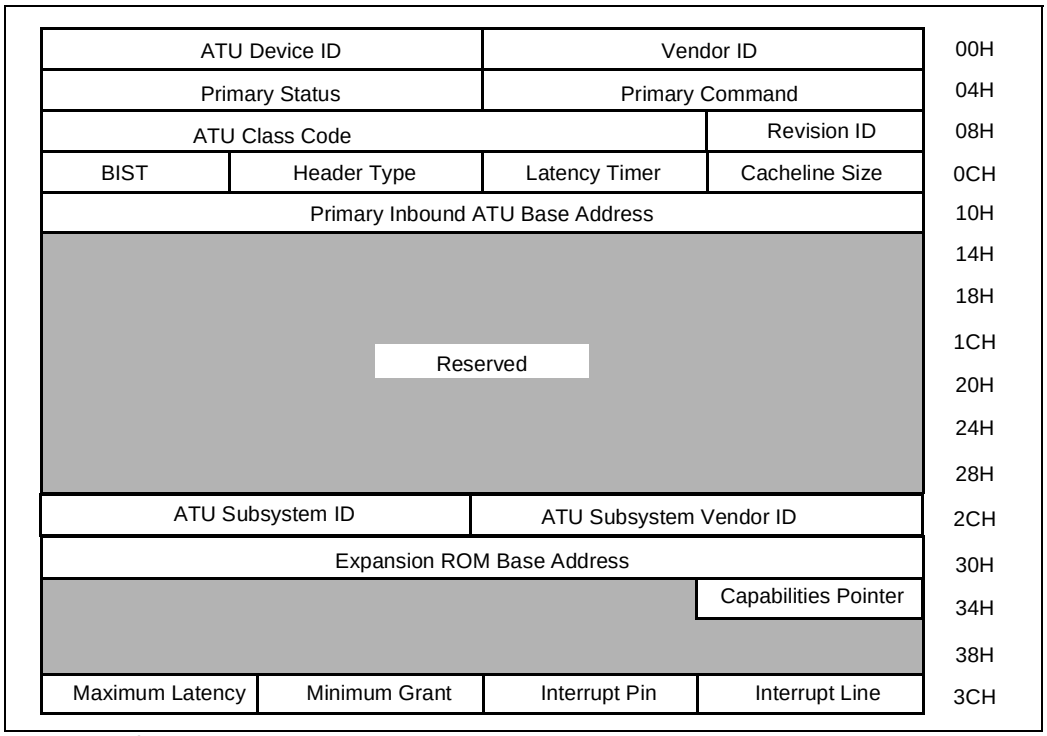
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
15:11	00000_2	PME_Support - This function is not capable of asserting the PME# signal in any state, since PME# is not supported by the i960 RM/RN I/O processor, thus the value of PME_Support is set to 00000B.
10	0_2	D2_Support - This bit is set to 0_2 indicating that the i960 RM/RN I/O processor does not support the D2 Power Management State
9	0_2	D1_Support - This bit is set to 0_2 indicating that the i960 RM/RN I/O processor does not support the D1 Power Management State
8:6	000_2	Aux_Current - This field is set to 000_2 indicating that the i960 RM/RN I/O processor has no current requirements for the 3.3Vaux signal as defined in the *PCI Bus Power Management Interface Specification* Revision 1.1
5	0_2	DSI - This field is set to 0_2 meaning that this function will not require a device specific initialization sequence following the transition to the D0 uninitialized state.
4	0_2	Reserved.
3	0_2	PME Clock - Since the i960 RM/RN I/O processor does not support PME# signal generation, this value is set to 0_2
2:0	010_2	Version - Setting these bits to 010_2 means that this function complies with *PCI Bus Power Management Interface Specification* Revision 1.1

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

25. Section 15.7 of the *i960® RM/RN I/O Processor Developer's Manual*

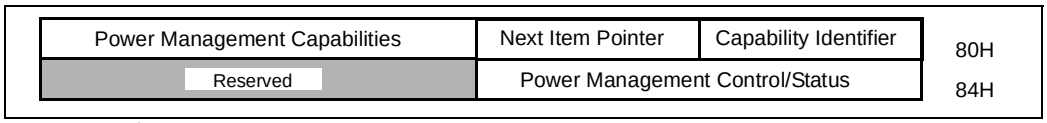
Issue: Figure 15-11 has been changed. It now reflects the following:



Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

26. Section 15.7 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new figure has been added: ATU Interface Extended Configuration Header.



Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

27. Section 15.7 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 15-26 has been changed to read:

Register Name	Register Size in Bits	PCI Configuration Cycle Register Number	Internal Bus Address
ATU Vendor ID Register - ATUVID	16	0	0000.1200H
Device ID Register - DID (80960RN) Device ID Register - DID (80960RM)	16	0	0000.1202H
Primary ATU Command Register - PATUCMD	16	1	0000.1204H
Primary ATU Status Register - PATUSR	16	1	0000.1206H
ATU Revision ID Register - ATURID	8	2	0000.1208H
ATU Class Code Register - ATUCCR	24	2	0000.1209H
ATU Cacheline Size Register - ATUCLSR	8	3	0000.120CH
ATU Latency Timer Register - ATULT	8	3	0000.120DH
ATU Header Type Register - ATUHTR	8	3	0000.120EH
ATU BIST Register - ATUBISTR	8	3	0000.120FH
Primary Inbound ATU Base Address - PIABAR	32	4	0000.1210H
Reserved	32	5	0000.1214H
Reserved	32	6	0000.1218H
Reserved	32	7	0000.121CH
Reserved	32	8	0000.1220H
Reserved	32	9	0000.1224H
Reserved	32	10	0000.1228H
ATU Subsystem Vendor ID Register - ASVIR	16	11	0000.122CH
ATU Subsystem ID Register - ASIR	16	11	0000.122EH
Expansion ROM Base Address Register -ERBAR	32	12	0000.1230H
ATU Capabilities Pointer Register	8	13	0000.1234H
Reserved	8	13	0000.1235H
Reserved	16	13	0000.1236H
Reserved	32	14	0000.1238H
ATU Interrupt Line Register - ATUILR	8	15	0000.123CH
ATU Interrupt Pin Register - ATUIPR	8	15	0000.123DH
ATU Minimum Grant Register - ATUMGNT	8	15	0000.123EH
ATU Maximum Latency Register - ATUMLAT	8	15	0000.123FH
Primary Inbound ATU Limit Register - PIALR	32	16	0000.1240H
Primary Inbound ATU Translate Value Register - PIATVR	32	17	0000.1244H
Secondary Inbound ATU Base Address Register - SIABAR	32	18	0000.1248H
Secondary Inbound ATU Limit Register - SIALR	32	19	0000.124CH
Secondary Inbound Translate ATU Value Register - SIATVR	32	20	0000.1250H
Primary Outbound Memory Window Value Register -POMWVR	32	21	0000.1254H
Reserved	32	22	0000.1258H
Primary Outbound I/O Window Value Register - POIOWVR	32	23	0000.125CH
Primary Outbound DAC Window Value Register - PODWVR	32	24	0000.1260H

Register Name	Register Size in Bits	PCI Configuration Cycle Register Number	Internal Bus Address
Primary Outbound Upper 64-bit DAC Register - POUDR	32	25	0000.1264H
Secondary Outbound Memory Window Value Register - SOMWVR	32	26	0000.1268H
Secondary Outbound I/O Window Value Register - SOIOWVR	32	27	0000.126CH
Reserved	32	28	0000.1270H
Expansion ROM Limit Register - ERLR	32	29	0000.1274H
Expansion ROM Translate Value Register - ERTVR	32	30	0000.1278H
Reserved	32	31	0000.127CH
ATU Capability Identifier Register	8	32	0000.1280H
ATU Next Item Pointer Register	8	32	0000.1281H
ATU Power Management Capabilities Register	16	32	0000.1282H
ATU Power Management Control/StatusRegister	16	32	0000.1284H
Reserved	16	33	0000.1286H
ATU Configuration Register - ATUCR	32	34	0000.1288H
Reserved	32	35	0000.128CH
Primary ATU Interrupt Status Register - PATUISR	32	36	0000.1290H
Secondary ATU Interrupt Status Register - SATUISR	32	37	0000.1294H
Secondary ATU Command Register - SATUCMD	16	38	0000.1298H
Secondary ATU Status Register - SATUSR	16	38	0000.129AH
Secondary Outbound DAC Window Value Register - SODWVR	32	39	0000.129CH
Secondary Outbound Upper 64-bit DAC Register - SOUDR	32	40	0000.12A0H
Primary Outbound Configuration Cycle Address Register - POCCAR	32	41	0000.12A4H
Secondary Outbound Configuration Cycle Address Register - SOCCAR	32	42	0000.12A8H
Secondary Outbound Configuration Cycle Data Register - SOCCDR	32	Not Available in PCI Configuration Space	0000.12ACH
Primary Outbound Configuration Cycle Data Register - POCCDR	32	Not Available in PCI Configuration Space	0000.12B0H
Primary ATU Interrupt Mask Register - PATUIMR	32	47	0000.12BCH
Secondary ATU Interrupt Mask Register - SATUIMR	32	48	0000.12C0H

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

28. Section 15.7 of the *i960® RM/RN I/O Processor Developer's Manual*

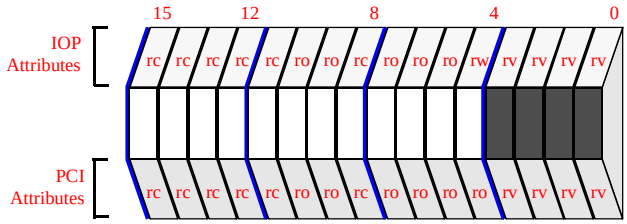
Issue: Table 15-27 has been changed to read:

Internal Bus Address Offset	ATU PCI Configuration Register Section, Name, Page
00H	Section 15.7.1, "ATU Vendor ID Register - ATUVID" on page 15-51
02H	Section 15.7.2, "ATU Device ID Register - ATUDID" on page 15-52
04H	Section 15.7.3, "Primary ATU Command Register - PATUCMD" on page 15-53
06H	Section 15.7.4, "Primary ATU Status Register - PATUSR" on page 15-54
08H	Section 15.7.5, "ATU Revision ID Register - ATURID" on page 15-56
09H	Section 15.7.6, "ATU Class Code Register - ATUCCR" on page 15-56
0CH	Section 15.7.7, "ATU Cacheline Size Register - ATUCLSR" on page 15-57
0DH	Section 15.7.8, "ATU Latency Timer Register - ATULT" on page 15-57
0EH	Section 15.7.9, "ATU Header Type Register - ATUHTR" on page 15-58
0FH	Section 15.7.10, "ATU BIST Register - ATUBISTR" on page 15-59
10H	Section 15.7.11, "Primary Inbound ATU Base Address Register - PIABAR" on page 15-60
2CH	Section 15.7.12, "ATU Subsystem Vendor ID Register - ASVIR" on page 15-61
2EH	Section 15.7.13, "ATU Subsystem ID Register - ASIR" on page 15-61
30H	Section 15.7.14, "Expansion ROM Base Address Register - ERBAR" on page 15-62
34H	"ATU Capabilities Pointer Register - ATU_Cap_Ptr"
3CH	Section 15.7.15, "Determining Block Sizes for Base Address Registers" on page 15-63
3DH	Section 15.7.16, "ATU Interrupt Line Register - ATUILR" on page 15-64
3EH	Section 15.7.18, "ATU Minimum Grant Register - ATUMGNT" on page 15-66
3FH	Section 15.7.19, "ATU Maximum Latency Register - ATUMLAT" on page 15-67
40H	Section 15.7.20, "Primary Inbound ATU Limit Register - PIALR" on page 15-68
44H	Section 15.7.21, "Primary Inbound ATU Translate Value Register - PIATVR" on page 15-69
48H	Section 15.7.22, "Secondary Inbound ATU Base Address Register - SIABAR" on page 15-70
4CH	Section 15.7.23, "Secondary Inbound ATU Limit Register - SIALR" on page 15-71
50H	Section 15.7.24, "Secondary Inbound ATU Translate Value Register - SIATVR" on page 15-72
54H	Section 15.7.25, "Primary Outbound Memory Window Value Register - POMWVR" on page 15-73
5CH	Section 15.7.26, "Primary Outbound I/O Window Value Register - POIOWVR" on page 15-74
60H	Section 15.7.27, "Primary Outbound DAC Window Value Register - PODWVR" on page 15-75
64H	Section 15.7.28, "Primary Outbound Upper 64-bit DAC Register - POUDR" on page 15-76
68H	Section 15.7.29, "Secondary Outbound Memory Window Value Register - SOMWVR" on page 15-77
6CH	Section 15.7.30, "Secondary Outbound I/O Window Value Register - SOIOWVR" on page 15-78
74H	Section 15.7.31, "Expansion ROM Limit Register - ERLR" on page 15-79
78H	Section 15.7.32, "Expansion ROM Translate Value Register - ERTVR" on page 15-80
80H	"ATU Capability Identifier Register - ATU_Cap_ID"
81H	"ATU Next Item Pointer Register - ATU_Next_Item_Ptr"
82H	"ATU Power Management Capabilities Register - APMCR"
84H	"ATU Power Management Control/Status Register - APMCSR"
88H	Section 15.7.33, "ATU Configuration Register - ATUCR" on page 15-81
90H	Section 15.7.34, "Primary ATU Interrupt Status Register - PATUISR" on page 15-83
94H	Section 15.7.35, "Secondary ATU Interrupt Status Register - SATUISR" on page 15-85
98H	Section 15.7.36, "Secondary ATU Command Register - SATUCMD" on page 15-87
9AH	Section 15.7.37, "Secondary ATU Status Register - SATUSR" on page 15-88
9CH	Section 15.7.38, "Secondary Outbound DAC Window Value Register - SODWVR" on page 15-89
A0H	Section 15.7.39, "Secondary Outbound Upper 64-bit DAC Register - SOUDR" on page 15-90
A4H	Section 15.7.40, "Primary Outbound Configuration Cycle Address Register - POCCAR" on page 15-91
A8H	Section 15.7.41, "Secondary Outbound Configuration Cycle Address Register - SOCCAR" on page 15-92
ACH	Section 15.7.42, "Primary Outbound Configuration Cycle Data Register - POCCDR" on page 15-93
B0H	Section 15.7.43, "Secondary Outbound Configuration Cycle Data Register - SOCCDR" on page 15-94
BCH	Section 15.7.44, "Primary ATU Interrupt Mask Register - PATUIMR" on page 15-95
C0H	Section 15.7.45, "Secondary ATU Interrupt Mask Register - SATUIMR" on page 15-96

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

29. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 15-32 has been changed. The change is that Bit 04 is no longer a reserved bit. It is now the "Capabilities" bit.



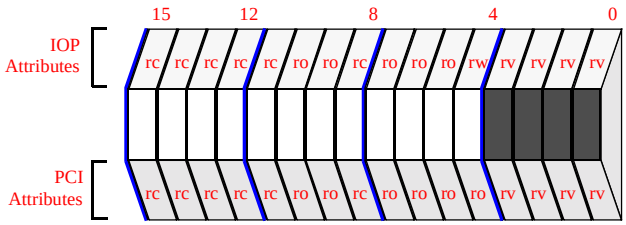
80960 Core Local Bus Address
1206H

PCI Configuration Address Offset
06H - 07H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
15	0_2	Detected Parity Error - set when a parity error is detected on the primary PCI bus even when the PATUCMD register's Parity Error Response bit is cleared. Set under the following conditions: • Write Data Parity Error when the PATU is a slave (inbound write). • Read Data Parity Error when the PATU, DMA Channel 0, or DMA Channel1 is a master (outbound read). • Any Address Parity Error on the Primary Bus (including one generated by the PATU or DMA Channels 0 &1).
14	0_2	P_SERR# Asserted - set when P_SERR# is asserted on the PCI bus by the primary ATU.
13	0_2	Master Abort - set when a transaction initiated by the primary ATU PCI master interface, DMA Channel 0, or DMA Channel 1 ends in a Master-Abort. Setting of this bit due to an error condition from either DMA Channel will not cause an ATU interrupt to the core.
12	0_2	Target Abort (master) - set when a transaction initiated by the primary ATU PCI master interface, DMA Channel 0 master interface or DMA Channel 1 master interface ends in a target abort. Setting of this bit due to an error condition from either DMA Channel will not cause an ATU interrupt to the core.
11	0_2	Target Abort (target) - set when the primary ATU interface, acting as a target, terminates the transaction on the primary PCI bus with a target abort.
10:09	01_2	DEVSEL# Timing - These bits are read-only and define the slowest DEVSEL# timing for a target device (except configuration accesses). 00_2 = Fast 01_2 = Medium 10_2 = Slow 11_2 = Reserved This primary and secondary ATU interfaces uses Medium timing (01_2)
08	0_2	Master Parity Error - The primary ATU interface sets this bit under the following conditions: • The PATU, DMA Channel 0, or DMA Channel 1 asserted S_PERR# itself or the PATU observed S_PERR# asserted. • And the PATU, DMA Channel 0, or DMA Channel 1 acted as the bus master for the operation in which the error occurred. • And the PATUCMD register's Parity Error Response bit is set Setting of this bit due to an error condition from either DMA Channel will not cause an ATU interrupt to the core.



80960 Core Local Bus Address
1206H

PCI Configuration Address Offset
06H - 07H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07	1_2	Fast Back-to-Back - The ATU/Messaging Unit interface is capable of accepting fast back-to-back transactions when the transactions are not to the same target.
06	0_2	UDF Supported - User Definable Features are not supported
05	0_2	66 MHz. Capable - 66 MHz operation is not supported.
04	0_2	**Capabilities** - When set, this function implements extended capabilities.
03:00	00000_2	Reserved

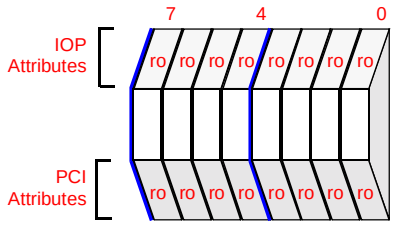
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

30. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: ATU Capabilities Pointer Register-ATU_Cap_Ptr (Address 1234H).

The Capabilities Pointer Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register provides an offset in this function's PCI Configuration Space for the location of the first item in the Capabilities linked list. In the case of the i960 RM/RN I/O processor, this is the PCI Bus Power Management extended capability as defined by the *PCI Bus Power Management Interface Specification* Revision 1.1.

Capabilities Pointer Register - ATU_Cap_Ptr



80960 Core Local Bus Addresst
0000 1234H

PCI Configuration Address Offset
34H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07:00	80H	Capability List Pointer - This provides an offset in this function's configuration space that points to the i960 RM/RN I/O processor's PCI Bus Power Management extended capability.

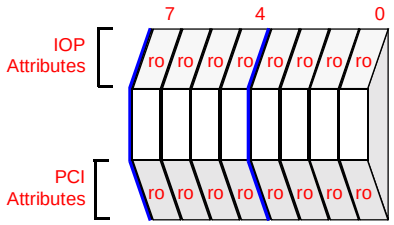
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

31. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: ATU Capability Identifier Register - ATU_Cap_ID (Address 1280H).

The Capability Identifier Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register in the PCI Extended Capability header identifies the type of Extended Capability contained in that header. In the case of the i960 RM/RN I/O processor, this is the PCI Bus Power Management extended capability with an ID of 01H as defined by the *PCI Bus Power Management Interface Specification* Revision 1.1.

ATU Capability Identifier Register - ATU_Cap_ID



PCI Configuration Offset
80H

80960 Core Local Bus Address
0000 1280H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07:00	01H	Cap_Id - This field with its' 01H value identifies this item in the linked list of Extended Capability Headers as being the PCI Power Management Registers.

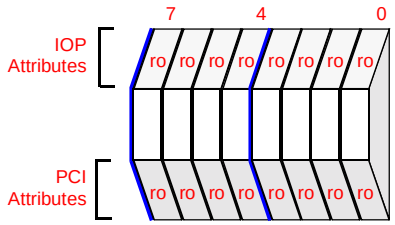
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

32. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: ATU Next Item Pointer Register-ATU_Next_Item_Ptr (Address 1281H).

The Next Item Pointer Register bits adhere to the definitions in the *PCI Local Bus Specification* Revision 2.2. This register describes the location of the next item in the function's capability list. For the i960 RM/RN I/O processor, the Power Management Registers are the only Extended Capability Supported, thus the Next_Item_Ptr is set to 00H, indicating the end of the Capabilities List.

ATU Next Item Pointer Register - ATU_Next_Item_Ptr



PCI Configuration Offset
81H

80960 Core Local Bus Address
0000 1281H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07:00	00H	Next_ Item_ Pointer - This field provides an offset into the function's configuration space pointing to the next item in the function's capability list. Since there are no other Extended Capabilities besides PCI Power Management in the i960 RM/RN I/O processor, the register is set to 00H.

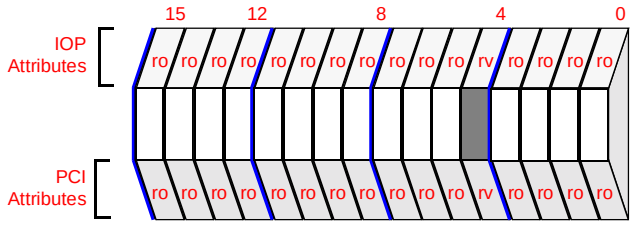
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

33. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: New register added: ATU Power Management Capabilities Register-APMCR (Address 1282).

Power Management Capabilities bits adhere to the definitions in the *PCI Bus Power Management Interface Specification* Revision 1.1. This register is a 16-bit read-only register which provides information on the capabilities of the ATU function related to power management.

ATU Power Management Capabilities Register - APMCR



PCI Configuration Offset
82- 83H

80960 Core Local Bus Address
0000 1282H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
15:11	00000_2	PME_Support - This function is not capable of asserting the PME# signal in any state, since PME# is not supported by the i960 RM/RN I/O processor, thus the value of PME_Support is set to 00000B.
10	0_2	D2_Support - This bit is set to 0_2 indicating that the i960 RM/RN I/O processor does not support the D2 Power Management State
9	0_2	D1_Support - This bit is set to 0_2 indicating that the i960 RM/RN I/O processor does not support the D1 Power Management State
8:6	000_2	Aux_Current - This field is set to 000_2 indicating that the i960 RM/RN I/O processor has no current requirements for the 3.3Vaux signal as defined in the *PCI Bus Power Management Interface Specification* Revision 1.1
5	0_2	DSI - This field is set to 0_2 meaning that this function will require a device specific initialization sequence following the transition to the D0 uninitialized state.
4	0_2	Reserved.
3	0_2	PME Clock - Since the i960 RM/RN I/O processor does not support PME# signal generation, this value is set to 0_2
2:0	010_2	Version - Setting these bits to 010_2 means that this function complies with *PCI Bus Power Management Interface Specification* Revision 1.1

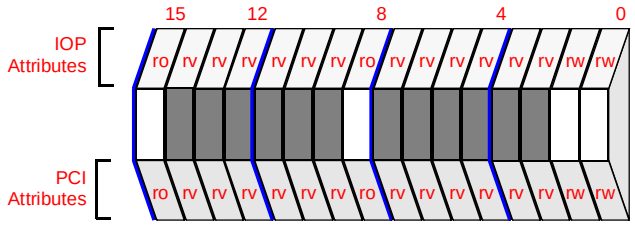
Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

34. Section 15.7.4 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: A new register has been added: ATU Power Management Control/Status Register-APMCSR (Address 1284).

Power Management Control/Status bits adhere to the definitions in the *PCI Bus Power Management Interface Specification* Revision 1.1. This 16-bit register is the primary control and status interface for the power management extended capability.

ATU Power Management Control/Status Register - APMCSR



PCI Configuration Offset
84- 85H

80960 Core Local Bus Address
0000 1284H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

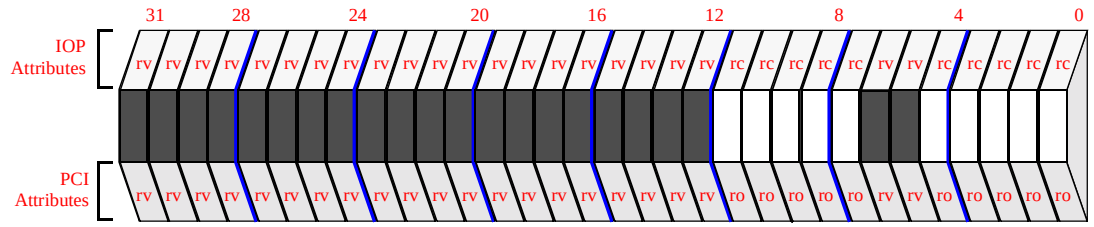
Bit	Default	Description
15	0_2	PME_Status - This function is not capable of asserting the PME# signal in any state, since PME# is not supported by the i960 RM/RN I/O processor, thus the value of PME_Status is set to 0_2 and is read-only.
14:9	00H	Reserved
8	0_2	PME_En - This bit is hardwired to read-only 0_2 since this function does not support PME# generation from any power state.
7:2	000000_2	Reserved
1:0	00_2	Power State - This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the values is: 00_2 - D0 01_2 - D1 (Unsupported) 10_2 - D2 (Unsupported) 11_2 - $D3_{hot}$ The i960 RM/RN I/O processor supports only the D0 and $D3_{hot}$ states. According to the specification, the register will need to be designed to discard writes of 01B or 10B, though the write operation should complete on the bus normally. In other words, no state change should occur! A change of state from D0 -> D3 or D3 -> D0 will result in an NMI interrupt of the i960 JF processor.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

35. Section 15.7.34 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 15-63 needs to be changed.

Bit 11 of the Primary ATU Interrupt Status Register is no longer a reserved bit. It is now the "Power State Transition" bit.



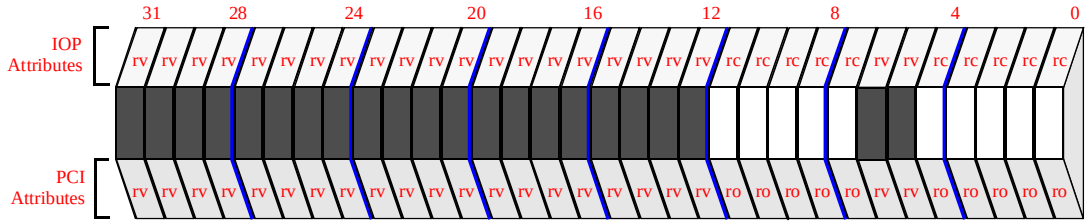
80960 Core Local Bus Address
1290H

PCI Configuration Address Offset
90H - 93H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:12	00000H	Reserved
11	0_2	Power State Transition - When the Power State Field of the ATU Power Management Control/Status Register is written to transition the ATU function Power State from either D3 to D0 or D0 to D3 and the ATU Power State Transition Interrupt mask bit is cleared, this bit is set.
10	0_2	P_SERR# Asserted - set when P_SERR# is asserted on the PCI bus by the primary ATU.
09	0_2	Detected Parity Error - set when a parity error is detected on the primary PCI bus even when the PATUCMD register's Parity Error Response bit is cleared. Set under the following conditions: • Write Data Parity Error when the PATU is a slave (inbound write). • Read Data Parity Error when the PATU is a master (outbound read). Read Data Parity Errors when DMA Channel 0 or DMA Channel 1 is the master ARE NOT logged here, and instead are logged in the appropriate DMA CSR. • Any Address Parity Error on the Primary Bus (including one generated by the PATU or DMA Channels 0 & 1 when loopback is enabled).
08	0_2	ATU BIST Interrupt - When set, the host processor has set the start BIST, ATUBISTR register bit 6, and the ATU BIST interrupt enable (ATUCR register bit 12) is enabled. The i960 core processor can initiate the software BIST and store the result in ATUBISTR register bits 3:0.
07	0_2	Internal Bus Master Abort - set when a transaction initiated by the ATU internal bus master interface ends in a Master-abort.
06:05	00_2	Reserved.



80960 Core Local Bus Address
1290H

PCI Configuration Address Offset
90H - 93H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

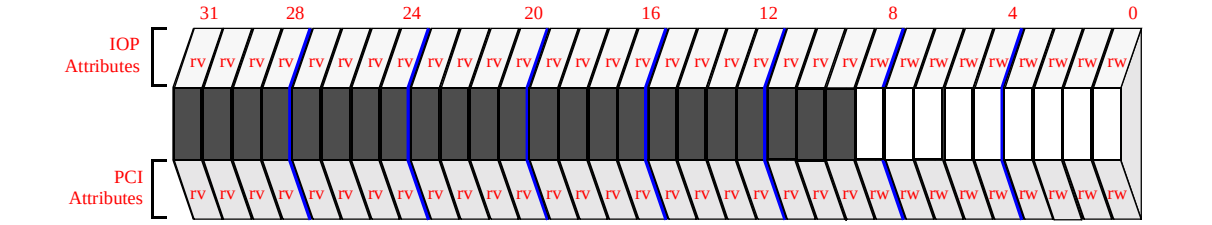
Bit	Default	Description
04	0_2	P_SERR# Detected - set when P_SERR# is detected on the PCI bus by the primary ATU.
03	0_2	PCI Master Abort - set when a transaction initiated by the ATU PCI master interface ends in a Master-abort.
02	0_2	PCI Target Abort (master) - set when a transaction initiated by the ATU PCI master interface ends in a Target-abort.
01	0_2	PCI Target Abort (target) - set when the ATU interface, acting as a target, terminates the transaction on the PCI bus with a target abort.
00	0_2	PCI Master Parity Error - The ATU interface sets this bit when three conditions are met: • the PATU asserted S_PERR# or observed S_PERR# asserted • the PATU acted as the bus master for the operation in which the error occurred • Parity Error Response bit is set (in the Primary ATU Command Register)

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

36. Section 15.7.44 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Table 15-73 has been changed.

Bit 08 of the PATUIMR is no longer reserved: it is now the "Power State Transition Interrupt Mask" bit.



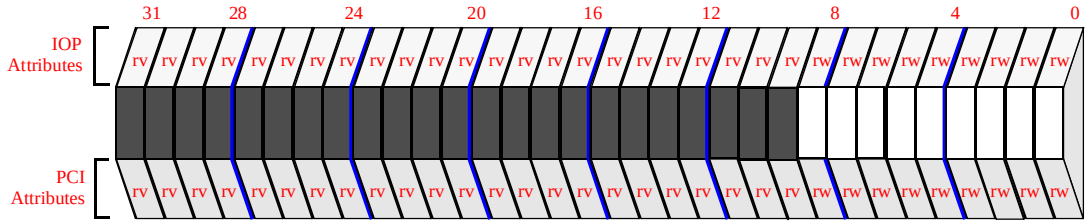
80960 Core Local Bus Address
12BCH

PCI Configuration Address Offset
BCH - BFH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:09	0000 00H	Reserved
08	1_2	Power State Transition Interrupt Mask - When this bit is set and the ATU Power Management Control/Status Register is written to transition the ATU Function Power State from either D0 to D3 or D3 to D0, bit 11of the PATUISR is not set.
07	0_2	PATU Detected Parity Error Interrupt Mask - When set, a parity error detected on the primary PCI bus that sets bit 15 of the PATUSR will *not* result in bit 9 of the PATUISR being set. When clear, an error that sets bit 15 of the PATUSR will result in bit 9 of the PATUISR being set.
06	0_2	PATU **P_SERR#** Asserted Interrupt Mask - When set, asserting **P_SERR#** on the primary interface resulting in bit 14 of the PATUSR being set will *not* result in bit 10 of the PATUISR being set. When clear, an error that sets bit 14 of the PATUSR will cause bit 10 of the PATUISR to be set. Note that this bit is specific to the PATU asserting **P_SERR#** and not detecting **P_SERR#** from another master.
05	0_2	PATU PCI Master Abort Interrupt Mask - When set, a master abort error resulting in bit 13 of the PATUSR being set will *not* result in bit 3 of the PATUISR being set. When clear, an error that sets bit 13 of the PATUSR will cause bit 3 of the PATUISR to be set.



80960 Core Local Bus Address
12BCH

PCI Configuration Address Offset
BCH - BFH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
04	0_2	PATU PCI Target Abort (Master) Interrupt Mask- When set, a target abort error resulting in bit 12 of the PATUSR being set will *not* result in bit 2 of the PATUISR being set. When clear, an error that sets bit 12 of the PATUSR will cause bit 2 of the PATUISR to be set.
03	0_2	PATU PCI Target Abort (Target) Interrupt Mask- When set, a target abort error resulting in bit 11 of the PATUSR being set will *not* result in bit 1 of the PATUISR being set. When clear, an error that sets bit 11 of the PATUSR will cause bit 1 of the PATUISR to be set.
02	0_2	PATU PCI Master Parity Error Interrupt Mask - When set, a parity error resulting in bit 8 of the PATUSR being set will *not* result in bit 0 of the PATUISR being set. When clear, an error that sets bit 8 of the PATUSR will cause bit 0 of the PATUISR to be set.
01	0_2	Primary ATU Inbound Error P_SERR# Enable - When set, the PATU will assert (if enabled through the PATUCMD) **P_SERR#** on the primary interface in response to a master abort on the internal bus during an inbound write transaction or a target abort from the memory controller (ECC Error) during an inbound write transaction. When clear, **P_SERR#** will not be asserted under the previous conditions.
00	0_2	Primary ATU ECC Target Abort Enable - When set, the PATU will perform a target abort on the primary PCI interface in response to a target abort (ECC error) from the memory controller on the internal bus. This action only occurs when during an inbound read transaction where the data phase that was target aborted on the internal bus is actually requested from the inbound read queue. When clear, the response under the same conditions is a disconnect with data (the data being up to 64 bits of 1's) on the PCI bus instead of a target abort.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

37. Section 15.7.20, Table 15-49

Issue: Table 15-49 has been changed.

The default value of bits 31:12 in the Primary Inbound ATU Limit Register (PIALR) has changed on the B-0 stepping from FFFFEH to FF000H, which corresponds to an inbound window of 16MB.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

38. Section 15.7 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: On page 15-49, register 12ACh should be POCCDR and register 12B0h should be SOCCDR. Table 15-26 has been changed.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

39. Section 3.5.1, page 3-11

Issue: In the paragraph headed by the words “atomic access”, remove the last two sentences that state: “An atomic memory system can be implemented by using the LOCK# signal to qualify hold requests from external bus agents. The processor asserts LOCK# for the duration of an atomic memory operation.” There is no LOCK# signal on the 80960RM/RN.

Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

40. Section 13.2.3, page 13-8

Issue: The statement in the 4th paragraph, that reads “The core is the only device permitted to write to the Flash device...” should read “Software must ensure that only a single byte is written”.

The Flash device can be programmed via PCI commands through the ATU. In fact Intel’s FlashI/O utility (which is part of our ProI/O Utilities) programs the Flash using the ATU.

Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

41. Section 12.3.1, page 12-4

Issue: The sentence on page 12-4, ‘The LMCON registers and their programming are described in Section 12.3, “Programming the Logical Memory Attributes” on page 12-4.’ has been removed.

Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

42. Section 11.2.8, page 11-5

Issue: The sentence on page 11-5, “Specifications for cold and warm reset can be found in the 80960RM I/O Processor Data Sheet and the 80960RN I/O Processor Data Sheet.” has been removed.

Unlike the i960RP/RD I/O processor, the i960RM/RN I/O processor has no external local bus. The cold and warm reset signals referenced in the i960RP/RD I/O processor data sheet are not accessible on the i960RM/RN I/O processor. The i960RM/RN I/O processor complies with the PCI local bus spec v2.2. Reset parameters are defined in this spec.

Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

43. Section 14.15 Bridge Configuration Header Bottom Address Offset 60H

Issue: The bottom - address offset 60H in Figure 14-11 is Reserved. See Documentation Change 12 in this spec update.

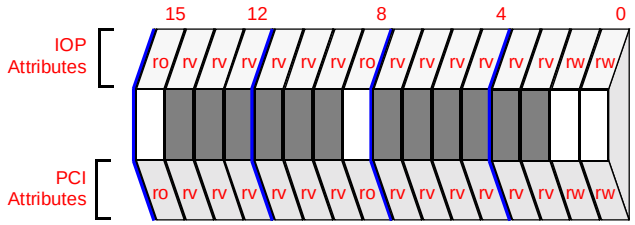
Affected Docs: *i960® RM/RN I/O Processor Developer’s Manual*

44. Power Management Control/Status Register - PMCSR (address 106C)

Issue: This new register has been added. Power Management Control/Status bits adhere to the definitions in the *PCI Bus Power Management Interface Specification* Revision 1.1. This 16-bit register is the primary control and status interface for the power management extended capability.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

Power Management Control/Status Register - PMCSR



PCI Configuration Offset
6C- 6DH

80960 Core Local Bus Address
0000 106CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

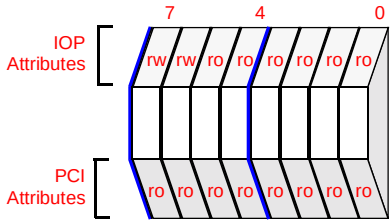
Bit	Default	Description
15	0_2	PME_Status - This function is not capable of asserting the PME# signal in any state, since PME# is not supported by the i960® RM/RN I/O processor, thus the value of PME_Status is set to 0_2 and is read-only.
14:9	00H	Reserved
8	0_2	PME_En - This bit is hardwired to read-only 0_2 since this function does not support PME# generation from any power state.
7:2	000000_2	Reserved.
1:0	00_2	Power State - This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the values is: 00_2 - D0 01_2 - D1 (Unsupported) 10_2 - D2 (Unsupported) 11_2 - $D3_{hot}$ The i960® RM/RN I/O processor supports only the D0 and $D3_{hot}$ states. According to the specification, the register will need to be designed to discard writes of 01B or 10B. Although such write operations should complete on the bus normally, no state changes should occur. A change of state from D0 -> D3 or D3 -> D0 will result in an NMI interrupt of the i960 JT processor.

45. PMCSR PCI to PCI Bridge Support - PMCSR_BSE

Issue: This new register has been added (as part of ACPI). This register supports Bridge specific Power Management Control/Status functionality and is required for all PCI-to-PCI bridges.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

PMCSR PCI to PCI Bridge Support - PMCSR_BSE



PCI Configuration Offset
6EH

80960 Core Local Bus Address
0000 106EH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07	0_2	BPCC_En (Bus Power/Clock Control Enable) - If this bit is set, the Power State field in the PMCSR register can be used to control the secondary bus Power/Clock.
06	0_2	B2_B3# (B2/B3 support for $D3_{hot}$) - If BPCC_EN (bit 07) is set, the state of this bit determines the action that is to occur as a direct result of programming the Power State field of the PMCSR from D0 to $D3_{hot}$. If this bit is set, the secondary bus PCI clock will be stopped (B2) when the Power State field of the PMCSR is programmed to $D3_{hot}$ and BPCC_EN is set. If this bit is cleared, the secondary bus will have its power removed (B3) when the Power State field of the PMCSR is programmed to $D3_{hot}$ and BPCC_EN is set.
5:0	000000_2	Reserved.

46. 128Mbit SDRAM Technology

Issue: Table 13-6 of the *i960® RM/RN I/O Processor Developer's Manual*, lists the supported SDRAM configurations. The table only lists 16Mbit and 64Mbit SDRAM technology.

Status: 128Mbit SDRAM devices configured as 8Mx16 can also be used with the 80960 RM/RN. These devices multiplex 12 rows and 9 columns on the address bus, which is the same as the 64Mbit, 8Mx8 SDRAM devices. Therefore, all the 128Mbit memory will be addressable when the SDRAM boundary register bit 31 is set to indicate 64Mbit.

There is one limitation to using this configuration. Using x16 SDRAM with ECC-on, means half of one of the ECC SDRAM modules will not be used. The developer's manual states on page 13-11, 'Since an ECC-supported system needs to be 72 bits wide, x16 devices are not optimal.'

Using three 128Mb 8Mx16 devices, a 32-bit configuration with ECC-on in a single 40-bit bank (40 of 48-bits usable) would yield 32Mbytes of usable ECC memory.

Using five 128Mb 8Mx16 devices, a 64-bit configuration with ECC-on in a single 72-bit bank (72 of 80-bits usable) would yield 64Mbytes of usable ECC memory.

Table 13-6 on page 13-11 has changed.

Table 13-6. Supported SDRAM Configurations

SDRAM Technology	SDRAM Arrangement	# Banks	Address Size		Leaf Select		Total Memory Size
			Row	Column	SBA[1]	SBA[0]	
16 Mbit	2M x 8	1	11	9	-	I_AD[23]	16M
		2					32M
	1M x 16	1	11	8	-	I_AD[22]	8M
		2					16M
64 Mbit	8M x 8	1	12	9	I_AD[25]	I_AD[24]	64M
		2					128M
	4M x 16	1	12	8	I_AD[24]	I_AD[23]	32M
		2					64M
128 Mbit	8M x 16	1	12	9	I_AD[25]	I_AD[24]	64M
		2					128M

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

47. 64 Bit Operation

Issue: Section 14.6.3 of the *i960® RM/RN I/O Processor Developer's Manual*, titled "64-Bit Operation," incorrectly states that the i960® RM I/O processor is a 64 bit PCI device. This is a typographical error. The i960 RM I/O processor is a 32 bit/33MHz PCI device. Any reference to the i960® RM I/O processor in section 14.6.3 on pages 14-26—14-31 should be ignored.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

48. Scrubbing

Section 13.3.7.4 of the Developer's Manual mentions using the i960 JT I/O processor **atmod** instruction as well as **ldl/stl** and **ld/st** instructions in a scrubbing routine. The entire section should be changed to read as follows:

Fixing the data error in memory is called scrubbing. The i960 RM/RN I/O processor relies on software scrubbing. Once the MCU detects an error during a read, the MCU writes the address where the error occurred in the ECARx register, updates the ELOGx register with information regarding the error and interrupts the core with an NMI. The core decides how to fix the error through an interrupt handler. Software could decide to perform the scrubbing on:

- the data location that failed
- the entire row of the data that failed
- the entire memory

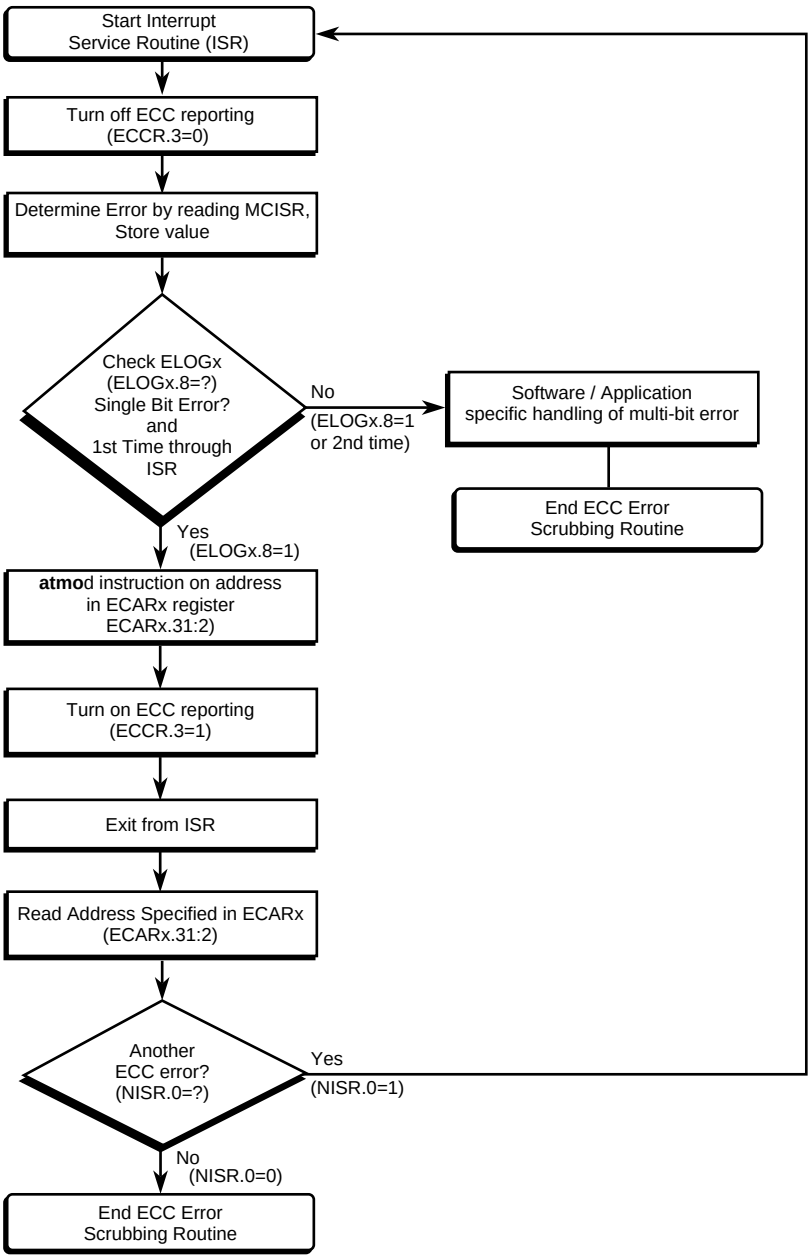
The interrupt handler should perform the following actions.

1. Turn off ECC error reporting.

Note: Since the scrubbing routine reads the failed location in order to fix the single-bit error, a second error is reported. Therefore, software should disable single-bit ECC reporting (ECCR[0]) during the scrubbing routine.

2. Read the MCISR register and store the results. Determine which ECAR/ELOG register the MCU used to record the ECC error. Note: This is a read clear register.
3. Check the ELOGx register for information about the ECC error. Determine if the error is a single bit or multi-bit error. Double-bit or nibble errors cannot be fixed. If it's a single-bit error, continue.
4. Do an **atmod** (read, modify, write) to the address specified in the ECARx register. Even though an atmod instruction is only a 32 bit instruction, this will work for either 32 bit memory mode or 64 bit memory mode. The error is fixed by the MCU when it reads the memory location and stores the value in the register, then the corrected data is written back to the memory location.
5. Turn on ECC error reporting.
6. Exit from ISR.
7. Read from the address specified in the ECARx register again.
8. If no errors are reported (through NMI interrupt), the scrubbing procedure worked.
9. If another error is generated, treat this as a multi-bit error.

The diagram below is a flowchart version of the scrubbing routine.



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Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*

49. I²C Reset Condition/Lockup

Issue: Section 22.7 of the *i960® RM/RN I/O Processor Developer's Manual* states that software is responsible for ensuring the I^2C bus is idle before enabling the unit after reset. If this guidance is not adhered to, the 80960 RM/RN could lock up the I^2C bus by pulling SCL low and locking it in that state. If this does occur, it is possible to release the lock by toggling the I^2C unit enable bit (bit 06) in the I^2C Control Register (ICR - 1680H).

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

50. New PCI Clock Buffer

Issue: There is a new clock buffer recommended for 80960 RM/RN designs. While this new clock buffer has the same geometry and pin outs as the CY7B9910, it has the advantage of being spread spectrum aware and has a PLL lock time of 25 us. Contact Cypress Semiconductor for pricing and availability questions.

Manufacturer	Part Number
Cypress	W217 (new)
Cypress	CY7B9910

Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

Status: ***Design Guide revised.***

51. Section 13.6.4 SDRAM Boundary Register 0 - SBR0

The guidance in this paragraph differs from the examples that are referenced. The second sentence should read:

If bank 0 is unpopulated, SBR0[5:0] is programmed with the same value as SBR1[5:0].

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

52. Section 13.6.5 SDRAM Boundary Register 1- SBR1

The guidance in this paragraph differs from the examples that are referenced. The second sentence should read:

If bank 0 is unpopulated, SBR1[5:0] is programmed with the same value as SBR0[5:0].

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

53. Section 13.2.3 Flash Write Cycle (pg 13-8)

The first sentence of the 4th paragraph should read:

"The MCU does not support bursting data to a Flash device since the flash device has no write buffers to support bursting data.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

54. Section 11.5 Device Identification on Reset

The last sentence of the second paragraph should read:

"During initialization, the DEVICEID is placed in g0."

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

55. Table 21, line 7, Symbol "V_{OH1}", Notes Section Next to I_{OH} = -200uA (3) Add Note (6)

Note 6 should read: "Guaranteed by characterization."

Affected Docs: *i960® RM/RN I/O Processor Design Guide.*

Status: ***Design Guide revised.***

56. Section 5.0, pg 54, Last Sentence of the First Paragraph

This sentence should read: "During initialization, the DEVICEID is placed in g0."

Affected Docs: *i960® RM/RN I/O Processor Design Guide.*

Status: ***Design Guide revised.***

57. Section 13.4.1.2, System Assumptions

Change the first sentence in item 1 to the following.

P_RST# is asserted to the i960® RM/RN I/O processor, when there is at least 0.6 µs of reliable power remaining and remains asserted as long as reliable power is available.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

58. Section 13.4.1.2, System Assumptions

Add item #2 to the list of system assumptions for the power fail sequence.

2. The PCI clock will continue to run for at least 20 clock cycles after P_RST# is asserted. The i960® RM/RN requires a PCI clock operating in the specified range of 16-33Mhz in order to complete the power fail sequence and put the SDRAM in self-refresh mode

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

59. Section 8.0, Table 8-12, 80960RM Signals Requiring Pull-Up/Down Resistors

Remove the 4th signal: RAD[1]/32BITPCI_EN# from this table. It is enabled internally.

Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

60. Section 9.5, VCCPLL Pins Requirement

The third sentence is changed to the following:

The trace lengths between the 4.7 µF capacitor, the 0.01 µF capacitor, and VCCPLL must be as short as possible.

Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

Status: ***Design Guide revised.***

61. Section 10.2, Bulk Decoupling Capacitance

Remove the word "tantalum" from the third and fifth sentences.

Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

Status: ***Design Guide revised.***

62. Section 14.1, Thermal Recommendations

The entire section is replaced with the following:

"Thermal data collected in worst case test conditions, (no airflow, an ambient temperature of 60° C with the processor executing a maximum power test), suggest the following guidance for heat sinks:

- 80960RM processor, under the conditions described above, does not require a passive heat sink.
- 80960RN processor, under the conditions described above, will require a passive heat sink.

For less than the worst case conditions above, customers can validate their own requirements for heat sinks, using anticipated air flows, ambient working temperatures, processor loads, and Section 3.2.2 (Thermal Analysis) of the 80960RN datasheet to determine if a heat sink is required for their application."

Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

Status: ***Design Guide revised.***

63. Section 4.3, VCCPLL Pins Requirement

The third sentence is changed to the following:

"The trace lengths between the 4.7 µF capacitor, the 0.01 µF capacitor, and VCCPLL must be as short as possible."

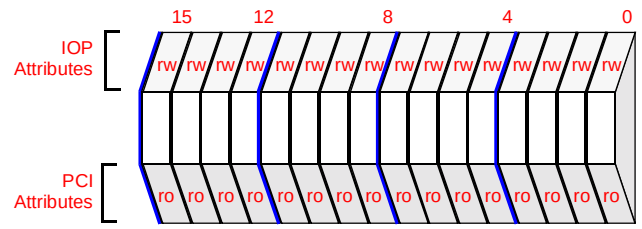
Affected Docs: *80960 RN/RM/RS I/O Processor Data Sheets.*

Status: ***Datasheet revised.***

64. Section 14.15.2 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Add table 14-26a. - Device Identification register (DIDR) for the 80960RS.

Device Identification Register - DIDR (80960RS)



PCI Configuration Offset
02 - 03H

Internal Bus Address
0000 1002H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

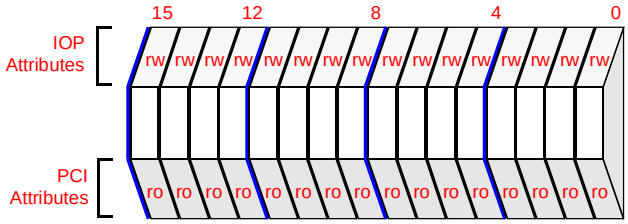
Bit	Default	Description
15:00	2962H	Device ID - This is a 16-bit value assigned to the i960 RM/RN I/O processor. This register, combined with the VID, uniquely identify any PCI device.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

65. Section 15.7.2 of the *i960® RM/RN I/O Processor Developer's Manual*

Issue: Add Table 15-30a. - ATU Device Identification register (ATUDID) for the 80960RS

ATU Device Identification - ATUDID (80960RS)



Internal Bus Address: 1202H

PCI Configuration Address Offset: 02H - 03H

Attribute Legend: RW = Read/Write, RV = Reserved, RC = Read Clear, PR = Preserved, RO = Read Only, RS = Read/Set, NA = Not Accessible

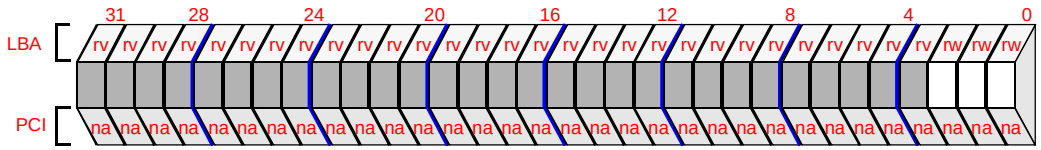
Bit	Default	Description
15:00	3962H	ATU Device ID - This is a 16-bit value assigned to the ATU and MU. This ID, combined with the VID, uniquely identify any PCI device.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual.*

66. Section 12.2.2 Bus Control Register - BCON of the *i960® RM/RN I/O Processor Developer's Manual*

Problem: Descriptions for Bit 02 and Bit 00 need to be reversed. The Register below is corrected.

Table 0-1. Bus Control Register – BCON



LBA: 86FCH

PCI: NA

Legend: NA = Not Accessible, RO = Read Only, RV = Reserved, PR = Preserved, RW = Read/Write, RS = Read/Set, RC = Read Clear, LBA = 80960 Local Bus Address, PCI = PCI Configuration Address Offset

Bit	Default	Description
31:03	0000 0000H	Reserved.
02	0_2	Supervisor Internal RAM Protection (0) = First 64 bytes not protected from supervisor mode write (1) = First 64 bytes protected from supervisor mode writes
01	0_2	Internal RAM Protection (0) = Internal data RAM not protected from user mode writes (1) = Internal data RAM protected from user mode write
00	0_2	Configuration Entries in Control Table Valid) (0) = PMCON entries not valid, default to PMCON14_15 setting (1) = PMCON entries valid

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual.*

67. Section 7.0 of the *i960® RM/RN I/O Processor Design Guide*

Problem: Change title to read Intel® 80960RN Processor Signals Requiring Pull-Up/Down Resistors

Affected Docs: *i960® RM/RN I/O Processor Design Guide*

68. Section 8.0 of the *i960® RM/RN I/O Processor Design Guide*

Problem: Change title to read Intel® 80960RM Processor Signals Requiring Pull-Up/Down Resistors

Affected Docs: *i960® RM/RN I/O Processor Design Guide*

69. Section 8.0, Table 8-12. of the *i960® RM/RN I/O Processor Design Guide*

Problem: Remove RAD[2]/32BITMEM_EN# row with related data.

Affected Docs: *i960® RM/RN I/O Processor Design Guide*

70. Section 11.3.1.5 FAIL# Code of the *i960® RM/RN I/O Processor Developer's Manual*

Problem: The verbiage in this section is residual from the *i960® Rx I/O Microprocessor Developer's Manual*, where the internal bus was accessible from the outside. The internal bus is not accessible from the outside for i960 RM/RN I/O processor. Since the customer cannot "see" the internal bus, whatever is on it is not useful and is only confusing. Therefore, this section has been removed.

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

71. Table 13-13, page 13-31 of the *i960® RM/RN I/O Processor Developer's Manual*

Problem: The error correction code can correct a single-bit error. An error of two or more bits will be treated the same. Delete the entire row in Table 13-13 which refers to "nibble. In the last row of the table, change "Double-bit" to "Multi-bit".

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

72. Section 13.3.7.3 of the *i960® RM/RN I/O Processor Developer's Manual*

Problem: The error correction code can correct a single-bit error. An error of two or more bits will be treated the same. In the first sentence of the paragraph following Table 13-13: "If decoding the syndrome indicates a double-bit or nibble error (Table 13-13), the transaction results in a target-abort." Change "double-bit or nibble error" to "multi-bit error".

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.

73. Section 13.3.7.3 of the *i960® RM/RN I/O Processor Developer's Manual*

Problem: The error correction code can correct a single-bit error. An error of two or more bits will be treated the same. In the first sentence of the second paragraph following Table 13-13: "If error reporting is enabled in the ECCR and the MCU detects a nibble, single-bit, or double-bit error, the MCU stores the address in ECARx and the syndrome in ELOGx." Change "a nibble, single-bit, or double-bit error" to "a single-bit or multi-bit error".

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual*.